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Design and Simulation of Advance Multi Precision Arithmetic Adder Using VHDL

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ABSTRACT

In the design of digital circuits using programmable logic array such as FPGA/CPLD low propagation delay, high speed & low area are the major parameter to be achieved. Digital circuits' especially digital adders are implemented through three methods Ripple carry adder, Carry look-ahead adder and Carry select adder. Ripple carry adder suffers from high area and high propagation delay and high speed. Carry select adder incorporates pair of adder and select desired output sum and carry through multiplexers. Therefore carry look ahead adder suffers from high area requirements but achieving high speed of operations. Design of homogeneous single precision adder includes either ripple carry adder or carry look-ahead adder in combination with carry select adder in combines the advantages and disadvantages of both adders. It is proposed to design hybrid multi precision adder that includes Ripple carry adder, Carry look-ahead adder and Carry select adder. Hybrid adders combine the benefits of Ripple carry adder, Carry look-ahead adder and Carry select adder. Thus dividing the 32 bit number in to section of 8 bit each achieves multi precision addition. Hybrid multi precision adder is expected to achieve low propagation delay and high speed of operation

Keywords : High Speed, Multi Precision, Low Area, Hybrid, Digital Adders

I. INTRODUCTION

In design of high speed digital adders with efficient area and power is one of the main areas of research in VLSI system design. In digital adder circuits, the speed of addition is limited by the time required for a carry to propagate through the adder. The CSA is used in many arithmetic circuits to solve the problem of carry propagation delay by generating multiple carries and then select a carry to generate the final sum [1]. However, the CSA is not area efficient because it uses various pairs of adders to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers. usually carry select adders are realize using the full adders and 2:1 multiplexers. On the other hand multi precision hybrid carry select adders involve a combination of carry select,

Ripple carry adders and carry look ahead adders. CSA belongs to the family of high speed square root time adders and provides a good cooperation between the low area occupancy of ripple carry adders and the high-speed performance of carry look-ahead adders [2].

1.1 Ripple Carry Adder

Ripple Carry Adder for N-bit numbers is implemented by joining N full adders in parallel 3, where N=8. This is called a RCA, since the carry signal "ripple" from the least significant bit position to

the most significant bit position. The carry of this adder traverses longest path called worst case delay path through N stages. The gate delay can easily be calculated by inspection of the FA circuit. In a 32-bit RCA, there are 32 full adders, so the critical path (worst case) delay is 3 (from input to carry in first adder) + 31 × 2 (for carry propagation in later adders) = 65 gate delays [1].

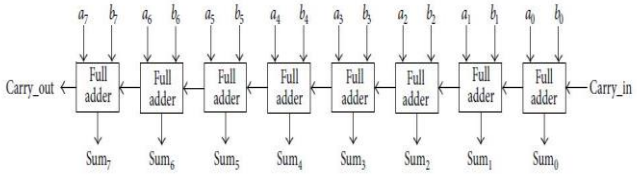


Fig -1: Ripple Carry Adder

Fig.1 depicts an 8-bit RCA, which is formed by a cascade of full adder modules. The FA is an arithmetic building block that adds augends and addends bit (say, a and b) along with any carry input (Carrying) and produces two outputs, namely, sum (Sum) and carry overflow (Carryout). Since there is a rippling of carry from one FA stage to another, the propagation delay of the RCA varies linearly in proportion to the width of the adder. A RCA is a logic circuit in which the carry-out of each FA is the carry in of the next significant full adder. It is called a RCA because every carry bit gets rippled into the next stage.

1.2 Carry Look-Ahead Adder

The CLA is faster than a RCA. A significant speed improvement in the implementation of a parallel adder was introduced by a Carry-Look-Ahead-Adder. In architectures of RCA rippling effect of the carry is still present. In CLA sum and carry is independent on the previous bit. The rippling effect has been eliminated in CLA as the dependency Cout on previous stages is completely eliminated by expanding the below equation. Thus the addition time is independent of number of bits in CLA [1]. In most cases, P (propagate bit) is simply the sum output of a half adder and G (generate bit) is the carry output of the same adder. After P and G are generated the carries for each bit position are created. Although the concept of CLA is widely understood, the concept of section-carry based carry look-ahead generator shown enclosed within the circle in fig.2 produces a single look-ahead carry signal corresponding to a "section" or "group" of the adder inputs (hence the term "section-carry"), while the conventional carry look-ahead generator encapsulated within the rectangle produces several look-ahead carry signals corresponding to each pair of augends and addend Primary inputs. The XOR and AND gates used for producing the necessary propagate and generate signals (P3 to P0 and G3 to G0) are highlighted using dotted lines in fig,2 We can calculate the generate bit, propagate bit, sum and carry in carry look-ahead generator form following equations [1].

$$C_i = G_i + P_i C_{i-1} \quad (1)$$

$$G_i = a_i b_i \quad (2)$$

$$P_i = a_i \oplus b_i \quad (3)$$

$$Sum = P_i \oplus C_{i-1} \quad (4)$$

The expressions governing a 4-bit carry look-ahead module are specified as

$$C3 = G3+P3G2+P3P2G1+P3P2P1G0+P2P1P0Cin \quad (5)$$

$$C2 = G2 + P2G1+P2P1G0 + P2P1P0Cin \quad (6)$$

$$C1 = G1+P1G0+P1P0Cin \quad (7)$$

$$C0 = G0 + P0Cin \quad (8)$$

For calculation of SUM

$$S0=P0 \oplus Cin \quad (9)$$

$$S1=P1 \oplus C0 \quad (10)$$

$$S2=P2 \oplus C1 \quad (11)$$

$$S3=P3 \oplus C2 \quad (12)$$

Where, G is a generate bit, P is a propagate bit, C is carry and S is sum. Symbol ⊕ is exclusive-or operation (XOR) [1].

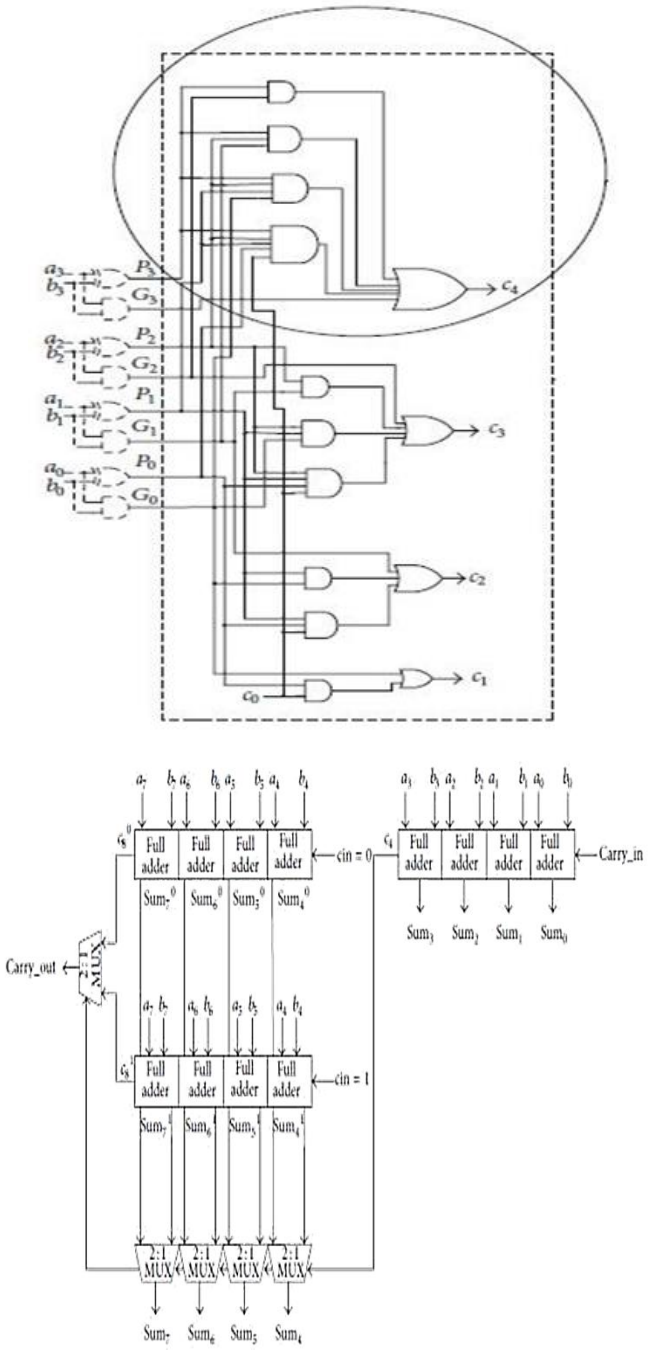


Fig -2: Carry Look-Ahead Adder

1.3 Carry Select Adder

Carry select adder belongs to the family of high speed square root time adders and provides a good cooperation between the low area occupancy of RCA and the high-speed performance of CLA. CSLAs usually involve duplication of RCA structures with presumed carry inputs of binary 0 and binary 1 to enable parallel addition and thereby speed up the addition process. The CSLA partitions the input data into groups and addition within the groups is carried out in parallel; that is, the CSLA is composed of partitioned and duplicated RCAs. It can be seen from fig.3 that the least significant 4-bit adder stages of RCA and CSLAs are equal. However, the carry produced by the least significant nibble is simply propagated through the more significant nibble in the case of the RCA bit-by-bit, while the carry corresponding to the least significant nibble serves as the selection input for Multiplexers present in the more significant situation in the case of CSLAs.

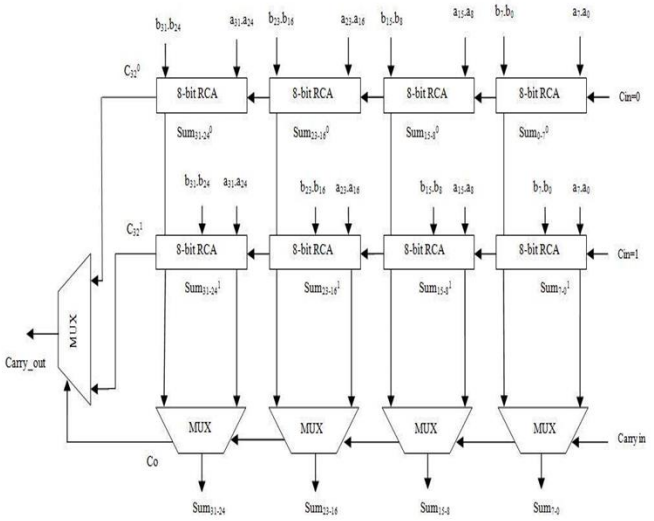


Fig -3: Carry Select Adder

II. MULTI PRECISION ADDERS

Multi precision / Hybrid adders are also known as heterogeneous adders. Hybrid adder is a combination of CSA, RCA and CLA. The interest behind hybrid adders is supported by the fact that hybrid/heterogeneous adders tend to better optimize the design metrics compared to homogeneous adders through multi precision. Hybrid adders overcome the drawbacks of homogeneous adder. Multi precision hybrids adders are used to reduce the propagation path delay and reduce the area. Hybrid adders are also use to increase the operational speed of adders. Its parallel configuration supports high performance

application. Hybrid adders are energy efficient than fixed point unit as well as floating point unit. They have a better accuracy than any other adders. And provide very large range due to multi precision. Hybrid adders help to improve the performance characteristic of the configuration.

2.1 Multi Precision using Ripple Carry Adder & Carry Select Adder

Multi precision hybrid adder using combination of ripple carry adder and carry select adder is designed. 32-bit adder consists of blocks of 8-bit ripple carry adder connected using carry select adder. Since there is a rippling of carry from one stage to another, the delay of RCA is varies linearly in proportion to the adder width. The CSA basically partitions the input data into groups and addition within the groups is carried out in parallel, that is, the CSA is composed of partitioned and duplicated RCA. It can be seen from fig.4 that the least significant 32-bit adder stages of RCA and CSA are identical. However, the carry produced by least significant bit is simply propagated through the more significant bit in the case of RCA bit-by-bit, while the carry corresponding to the least significant bit serves as the selection input for multiplexers present in the more significant position in the case of CSA.

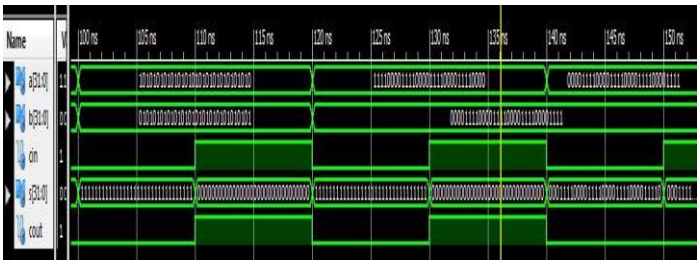


Fig -4: RCA & CSA

Waveform -1: For 32-bit RCA & CSA

32-bit multi precision using RCA & CSA was designed in VHDL using mixed style modeling that includes dataflow style and structural style of modeling. Waveform 1 shows result of addition of 32-bit numbers.

2.2 Multi Precision using Carry Look Ahead Adder & Carry Select Adder

It is known that CLA is faster than a RCA, and hence it may be worthwhile to have a CLA as a replacement for the least significant RCA in the CSA structure. The CLA along with CSA is shown in fig.5 The section-carry based carry look-ahead generator differs from a carry look-ahead generator in that bit-wise look-ahead carry signal are not required to be computed for the former It can be seen from fig.5 that the least significant 32-bit adder stages of CLA and CSA are identical. However, the carry produced by least significant bit is simply propagated through the more significant bit in the case of CLA bit-by-bit, while the carry corresponding to the least significant bit serves as the selection input for multiplexers present in the more significant position in the case of CSA

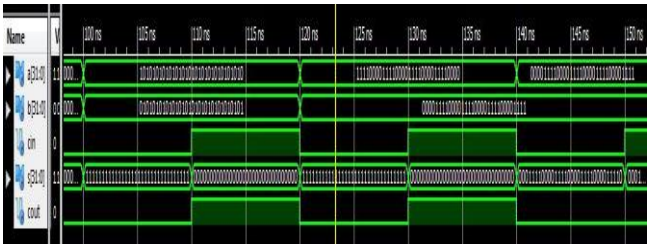
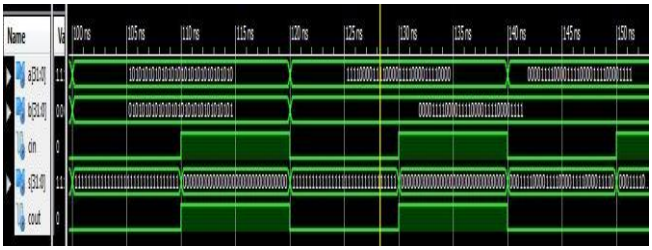


Fig -5: CLA & CSA



Waveform -2: For 32-bit CLA & CSA

32-bit multi precision using CLA & CSA was designed in VHDL using mixed style modeling that includes data flow style and structural style of modeling Waveform 2 shows result of addition of 32-bit numbers

2.3 Multiprecision using Carry Look Ahead Adder, Ripple Carry Adder & Carry Select Adder

Multi precision hybrid adder using RCA, CLA and CSA is design based on sections as shown in fig.6 Combination of RCA and CLA produces better results as compared to other hybrid adders. Here, the combine operation of both hybrid adders is very significant as compare to other hybrid adders. Hybrid adder offers excellent solution in the term of speed and area. The graphical representation of hybrid adders with the combination of RCA, CLA and CSA is given below. It is forms by cascade of RCA & CLA modules, the adder is an arithmetic building block that adds two input bits along with carry input and produce two output bit i.e. sum and carry out. The delay of RCA is varies linearly in proportion to the adder width. The carry produced by least significant bit is simply propagated through the more significant bit in the case of CLA bit-by-bit. The CSA basically partitions the input data into groups and addition within the groups is carried out in parallel, that is, the CSA is composed of partitioned and duplicated RCA and CLA

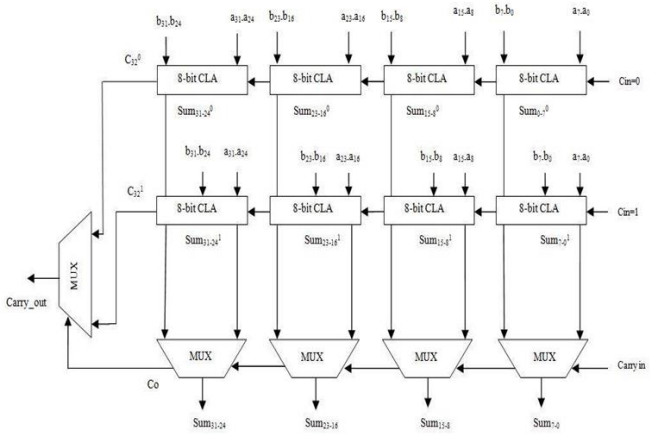
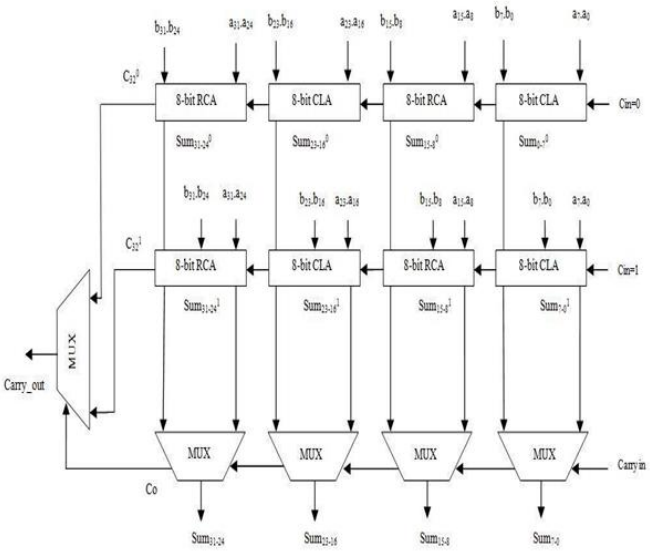


Fig -6: CLA, RCA & CSA



Waveform -3: For 32-CLA, RCA & CSA

In this 32 bit multi precision hybrid adder using RCA, CLA and CSA shows in waveform 3 achieves less propagation delay, high speed of operation and low area. Below Table 1 shows the comparison of all adders with respect to speed of operation.

Table -1: Comparison of all adders

ADDERS	DELAY	SPEED	AREA
RCA	13.33 ns	75 MHz	49
CLA	12.76 ns	78.36 MHz	48
RCA&CSA	9.6 ns	103.97 MHz	68
CLA&CSA	12.76 ns	78.36 MHz	48
RCA,CLA &RCA	9.52 ns	105.04 MHz	70

Hybrid and multi precision adders through carry look-ahead adder, ripple carry adder and carry select adder are implemented using VHDL. The designed circuits were simulated and synthesized in VHDL. The experimental results show that hybrid multi precision adder through combination of RCA, CLA

and CSA achieve lowest propagation delay and high speed of operation. However, it is observed that hybrid multi precision adder through combination of CLA and CSA achieve low area as compared to others. Most of the digital calculator, microprocessors and digital signal processor includes adders for performing addition / subtraction operation, therefore fast adder using RCA, CLA and CSA can be preferred.

III. CONCLUSIONS

In the design of parallel, multi precision hybrid 32-bit adder using ripple carry adder, carry look-ahead adder and carry select adder. For better performance of speed, propagation delay, area and device utilization. Hence it is to be concluding from the simulation and synthesis of the adders in comparison with RCA and CLA, CLA achieves higher speed and lower area than RCA. Also in comparison with respect section based an adder that includes RCA & CSA, CLA & CSA and RCA, CLA & CSA. The combination of RCA, CLA & CSA achieves highest speed of 105 MHz whereas the area required for implementation is almost similar to RCA.

IV. ACKNOWLEDGEMENT

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