# Interconnection Network of Asynchronous System 

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#### Abstract

As we know that, interconnection means, bidirectional connection of more the two autonomous computer systems, which are transfer (include memory and clock also) data's between all ports. Apart from this when a computer network is implemented as low latency, high bandwidth, energy efficiency, and robustness are several properties that are seek in networks for parallel and distributed system, also same as for asynchronous and synchronous system. As per our knowledge the network performance is not depends on only the network architecture, it depends on the number of factors which are directly related to the network characteristics, mostly depends on the speed of data exchange rate, throughput and turnaround time.


Keyword: Interconnected Network, PDN, PDS, Asynchronous System, MPI.

## I. INTRODUCTION

For the study of a large number of areas, many of the mathematicians, system designers and computer scientists has applied interconnection networks. As we know that, interconnection means, bidirectional connection of more the two autonomous computer systems, which are transfer (include memory and clock also) data's between all ports. Apart from this when a computer network is implemented as low latency, high bandwidth, energy efficiency, and robustness are several properties that are seek in networks for parallel and distributed system, also same as for asynchronous and synchronous system. As per our knowledge the network performance is not depends on only the network architecture, it depends on the number of factors which are directly related to the network characteristics, mostly depends on the speed of data exchange rate, throughput and turnaround time.

## II. METHODS AND MATERIAL

## Perfect Difference Network

Perfect Difference Network (PDN) that are based on mathematical notation of prefect difference sets, have already been shown to comprise an asymptotically optional method for connecting a number of nodes with
diameter 2 [5].

So, that all nodes are directly connected with one another node that means the data communicate in all direction where the nodes are placed. According to the definition of PDN, we can say that it is an example of interconnection network. In theoretically we explain this in terms of asynchronous system. We know the definition of asynchronous system and distributed system explains in our paper [6] according to that definition we assume all the nodes of PDN is represent processors, and the connection lines is like as a links or channel or communication medium (figure 5.). All processors are performing jobs individually (including sending or receiving messages and also the execution of task also). When the processor is working simultaneously it cannot share their memory and clocks. That means the interconnection network is an example of distributed system and transmitting data as asynchronously, i.e. an interconnection network is simulated as asynchronous system.

As we know," The perfect difference networks are depending on the mathematical notion of perfect difference sets, diameter of 2 in an asymptotically optimal manner" by J. M. Singer, we refer it constitute high performance interconnection networks for parallel and distributed system. Let's explain:

Let X be a n set of integer $0,1, \mathrm{n}-1$ module is $\mathrm{N}, \mathrm{D}$ is a set of diameter, where,
$\mathrm{D}=\mathrm{d}_{1}, \mathrm{~d}_{2}, \mathrm{~d}_{3}, \ldots \ldots \ldots \ldots \ldots \mathrm{~d}_{\mathrm{k}}$.

Where,
k is a subset of x for every $\mathrm{a} \neq 0$ i.e. $\bmod \mathrm{N}$, the simple difference set for each of the possible difference is:

$$
\begin{aligned}
& \mathrm{d}_{\mathrm{i},} \mathrm{~d}_{\mathrm{j}} \mathrm{i} \neq \mathrm{j} \text { such that } \\
& \mathrm{d}_{\mathrm{i}}-\mathrm{d}_{\mathrm{j}}=\mathrm{a}(\bmod \mathrm{~N})
\end{aligned}
$$

If $D$ fulfill all requirement is called a perfect difference set, which is create an interconnection network. Those interconnection networks are transmitting data in all the possible exits, these exits are the processor ports. Thus, they are receiving data in every node.

According to the remainder theorem:

$$
\begin{align*}
& \mathrm{R}=\mathrm{N}-\mathrm{D} * \mathrm{Q}  \tag{1}\\
& \mathrm{~N}=\mathrm{R}+\mathrm{D} * \mathrm{Q}  \tag{2}\\
& \mathrm{R}=\mathrm{N} \bmod \mathrm{D} \tag{3}
\end{align*}
$$

### 2.1 Perfect Difference Set

PDS have already been show to comprise an asymptotically optimal method for connecting a number of nodes into a network with diameter 2 . We know that PDS is a set of $\left\{\delta_{0}, \delta_{1}, \delta_{2}, \ldots, \delta_{n}\right\}$ of $\delta+1$ integers having the property that their $\delta^{2+} \delta$ differences $\delta_{i}-\delta_{j}$.

Where, $\quad 0<=\mathrm{i}$,

$$
\mathrm{j}<=\delta
$$

It represent congruent module i.e. $\delta^{2+} \delta+1$ to the integer in some order is a perfect difference set of which order is define as a terms of diameter.

Definition 2.1: PDS is a set of $\left\{\mathrm{s}_{0}, \mathrm{~s}_{1}, \mathrm{~s}_{2}, \ldots, \mathrm{~s}_{\delta}\right\}$ of $\delta+1$ integers having the property that their $\delta^{2+} \delta$ difference $\delta_{\mathrm{i}}$ - $\delta_{\mathrm{j}}, 0 \leq \mathrm{i} \neq \mathrm{j} \leq \delta$ are congruent module [5].

According to the definition of PDS, we have the result i.e. a sufficient condition that have their exists $\delta+1$ integers $\mathrm{s}_{0}, \mathrm{~s}_{1} \ldots \mathrm{~s}_{\delta}$, having the property that their $\delta^{2}+\delta$ differences $s_{i}-s_{j}$,
where $\mathrm{i} \neq \mathrm{j}, 0 \leq \mathrm{i}, \mathrm{j} \leq \delta$ are congruent modulo $\delta_{2}+\delta+$ 1 , is integers value always, $1,2, \ldots \ldots, \delta^{2}+\delta$ in some order is that $\delta$ be a prime number or power of a prime
number.
We know, $\delta \rightarrow$ prime or power of prime
Then,

$$
\begin{equation*}
\mathrm{n}=\delta^{2}+\delta+1 \tag{4}
\end{equation*}
$$

Definition 2.2: $A\left\{\mathrm{~s}_{0}, \mathrm{~s}_{1}, \mathrm{~s}_{2}, \ldots, \mathrm{~s}_{\delta}\right\}$ of $\delta+1$ integers value having the property that their $\delta^{2}+\delta$ differences $\mathrm{s}_{\mathrm{i}}-$ $\mathrm{s}_{\mathrm{j}}, 0 \leq \mathrm{i} \neq \mathrm{j} \leq \delta$ are concurrent module. Then the integer modulo $\delta^{2}+\delta+1$, to the integers $1,2, \ldots, \delta^{2}+\delta$. In some order is a PDS of order $\delta$. The simple difference set is also known as perfect difference sets 4 , it is given that they correspond to the special $\lambda=1$ case of difference sets for which each of the possible difference is formed in exactly $\lambda$ ways.

Then we have found that the PDS not satisfy the closer property that means a PDS need not contain an integer outside the interval $\left\{0 . . \delta^{2}+\delta\right\}$

The value of $n$ is $7,13,31,57$.
By the equation: (3) we have several results as example,

| $\boldsymbol{\delta}$ | $\boldsymbol{\delta}^{\mathbf{2}+\boldsymbol{\delta}}$ | $\boldsymbol{\delta}^{\mathbf{2}+\boldsymbol{\delta}+\mathbf{1}}$ |
| :---: | :---: | :---: |
| 2 | 6 | 7 |
| 3 | 12 | 13 |
| 5 | 30 | 31 |
| 7 | 56 | 57 |
| 9 | 90 | 91 |
| 11 | 132 | 133 |
| 13 | 182 | 183 |
| 17 | 306 | 307 |
| 19 | 380 | 381 |
| 23 | 552 | 553 |

Table: 2.1
By the definition, any perfect difference set contains a pair of integers $s_{x}$ and
$\mathrm{s}_{\mathrm{y}}$ such that $\mathrm{s}_{\mathrm{x}}-\mathrm{s}_{\mathrm{y}}=1 \bmod \delta^{2}+\delta+1$
If we assume $\delta=2$ then the value of $\mathrm{n}=7$
Let explain in number scale


For all $n=7$ the PDS is $\{ \pm 0, \pm 1, \pm 3\}$ i.e. $\{0,1,3\}$
According to the definition, for all intervals $\left\{0 . . \delta^{2}+\delta\right\}$ the PDS is, if $\mathrm{n}=7$, then we get the $\operatorname{PDS}\{0,1,3\}$. The normal PDS is reduced if it contains the integers 0 and 1 . Hence the definition is

Definition 2.3: A PDS $\left\{\mathrm{s}_{0}, \mathrm{~s}_{1}, \mathrm{~s}_{3}\right.$. $\left.\mathrm{s}_{\delta}\right\}$ is reduced if it contains the integer number 0 and 1 , A reduced PDS is satisfies follows condition.
a) $\quad \mathrm{s}_{\mathrm{i}}<\mathrm{s}_{\mathrm{i}+1} \leq \delta^{2}+\delta$
b) $\quad 0 \leq$ i $<\delta$

But, the equivalent PDS have the same normal form $\{0$, $\left.1, s_{2}, \ldots, s_{\delta}\right\}$ hence the definition is for equivalent PDS.

Definition 2.4: If two different PDS's are equivalent when they have the same normal form $\left\{0,1, \mathrm{~s}_{2}, \ldots, \mathrm{~s}_{\delta}\right\}$. By the definition of PDS's, we take a chordal ring structure of the PDN with $\mathrm{n}=7$ nodes based on the perfect difference set $\{0,1$, and 3$\}$.


Figure: 2.1 Chordal Representations
Here, the value of $\delta$ is 2 and $n=\delta^{2}+\delta+1$.
Where we assume that all the points of chordal is similarly represent the processors. They are interconnected with each other to communicate data with ones to another. This representation is similar as a


Figure: 2.2
That means the chordal representation is represent the connection of nodes or processors, they are placed in anywhere in the surrounding of the world. It shows either the global connection of internet, in which user machine are connected with another machine which is placed on different countries.

Lemma 1: In PDS $2^{\text {n }}$ differences.
Proof: Let us explain in another sense,

$$
\begin{array}{ll}
\Rightarrow & \mathrm{T}_{0}=0=(0-0) \\
\Rightarrow & \mathrm{T}_{1}=1=(1-0) \\
\Rightarrow & \mathrm{T}_{2}=2=(3-1) \\
\Rightarrow & \mathrm{T}_{5}=3=(3-0) \\
\Rightarrow & \mathrm{T}_{4}=4=(0-3) \\
\Rightarrow & \mathrm{T}_{5}=5=(1-3) \\
\Rightarrow & \mathrm{T}_{6}=6=(0-1)
\end{array}
$$

Where, $\mathrm{T}_{1}$ is the mirror image of $\mathrm{T}_{6}, \mathrm{~T} 2$ is the mirror image of $\mathrm{T}_{5}$, and,
$\mathrm{T}_{3}$ is the mirror image of $\mathrm{T}_{4}$.
Then,
By, the reason of definition the perfect difference network is the property of reminder theorem;
$\Rightarrow \mathrm{N}=\mathrm{R}+\mathrm{D} * \mathrm{Q}$ from the equation (2),

$$
\begin{align*}
& \Rightarrow s_{i}-s_{j}=\delta^{2}+\bmod \delta^{2}+\delta+1 \\
& \Rightarrow N=R+D * Q \\
& \Rightarrow N=\left(R_{1}-R_{2}\right)+D * Q \tag{5}
\end{align*}
$$

In equation (5), assume the value of $\mathrm{Q}=1$ and put it in
equation (5).

Then we get the results,

$$
\begin{align*}
& \Rightarrow N=\left(R_{1}-R_{2}\right)+D  \tag{6}\\
& \Rightarrow R_{1}-R_{2}=N-D \\
& \Rightarrow R_{2}=R_{1}-(N-D) \\
& \Rightarrow R_{2}=R_{1}-N+D \tag{8}
\end{align*}
$$

(7) $\quad=>\mathrm{R}_{1}=$
$\mathrm{N}-\mathrm{D}+\mathrm{R}_{2}$
Put, $\mathrm{R}_{2}=0$, in equation (8) and, $\mathrm{R}_{1}=0$, in equation (7)
Hence, we get from equation (8):

$$
\begin{equation*}
\Rightarrow \mathrm{R}_{1}=\mathrm{N}-\mathrm{D} \tag{9}
\end{equation*}
$$

And, from equation (7):
$\Rightarrow R_{2}=-N+D$

Again, we put the value of $\mathrm{R}_{2}=1$ in equation (8) and $\mathrm{R}_{1}$ $=1$ in equation (7)
Hence, the result is:
$\Rightarrow \mathrm{R}_{2}=\mathrm{N}-\mathrm{D}+1$
\{from equ. 8\}
$\Rightarrow R_{1}=1-\mathrm{N}+\mathrm{D}$
\{from equ. 7\}
If $\mathrm{N}=\{0,1,2,3,4,5,6\}$

Then, we have put all these value in equ. (8),
And, also assume the value of $\mathrm{R}_{2}=0$ for all cases
$\Rightarrow \mathrm{N}=0 \Rightarrow \quad \mathrm{R}_{1}=\mathrm{D}$
$\Rightarrow \mathrm{N}=1 \Rightarrow \quad \mathrm{R}_{1}=(1-\mathrm{D})$
$\Rightarrow \mathrm{N}=2 \Rightarrow \quad \mathrm{R}_{1}=(2-\mathrm{D})$
$\Rightarrow \mathrm{N}=3 \Rightarrow \quad \mathrm{R}_{1}=(3-\mathrm{D})$
$\Rightarrow \mathrm{N}=4 \Rightarrow \quad \mathrm{R}_{1}=(4-\mathrm{D})$
$\Rightarrow \mathrm{N}=5 \Rightarrow \quad \mathrm{R}_{1}=(5-\mathrm{D})$
$\Rightarrow \mathrm{N}=6 \Rightarrow \quad \mathrm{R}_{1}=(6-\mathrm{D})$

Again, in a chordal ring structure as shown in figure: 2.1 all nodes are 7 then, the value of D is also 7 .
Put, if $\mathrm{D}=7$ in equation (8) then,

$$
\begin{array}{ll}
\Rightarrow & \mathrm{R}_{1}=0-7=-7=>0 \\
\Rightarrow & \mathrm{R}_{1}=1-7=-6=>1 \\
\Rightarrow & \mathrm{R}_{1}=2-7=-5=>2 \\
\Rightarrow & \mathrm{R}_{1}=3-7=-4 \Rightarrow>3 \\
\Rightarrow & \mathrm{R}_{1}=4-7=-3=>4 \\
\Rightarrow & \mathrm{R}_{1}=5-7=-2 \Rightarrow 5 \\
\Rightarrow & \mathrm{R}_{1}=6-7=-1=>6
\end{array}
$$

But, for all cases $R_{1}-R_{2}=-1$ is not working. If $R_{2}=D-N$ when, $R_{1}=0$ for all cases by the equation (8)

Then,

$$
\begin{array}{lll}
\Rightarrow & \mathrm{R}_{2}=7-0 & \Rightarrow 7 \\
\Rightarrow & \mathrm{R}_{2}=7-1 & \Rightarrow 6 \\
\Rightarrow & \mathrm{R}_{2}=7-2 & =>5
\end{array}
$$

$$
\begin{array}{lll}
\Rightarrow & \mathrm{R}_{2}=7-3 & \Rightarrow>4 \\
\Rightarrow & \mathrm{R}_{2}=7-4 & \Rightarrow>3 \\
\Rightarrow & \mathrm{R}_{2}=7-5 & \Rightarrow>2 \\
\Rightarrow & \mathrm{R}_{2}=7-6 & \Rightarrow>1 \\
\Rightarrow & \mathrm{R}_{2}=7-7 & \Rightarrow>0
\end{array}
$$

$\Rightarrow \mathrm{R}_{1}=$ Hence, we have the perfect difference set in 7 nodes chordal ring is $\{0,1,3\}$
$\Rightarrow \mathrm{s}_{\mathrm{i}}-\mathrm{s}_{\mathrm{j}}=\left(\delta^{2}+\delta\right) \bmod \left(\delta^{2}+\delta+1\right)$
$\Rightarrow 0-1=\mathrm{n} \bmod 7 \Rightarrow \mathrm{n}=(0-1)+7=6$
$\Rightarrow 0-3=\mathrm{n} \bmod 7 \Rightarrow \mathrm{n}=(0-3)+7=5$
$\Rightarrow 1-3=\mathrm{n} \bmod 7 \Rightarrow \mathrm{n}=(0-3)+7=4$
$\Rightarrow 1-0=\mathrm{n} \bmod 7=>\mathrm{n}=(1-0)+7=8 \% 7=1$

Where, 1 is a reminder by reminder theorem.

$$
\Rightarrow 3-0=n \bmod 7 \Rightarrow n=(3-0)+7=10 \% 7=3
$$

Where, 3 is a reminder by reminder theorem.
$\Rightarrow 3-1=\mathrm{n} \bmod 7 \Rightarrow \mathrm{n}=(3-1)+7=9 \% 7=2$

Where, 2 is a reminder by reminder theorem.
Hence we have $2^{\mathrm{n}}$ difference in 7 nodes chordal ring the PDS.

For example: $2^{n}=2^{3}=>8$ assume $n=3$ where is the no of members in PDS

Lemma 2: The ${ }^{\mathrm{n}} \mathrm{P}_{2}$ mirror image in a PDN.
Proof: $\{\varnothing\},\{0\},\{0,1\}\{0,3\},\{1,1\},\{0,3\},\{3,3\}$

$$
\begin{aligned}
& 3_{c_{2}}=\frac{\angle 3}{\angle 3 \angle 3-2}=\frac{\angle 2}{\angle 3 \angle 3}=3 \\
& \quad(0,1)(0,3)(1,3) \\
& 3_{P_{2}}=\frac{\angle 3}{\angle 3-2}=\frac{3 \times 2 \times 1}{1}=6 \\
& \{0,0\},\{0,1\}\{0,3\},\{1,1\},\{1,3\},\{3,3\} \\
& \{0-0\},\{0-1\}\{0-3\},\{1-1\},\{1-3\},\{3-3\} \\
& \{1-0\},\{3-0\}\{3-1\}
\end{aligned}
$$

### 2.2 Asynchronous Communication in Interconnection Network

We know that, the normal PDS $\left\{0,1, S_{2} \ldots \ldots . S_{\delta}\right\}$ of order $n$, by this we can construct a direct interconnection network with a node n . where, $\mathrm{n}=\delta^{2}+\delta+1$.

Definition 2.5: The PDN based on the normal-from of $\operatorname{PDS}\left\{0,1, S_{2}, \ldots \ldots S_{\delta}\right\}$ and it have $n$ nodes; they are numbered 0 to $\mathrm{n}-1$. The node is directed connected via nodes $\mathrm{i} \pm 1$ and $\mathrm{i} \pm \mathrm{S}_{\mathrm{j}}(\bmod \mathrm{n})$ for $2 \leq \mathrm{j} \leq \delta$.

For Every normal PDS contains 1 as a member. Therefore, PDN's based on normal form PDS's are special types of chordal rings. In chordal ring technology, the links connecting with i and $\mathrm{i}+1$ connecting ring links, while these that connect with nodes i and $\mathrm{i}+\mathrm{S}_{\mathrm{j}}$ are non-connecting $\square, 2 \leq \mathrm{j} \leq$ skip links or chords. The links are connected with i node and $\mathrm{i}+\mathrm{S}_{\mathrm{j}}$ nodes. In which node $i$, is a formal-skip node and node $\mathrm{i}+\mathrm{S}_{\mathrm{j}}$ is backward skip nodes. By this reason we can also says, the ring link for i is forward link and $\mathrm{i}+1$ is backward ring.

Lemma 3: The message passing over a PDN is asynchronously.

## Proof:-

For asynchronous communication again we take seven nodes chordal ring shown in figure: 2.1 ,

$$
\begin{aligned}
& =>\mathrm{T}_{0}=\mathrm{T}_{1}+\mathrm{T}_{3}+\mathrm{T}_{4}+\mathrm{T}_{6}=\mathrm{T}_{7} \\
& =>\mathrm{T}_{1}=\mathrm{T}_{0}+\mathrm{T}_{2}+\mathrm{T}_{4}+\mathrm{T}_{5}=\mathrm{T}_{8} \\
& =>\mathrm{T}_{2}=\mathrm{T}_{1}+\mathrm{T}_{3}+\mathrm{T}_{5}+\mathrm{T}_{6}=\mathrm{T}_{9} \\
& \Rightarrow>\mathrm{T}_{3}=\mathrm{T}_{2}+\mathrm{T}_{4}+\mathrm{T}_{0}+\mathrm{T}_{6}=\mathrm{T}_{10} \\
& \Rightarrow>\mathrm{T}_{4}=\mathrm{T}_{1}+\mathrm{T}_{0}+\mathrm{T}_{3}+\mathrm{T}_{5}=\mathrm{T}_{11} \\
& =>\mathrm{T}_{5}=\mathrm{T}_{4}+\mathrm{T}_{6}+\mathrm{T}_{2}+\mathrm{T}_{1}=\mathrm{T}_{12} \\
& \Rightarrow>\mathrm{T}_{6}=\mathrm{T}_{2}+\mathrm{T}_{3}+\mathrm{T}_{0}+\mathrm{T}_{5}=\mathrm{T}_{13}
\end{aligned}
$$

With different clock in message will be passed in different channel, these are shown in follows figure: 2.3. In every node connected with the other node that means in interconnection network every machine has store own address and the recipient machine port address by this all machine are transforming data between each other. But, in this distributed data processing machine architecture all machine communicated message in asynchrously. Hence, it is prove that in all interconnection networks passed message through that channel is asynchronous at a part of given interval.


Figure: 2.3

Again,

$$
\begin{aligned}
& \Rightarrow \mathrm{T}_{7} \quad \Rightarrow \mathrm{~T}_{1}+\mathrm{T}_{3}+\mathrm{T}_{4}+\mathrm{T}_{6} \\
& \Rightarrow \mathrm{~T}_{1}+\left(\mathrm{T}_{0}+\mathrm{T}_{2}\right)+\left(\mathrm{T}_{0}+\mathrm{T}_{5}\right)+\mathrm{T}_{6} \\
& \Rightarrow 2 \mathrm{~T}_{0}+\mathrm{T}_{1}+\mathrm{T}_{2}+\mathrm{T}_{5}+\mathrm{T}_{6}
\end{aligned}
$$



Figure: 2.3 DAG representation of interconnection network. Where $T_{i}$ is connected to the $T_{n}$.

Apply the above architecture for all nodes hen we get the result of all nodes.
Hence, the convergency and divergency of algorithms suggest the creation on of vector fields.

$$
\begin{aligned}
& \Rightarrow \mathrm{T}_{7} \Rightarrow \mathrm{~m}_{\mathrm{mod}} 7 \\
& \Rightarrow \mathrm{~T}_{8} \Rightarrow \mathrm{~T}_{0}+\mathrm{T}_{2}+\mathrm{T}_{4}+\mathrm{T}_{5} \\
& =>\mathrm{T}_{8}=>1 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{9} \Rightarrow \mathrm{~T}_{1}+\mathrm{T}_{3}+\mathrm{T}_{5}+\mathrm{T}_{6} \\
& \Rightarrow \mathrm{~T}_{9} \Rightarrow 2 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{10}=>\mathrm{T}_{0}+\mathrm{T}_{2}+\mathrm{T}_{4}+\mathrm{T}_{6} \\
& \Rightarrow>\mathrm{T}_{10} \Rightarrow 3 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{11} \Rightarrow \mathrm{~T}_{0}+\mathrm{T}_{1}+\mathrm{T}_{3}+\mathrm{T}_{5} \\
& \Rightarrow>\mathrm{T}_{11} \Rightarrow 4 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{12}=>\mathrm{T}_{1}+\mathrm{T}_{2}+\mathrm{T}_{4}+\mathrm{T}_{6} \\
& \Rightarrow \mathrm{~T}_{12} \Rightarrow 5 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{13}=>\mathrm{T}_{0}+\mathrm{T}_{2}+\mathrm{T}_{3}+\mathrm{T}_{5} \\
& \Rightarrow \mathrm{~T}_{13}=6 \bmod 7 \\
& \Rightarrow>\mathrm{T}_{14}=7 \bmod 7
\end{aligned}
$$

With, different clocks the message will be passed in following network of PDN. The message will be passed to as master processor in the following manner.

$$
\begin{aligned}
& \Rightarrow>\mathrm{T}_{0}=\mathrm{T}_{7} \Rightarrow>0 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{1}=\mathrm{T}_{8} \Rightarrow>1 \bmod 7 \\
& =>\mathrm{T}_{2}=\mathrm{T}_{9} \Rightarrow 2 \bmod 7 \\
& \Rightarrow>\mathrm{T}_{3}=\mathrm{T}_{10} \Rightarrow>3 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{4}=\mathrm{T}_{11} \Rightarrow 4 \bmod 7 \\
& \Rightarrow \mathrm{~T}_{5}=\mathrm{T}_{12} \Rightarrow 5 \bmod 7 \\
& \Rightarrow>\mathrm{T}_{6}=\mathrm{T}_{13} \Rightarrow 6 \bmod 7
\end{aligned}
$$

i.e., the above processor can be explained in matrix multiplication by using message-passing interconnection. It is known as interconnection communication in asynchronous system in perfect difference networks.
For multicore PDN we assume that according to the
above figure: 5.3
$\Rightarrow \mathrm{T}_{0}+\mathrm{T}_{1}=\mathrm{T}_{0}+\mathrm{T}_{6}$
$\Rightarrow \mathrm{T}_{0}+\mathrm{T}_{3}+\mathrm{T}_{2}=\mathrm{T}_{0}+\mathrm{T}_{4}+\mathrm{T}_{5}$
$\Rightarrow \mathrm{T}_{7}=>0 \bmod 7$
$\Rightarrow \mathrm{T}_{7}=\left(\mathrm{T}_{0}+\mathrm{T}_{1}\right)+\left(\mathrm{T}_{0}+\mathrm{T}_{6}\right)+\left(\mathrm{T}_{0}+\mathrm{T}_{3}+\mathrm{T}_{2}\right)+$ $\left(\mathrm{T}_{0}+\mathrm{T}_{3}+\mathrm{T}_{2}\right)$
$\Rightarrow \mathrm{T}_{7}=\mathrm{T}_{0} \bmod 7$
i.e., the communication latency is $\mathrm{T}_{0}+\mathrm{T}_{6}=\mathrm{T}_{0}+$ $\mathrm{T}_{1}=\mathrm{T}_{0}+\mathrm{T}_{4}=\mathrm{T}_{0}+\mathrm{T}_{3}=\mathrm{T}_{4}+\mathrm{T}_{5}=\mathrm{T}_{3}+\mathrm{T}_{2}$
Hence, the nodes $\mathrm{T}_{0}, \mathrm{~T}_{1}, \mathrm{~T}_{3}$ and $\mathrm{T}_{4}$ are in direct communication with the main node which is $\mathrm{T}_{0}$. And, also the node $T_{5}$ and $T_{2}$ are indirect connected with $T_{0}$. Apart from this all the above declare nodes are interconnected and passed message in asynchronously. But there is no communication between
$\left(\mathrm{T}_{6} \& \mathrm{~T}_{5}\right)$, $\left(\mathrm{T}_{1} \& \mathrm{~T}_{2}\right)$, and $\left(\mathrm{T}_{4} \& \mathrm{~T}_{3}\right)$ is according to the figure: 5.3.
According to the above interconnection network we refer several issues as follows:
$>$ Total communication time of a complete graph is always greater than the total communication time of an interconnection network.
$>$ Total number of circuits in a complete graph is always greater than the total no of circuits of an interconnection network.
$>$ Minimum communication time in a complete graph is always greater than the minimum communication time of an interconnection network.
$>$ Minimum communication time in an interconnection network of $\delta=2$ is equal to 6 edges, which lies between all the seven nodes.
Again we can say according to our research, in an interconnection network:
$>$ More circuits more communication.
$>$ More circuit more robustness.
> More circuit more expansive.

## III. RESULTS AND DISCUSSION

### 3.1 Stransen Matrix Multiplication in MPI

Here, we had given stranssen's algorithm for matrix multiplication in its original notation [1]. First divided the input matrices A ; B and the output matrix C into 4 sub matrices:
$\mathrm{A}=\left[\begin{array}{ll}A_{11} & A_{12} \\ A_{21} & A_{22}\end{array}\right], \quad \mathrm{B}=\left[\begin{array}{ll}B_{11} & B_{12} \\ B_{21} & B_{22}\end{array}\right]$ and $\quad \mathrm{C} \quad=$ $\left[\begin{array}{ll}C_{11} & C_{12} \\ C_{21} & C_{22}\end{array}\right]$.

Then, for one step of the algorithm, compute the following quantities:
$\mathrm{I}=\left(\mathrm{A}_{11}+\mathrm{A}_{12}\right) *\left(\mathrm{~B}_{11}+\mathrm{B}_{12}\right)$
II $=\left(\mathrm{A}_{21}+\mathrm{A}_{22}\right) * \mathrm{~B}_{11}$
III $=\mathrm{A}_{11} *\left(\mathrm{~B}_{12}-\mathrm{B}_{22}\right)$
$\mathrm{IV}=\mathrm{A}_{22} *\left(\mathrm{~B}_{21}-\mathrm{B}_{11}\right)$
$\mathrm{V}=\left(\mathrm{A}_{11}+\mathrm{A}_{12}\right) * \mathrm{~B}_{22}$
$\mathrm{VI}=\left(\mathrm{A}_{21}-\mathrm{A}_{11}\right) *\left(\mathrm{~B}_{11}+\mathrm{B}_{12}\right)$
$\mathrm{VII}=\left(\mathrm{A}_{12}-\mathrm{A}_{22}\right) *\left(\mathrm{~B}_{21}+\mathrm{B}_{22}\right)$
And the output is:

$$
\begin{aligned}
& \mathrm{C}_{11}=\mathrm{I}+\mathrm{IV}-\mathrm{V}+\mathrm{VII} \\
& \mathrm{C}_{12}=\mathrm{II}+\mathrm{IV} \\
& \mathrm{C}_{21}=\mathrm{III}+\mathrm{V} \\
& \mathrm{C}_{22}=\mathrm{I}+\mathrm{III}-\mathrm{II}+\mathrm{VI}
\end{aligned}
$$

That means the algorithm is recursive since it can be used for each of the 7 smaller matrix multiplications. The recursion for the computational cost of the algorithm is $\mathrm{F}(\mathrm{n})=7 \mathrm{~F}(\mathrm{n} / 2)+18 \mathrm{n}^{2}$, yielding a solution of

$$
F(n)=6 n^{\lg 7}-5 n^{2}
$$

For $n$ a power of two and using a base case of $n=1$.

### 3.2 Limit of Synchronization In Interconnection Network

1) Multicore System: It is a single computing component with two or more independent actual processing units, these units are also known as "cores". They are executing programming instructions and codes. The instructions are either arithmetic operation or other general instructions. But the multiple cores can run multiple instructions at the same execution time, increasing overall speed for programs amenable to synchronous system. In a multi-core processor implemented multiprocessing in a single physical package. Processors were originally developed with only one core. In the mid-1980s Rockwell International manufactured versions of the 6502 with two 6502 cores on one chip as the R65C00, R65C21, and R65C29 [2], sharing the chip's pins on alternate clock phases. Other multi-core processors were developed in the early 2000s by Intel, AMD and others. The
main factor of multicore system is to perform highly at lower energy. For example: Mobile devices.
2) Parallel And Distributed Data Processing System: Both systems can be defined as a collection of processing elements that communicate data's and process then to achieve a certain goals. In present environment, parallelism of machine using at all levels of technologies. Within each CPU's by executing multiple instructions from the same thread of control, simultaneously, thus make parallel systems. Simultaneously, advances in networking technology have created an explosion of distributed applications, making distributed computing an inherent fabric in our day-to-day lives. A system in which all components located at network and communicate data's and information through the communication medium with the help of communication media and coordinates their actions only by passing message ones to another, but remember that all machine are placed in different places.
3) Cloud Computing: Cloud computing metaphor: For a user, the network elements representing the provider-rendered services are invisible, as if obscured by a cloud [3]. Cloud computing is a model for enabling convenient, on-demand access to a shared pool of configurable computing resources [4]. Cloud computing and storage solutions provide users and enterprises with various capabilities to store and process their data in third-party data centers.
4) Internet: The internet is a network of networks which connects computers all over the world. The term "internet" has been coined by the combination of two words namely "interconnectivity" and "networks". Thus, the definition of internet we can also say that, it is interconnectivity of networks. It is the vast pool of resources that offers different opportunities to different people. We gave several concepts about internet as:

- It is an ocean of information waiting to be dived into.
- It is the place where we can show our
company's presence all over the world.
- It offers employment opportunities all over the world.
- It is a source of entertainment to young and old in all over the world.

Computers connected to the internet, communicates by using IP (internet protocol), that slices the information into packets and routes them to their destination. Along with IP, most computers on the internet communicate with TCP and the combination is known as TCP/IP. Each computer on internet is called a host or host computer. The computers on internet are connected by cables, phone lines and satellite connections.

## IV. REFERENCES

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