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Design Implementation of High-Performance Pipelined ADC

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ABSTRACT

This paper presents Design Implementation of High-Performance ADC in Deep-Submicron Technology. The Analog-to-Digital Converter (ADC) is the main link between the analog input and DSP part. However, for applications like hand-held or wireless devices, ADC should be featured with low power and high speed. The pipeline ADC architecture is best suitable for medium resolution, low power and high-speed applications. For design point of it is very flexible for power and area constraints. Main building-blocks in each stage of the pipelined ADC are sample and hold, sub-ADC, sub DAC and amplifier. First few implementations for each sub-block were reviewed. Then by selecting appropriate blocks 8-Bit pipelined ADC with sampling frequency 100 MHz is designed using CMOS TSMC 0.18 μm technology. The design has 1-Bit stage resolution. The power dissipation of the implemented ADC is found less than 82mW. Second Design shows the 1-Bit resolution with a power dissipation of 56 mW. By few modifications in design, effect of stage resolution and effect of other amplifier topology on power is observed. The analysis is very useful to decide the stage resolution. This power analysis is supported by suitable simulation results.

Keywords : Analog to Digital Converters (ADCs), Propagation delay, Offset Voltage, Power Dissipation, Comparator, Operational Amplifier (OP-AMP)

I. INTRODUCTION

Analog-to-digital converters (ADCs) are very important building blocks in modem signal processing and communication systems. For signal processing, digital domain is preferred over analog domain because of its advantages such as noise immunity, storage capability, security etc. For long distance, digital communication is more reliable due to regenerative repeater. Due to these, today nearly all modern electronics are primarily digitally operated, allowing for advanced digital signal processing (DSP). But the real world signals such as signals coming from various transducers are analog in nature. This analog signal must be converted into digital to allow digital signal processing. This is done by Analog to Digital Converter (ADC) as shown in Figure 1[1-3]. The applications of ADC include DC instruments, process control, thermocouple sensors, modems, digital radio, video signal acquisition etc. The ADC should be featured with low power and higher speed due to many reasons. First the rapid advent of battery operated portable system requires low power dissipation in order to prolong battery life, and a minimum number of battery cells to reduce the volume and weight of the system. Another reason is the smaller feature sizes offered by today's VLSI technology[1-4].

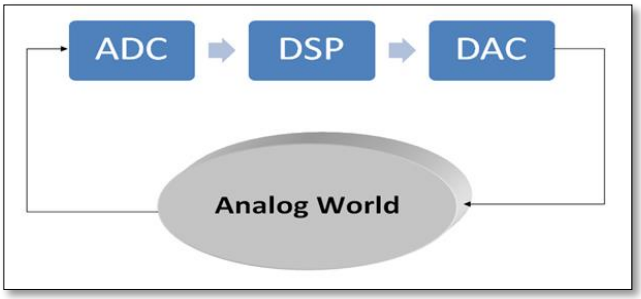

Figure 1. Data Conversion Flow

Many good ADC architectures have been invented to satisfy different requirements in different applications. To name some: flash ADC, folding and interpolating ADC, two-step ADC, pipeline ADC, successive-approximation-register (SAR) ADC, delta-sigma ADC, integrating ADC etc. Their little comparisons and applications are shown in figure 2. It is also summarized in table 1. Among various ADC architectures, the pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. Therefore, it is used extensively in high-quality video systems, high speed data acquisition systems and high performance digital communication systems where both precision and speed are critical.

Table 1. Comparisons of ADC Architectures

Architecture	Latency	Speed	Area
Flash	No	High	High
Folding/interpolating	No	Medium-High	Medium-High
Delta-Sigma	Yes	Low	Medium
SAR	Yes	Low	Low
Pipeline	Yes	Medium	Medium

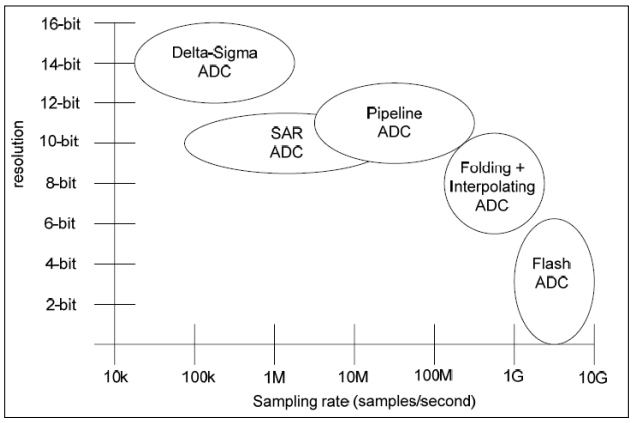

Figure 2. Various ADC Architectures

The state-of-the-art pipelined ADCs has exceeded 100 MSPS(mega-samples-per-second) in CMOS technology , the commonly achieved resolution is still bound within the range of 8-12 effective-number-of-bits (ENOBs) due to the limitations set by component mismatches and finite Op-Amp gain. The steep rise in the demand of compact devices has revolute the world. To reconstruct the exact signals in high quality better converters are needed. Apart from the problem of technology scaling and reduced supply voltages, another important aspect of use of ADCs are converting analog signals in the digital to store them for the future use.

As the nomenclature implies, Flash ADC conversion is the fastest possible way to quantize an analog signal. The concept of this architecture is relatively simple to understand. In order to achieve N-bit from a flash ADC, it requires 2^N-1 comparators, 2^N-1 reference levels and digital encoding circuits. The reference levels of comparators are usually generated by a resistor string. One example of simple flash ADC is shown in Figure 3. First, the analog input signal is sampled by comparators and is compared with one of the reference levels. Then, each comparator produces an output based on whether the sampled input signal is larger or smaller than the reference level. The comparators generate the digital output as a thermometer code. This thermometer code output is usually converted to a binary or a gray digital code by encoding logic circuits at the end. Since this operation is done in one clock cycle, a flash ADC can attain the highest conversion rate as discussed in [11]. The high sensitivity of the comparator offset and a large circuit area are the main drawbacks of a flash ADC. For instance, to build a 10-bit ADC based on flash architecture requires more than 1,023 comparators. Therefore, it will occupy a very large chip area and dissipate high power. Moreover, each comparator must have an offset voltage smaller than 1/2^10 , which is quite difficult to build. That is why we seldom see flash architecture with ADCs of more than 8-bits.

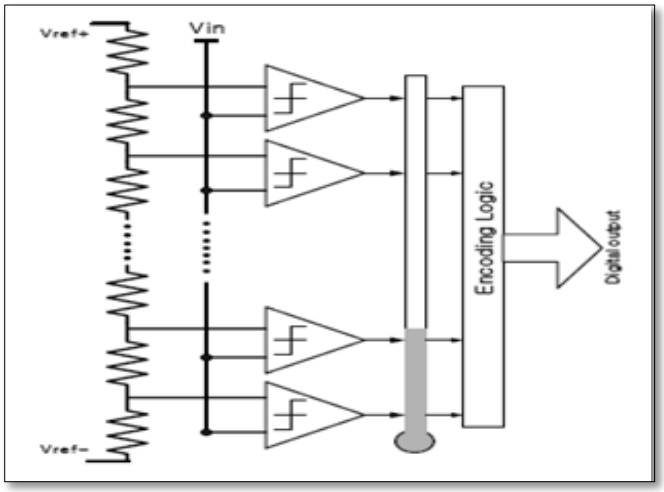

Figure 3. Flash ADC Architecture

The block diagram of a two-step Flash ADC is shown in Figure 4. It consists of a Sample and Hold Amplifier (SHA), two low-resolution flash ADCs, a digital-to-analog (DAC), a subtractor and a gain block. The conversion is executed in two-steps as the name implies. The sampled analog signal is digitized by the first coarse quantizer producing the B1 Most Significant Bits (MSBs). This digital code is changed back to an analog signal by the DAC and subtracted from the sampled input signal producing the residue signal. The residue signal is amplified by the gain block and digitized by the second quantizer producing the B2 LSBs. Because 1-bit out of the output digital codes is often used for error correction, the overall resolution is (B1+B2-1) bit.

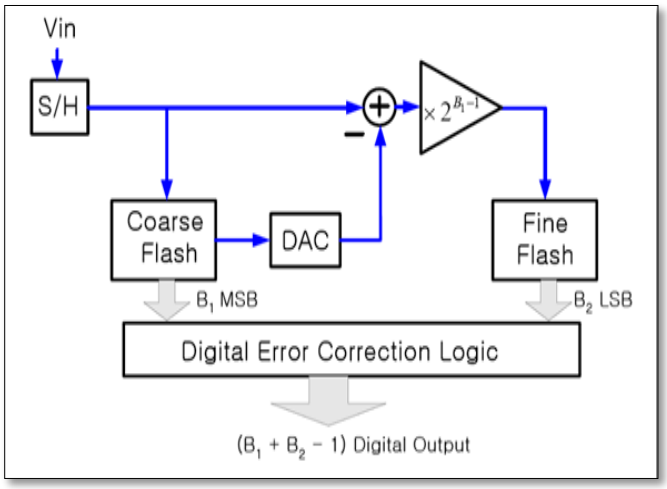

Figure 4. Two-step Flash ADC Architecture

In a sub ranging architecture, the fine quantizer must have full resolution accuracy while the coarse quantizer can have a much more relaxed accuracy requirement. In the two-step flash architecture, both quantizers can have relaxed accuracy requirement because the gain block amplifies the residue signal to the full input scale. The major drawback of the two-step ADC is that the DAC must have an accuracy of the entire resolution of the ADC. The DAC needs time to settle to the required accuracy and will limit the conversion speed of the ADC.

1. Existing Architectures of ADC Architecture

A folding ADC can have a high-speed conversion rate because it uses the parallelism of the flash ADC but uses fewer comparators and less power dissipation than a conventional flash ADC. This performance is achieved by adapting analog preprocessing. A typical block diagram of a folding ADC is shown in Figure 5. The analog preprocessor, in front of the fine quantizer, consists of folding amplifiers that generate the folded signals. The folded signal is like the residue signal in a sub ranging ADC, except for the fact that the residue signal is not generated from the output results of the coarse quantizer. A high conversion rate is achieved because the coarse and fine quantizers are in parallel. The open-loop design of the folding amplifiers also speeds up the converter. Ideally, an analog preprocessor should generate a saw-tooth waveform, but this is difficult to implement. Instead, a triangle waveform is used in actual implementation, but sharp corners remain difficult to realize. The actual waveform is more sinusoidal and causes nonlinearity errors in the ADC.

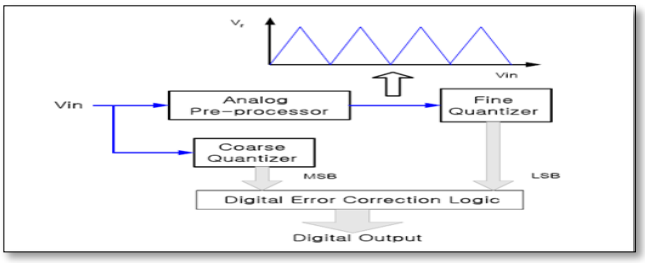

Figure 5. Folding ADC Architecture

In order to overcome such drawbacks as hardware complexity, large chip area and high power

dissipation, sub-ranging architecture was developed at the cost of the sampling speed. A simplified sub-ranging ADC is illustrated in Figure 6. It comprises a SHA, reference level generators, comparators and decoders. The number of comparators is 2^N/M where N is the total ADC resolution, and M is the number of stages. For a 2- stage 10-bit sub-ranging ADC, only 64 comparators are required instead of the 1,024 comparators in a flash ADC. Therefore, compared with a flash ADC, sub-ranging architecture yields a quite significant reduction in power consumption and in the required circuit area. However, the conversion in sub-ranging architecture is done by multiple clocks instead of one clock as in a flash ADC. The operation of the 2-stage sub-ranging ADC is as follows: In the first clock, an analog input signal is sampled by the SHA and quantized by a coarse flash ADC that determines the most significant bit from the sampled input signal. In the next clock, the segment of the resistor string is selected by the results from the coarse flash ADC, and the least significant bits are produced by the fine flash ADC. The comparator requirement of the coarse flash ADC can be relaxed, but the comparators of the fine flash ADC should be as accurate as the full resolution of the ADC. The conversion speed decreases as the number of sub-ranging stages increase.

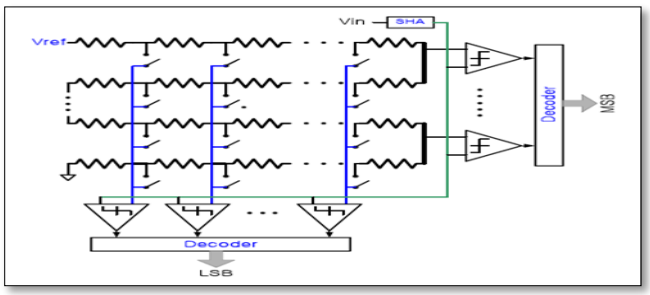

Figure 6. Sub-ranging ADC Architecture

The block diagram of a successive approximation ADC is shown in Figure 7. It consists of a comparator, a DAC and a successive approximation register (SAR). The successive approximation ADC uses a binary search algorithm to find the closest digital code for an input signal. When an input signal is applied to the converter, the comparator simply determines whether the input signal is larger or smaller than the DAC output and produces one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to change the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. In order to achieve N-bit resolutions, a successive approximation ADC requires N clock cycles. Because the performance is limited by DAC linearity, the calibration of the DAC is needed to achieve high resolution.

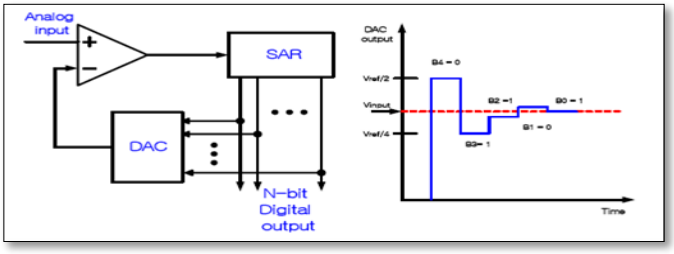

Figure 7. Successive Approximation ADC Architecture

A sigma-delta ADC is also known as an over-sampling data converter. The ADCs seen so far in this chapter are often called as Nyquist rate ADCs because the conversion rate of those ADCs is equal to the Nyquist rate. In sigma-delta ADCs, however, the sampling is performed at a much higher rate than the Nyquist rate. The ratio of the sampling rate to the Nyquist rate is called the over-sampling ratio (OSR). Each doubling OSR allows reducing the quantization noise power resulting in 3dB SNR improvement. A sigma-delta ADC also uses noise-shaping techniques to increase resolution. The quantization noise power is moved to higher frequencies by negative feedback. Then, the out-of-band noise is removed by a digital low pass filter, leaving only a small amount of the quantization noise. The conceptual block diagram is shown in Figure 8. It consists of a SH, a sigma delta modulator, a digital filter and a down sampler. The down sampler converts the over-sampled digital signal into the lower sample rate digital signal. The resolution of the sigma delta ADC can be enhanced

by increasing either the order of the modulator or the resolution of the quantizer. A Lth order sigma delta modulator improves SNR by 6L + 3 dB/octave. However, increasing the order of the modulator more than 2nd can cause instability problems. To avoid instability problem with a high order modulator, a special architecture like multistage noise shaping (MASH) can be employed. Increasing the resolution of the quantizer also cause a problem because of the nonlinearity of the DAC. Dynamic element matching is one of the methods available to reduce the distortion from the multi-bit DAC.

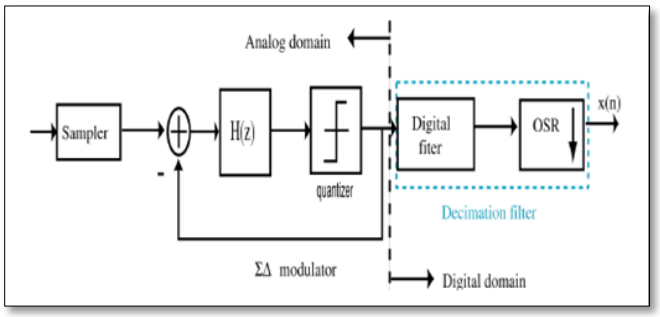

Figure 8. Oversampled ADC Architecture

II. Proposed Analog to Digital Converters (ADCs)

2.1 Pipelined ADC Architecture

Typical pipelined architecture is illustrated in Figure 9. Each stage has the four elements of a SHA, a sub-ADC, a sub-DAC and an inter-stage gain amplifier. The operation of a single stage consists of four steps. First, the input signal is captured by the sample and hold amplifier. Second, this signal is quantized by the sub-ADC, which produces a digital output. Third, this digital signal goes to the sub-DAC which converts it to an analog signal. This analog signal is subtracted from the original sampled signal - thereby, leaving a residual signal. Fourth, this residual signal is increased to the full scale through the inter-stage amplifier. The residual signal is passed to the next stage and the procedure mentioned above is repeated. Since every stage has the element of sample and hold, the above procedure occurs concurrently in every stage. The most interesting feature of a pipeline ADC is the throughput behavior. For a pipeline with m-stages, the very first signal will take m-clock cycles to go through the entire m-stages. Obviously, it will have the latency of m-clock cycles. The next signal - given the nature of the sample and hold element will have the latency of (m-1) clock cycles. After m-clock cycles, we will have a complete digital output in every clock cycle. At this moment, each sampled signal will have the latency of a singular clock cycle. The advantage of a pipeline ADC is that the conversion rate does not depend on the number of stages. The overall speed is determined by the speed of the single stage [13], [14].

In order to reduce the power even more, one can reduce the per-stage resolution and cascade more stages to get the full resolution [16]. One such 1-bit stage architecture is shown in Figure 10. To understand exact operation of this pipeline ADC architecture, let the input signal range vary from 0V to 1V and each stage is of 1-bit resolution. Let the input voltage is 0.7V. So, first this 0.7V is compared with 0.5V by the sub-ADC of first stage.

The output of the first stage will be high logic. Now 0.5v will be subtracted from 0.7V because sub-adc output is high logic. This 0.2 will be amplified with gain 2. So finally, 0.4 V is the output of the first stage, called residue and it serves as input to the next stage. Again this 0.4V is compared by the sub-ADC in the second stage and whole operation is repeated, as shown in Figure 11. The advantage of this architecture is its reduced complexity. With a given per stage resolution, an ADC of a given resolution can be achieved by cascading an appropriate number of identical pipelined stages. The major disadvantage of this architecture is the latency in the converter. Generally, if concurrent/interleaving processing is used, the delay through the converter is roughly clock cycles. From this basic architecture, there are mainly four sub-blocks in each stage: Sample and hold, sub-ADC, sub-DAC and amplifier. In some architecture, sub-DAC and amplifier are grouped in one sub-block and termed as Multiplying DAC (MDAC). Hence

implementation of these building blocks is discussed now onwards.

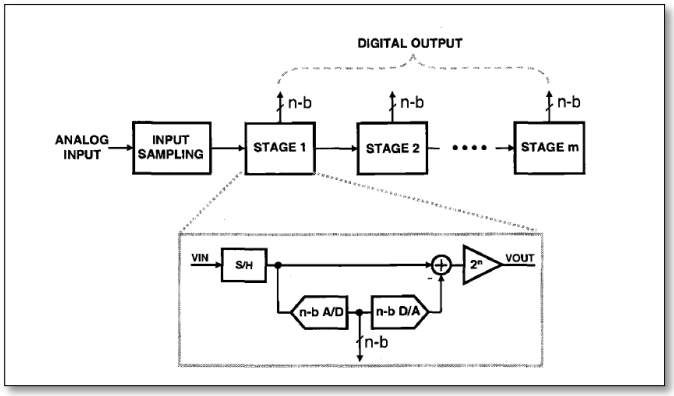

Figure 9. Generalized Pipelined ADC Architecture

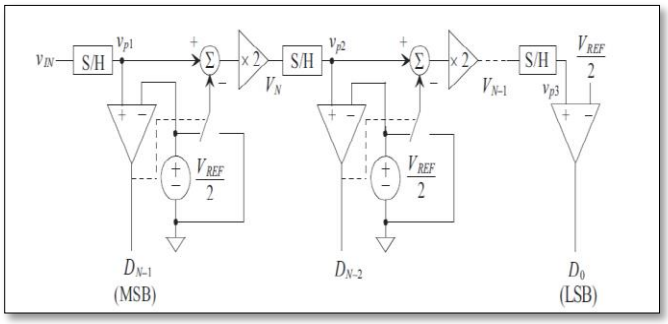

Figure 10. Block Diagram of 3-Stage Pipelined ADC

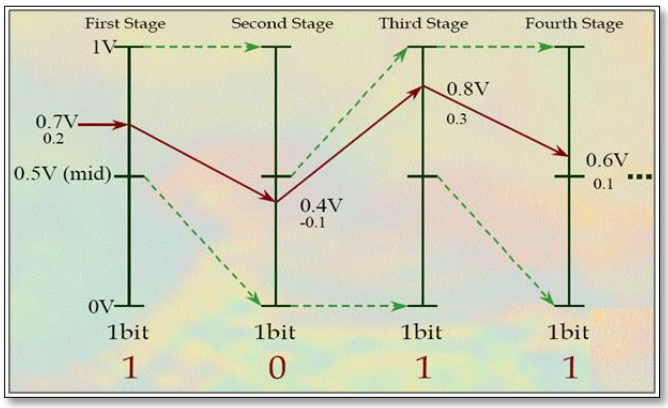

Figure 11. Operation of Pipelined ADC

Process and circuit no idealities like capacitor mismatches, finite amplifier gain (including effects of the parasitic capacitances at the amplifier inputs), amplifier offset, amplifier settling, comparator offset, and charge injection introduce linearity errors in the pipelined ADC. Reference voltage error introduces the shift in the decision level of the ADC; capacitance mismatch produces a digital-to-analog converter (DAC) error [10]. Charge injection, amplifier settling error produce gain error. There is a vertical shift in the residue plot either in the upward or downward direction with respect to +VREF or -VREF due to these errors is as shown in Figure 12. [16].

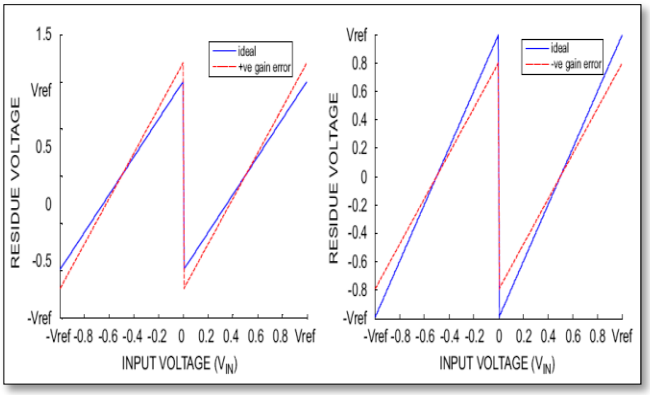

Figure 12. Gain Errors in Residue Plot of Pipelined ADC

2.2 1-Bit Stage using MDAC Architecture

In this implementation each stage can be divided in two sub-blocks, sub-ADC (using comparator or ash ADC) and MDAC (consists of OPAMP, switches and capacitors) as shown in Figure 13. This architecture reduces the chip area and power consumption drastically. During the Ø1phase, switch S1 is connected to ground while S2 and S3 are connected to the input. This is sample mode. During Ø2 phases, S1 is opened while S2 is connected to the feedback and S3 is connected to the DAC output. At this time subtraction and amplification will be performed [5]. This residue output will work as input to the next stage which can be given by equation 1[2]. The conversion accuracy thus solely relies on the precisions of the residue signals; the conversion speed, on the other hand, is largely determined by the settling speed of the residue amplifiers [20].

Here output of MDAC is

$$V_{out} = \frac{C_s + C_f}{C_f} V_{in} - \frac{C_s}{C_f} V_{dac} \quad ----(1)$$

If we select $C_s = C_f$, then $V_{out} = 2V_{in} - V_{dac}$

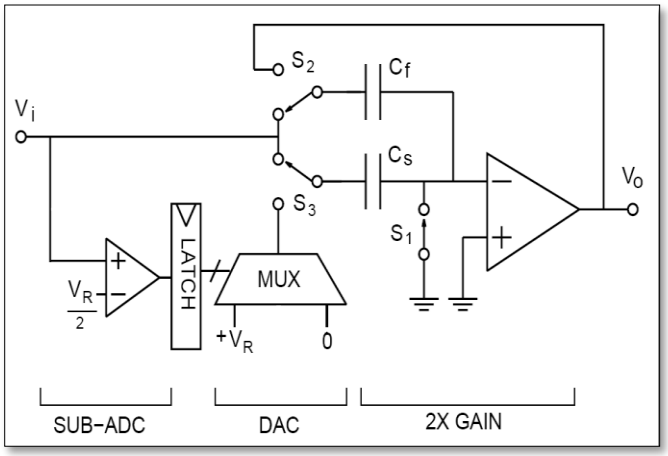

Figure 13. 1-Bit Stage Architecture using MD

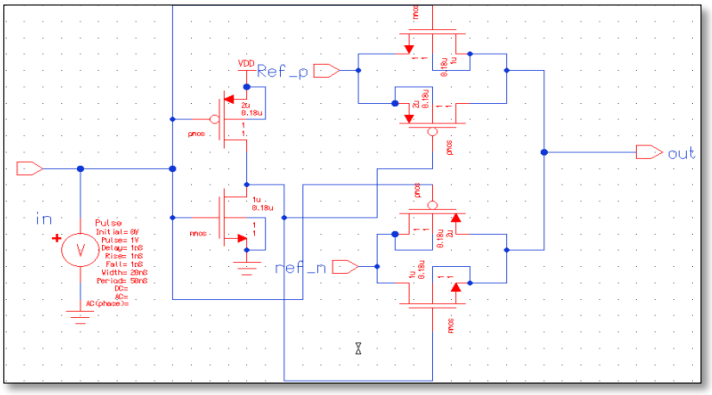

Figure 14. 1-Bit DAC Circuit

III. SIMULATION RESULT

3.1 Simulation Results of 8-Bit Pipelined ADC

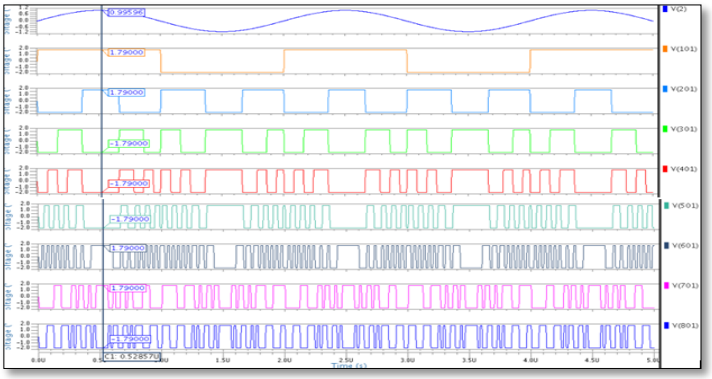

Figure 15. Digital Output of 8-Bit Pipelined ADC using Two Stages OPAMP simulated in 0.18µm Technology

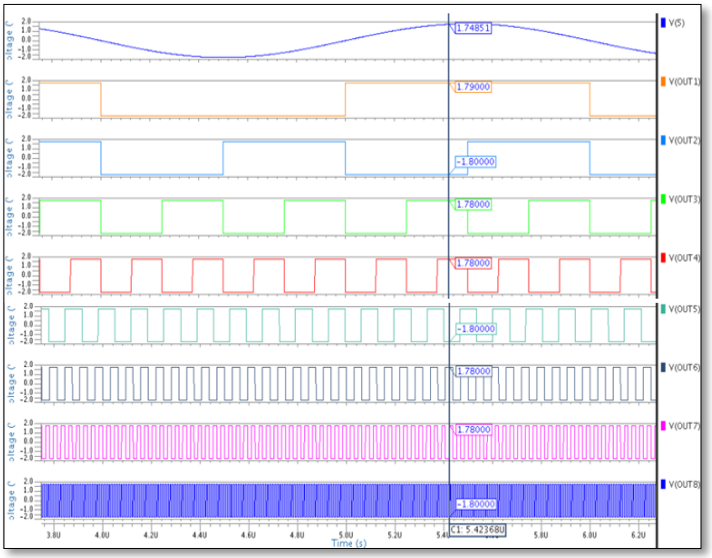

Figure 16. Digital Output of 8-Bit Pipelined ADC using Folded Cascode OPAMP simulated in 0.18µm Technology

2.3 1-Bit DAC

Fig.14 shows the circuit level diagram of 1-bit DAC. As the number of bits is only 1-bit, the corresponding analog output will also have two levels and like the digital output. The present 1-bit digital-to-analog converter has two reference voltages as shown in Fig.14, a positive reference voltage of +VREF and a negative reference voltage of – VREF. Basically the 1-bit DAC can be implemented using simple 2 x 1 analog multiplexer. Here the multiplexer must select Vref/2 Volt or 0 Volt depending on the output of the comparator which acts as a selection line. Here in implementation of 1-bit DAC, two TGs are used as shown in Figure 14. Inputs to these TGs are Vref/2 and ground, while the outputs are connected. Based on the comparator output Vref/2 or zero voltage is available at the output of DAC. The control signals for TGs are comparator output and its inverted output obtained by an inverter. There are two cases:

Case 1: If the comparator output is '1', then DAC output is Vref/2 Volt

Case 2: If the comparator output is '0', then DAC output is 0 Volt

In this design analog input to the DAC are 1V and 0V. Based on comparator output (+1.8V or -1.8V) one of the analog inputs will be available at the output. This is clearly observed in Figure 14.

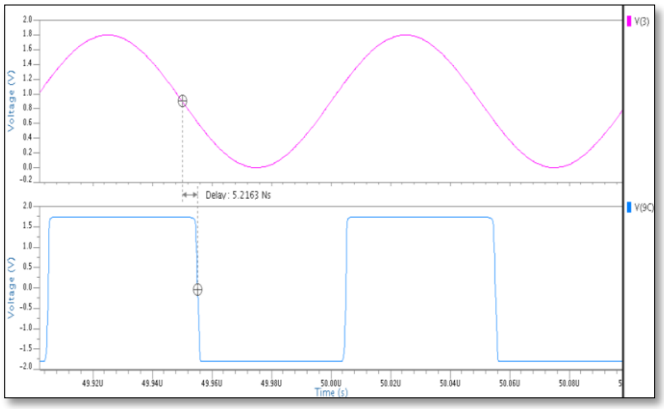

Figure 17. First Stage Comparator Delay of 8 bit Pipelined ADC simulated for 0.18µm Technology

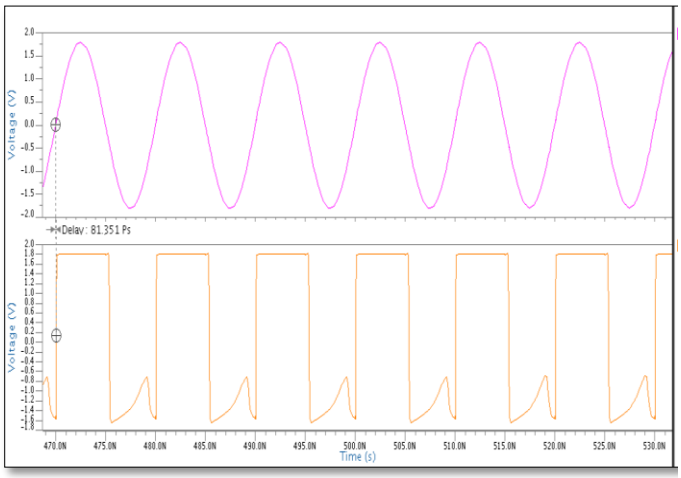

Figure 18. Delay for the First Stage Dynamic Charge Sharing Comparator for 8- Bit Pipelined ADC simulated for 0.18µm Technology

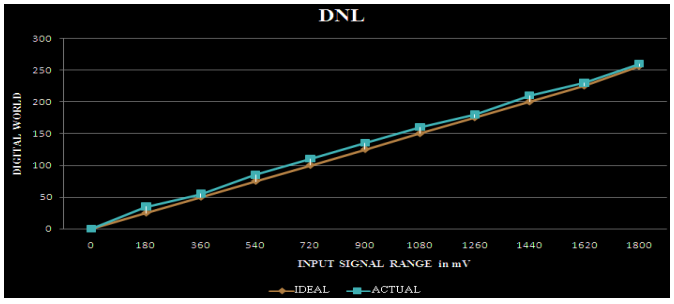

Figure 19. DNL Errors for the 8-Bit Pipelined ADC with OPAMP as a Comparator

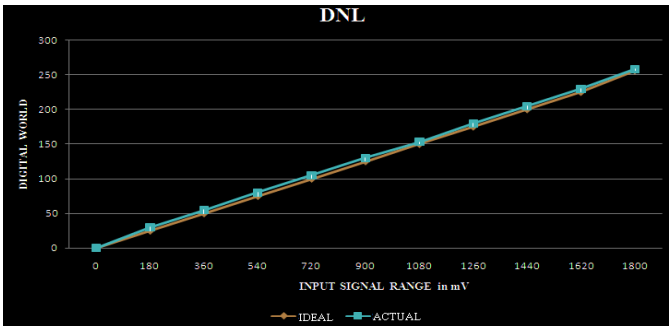

Figure 20. DNL Errors of 8-Bit Pipelined ADC with Dynamic Charge Sharing Comparator

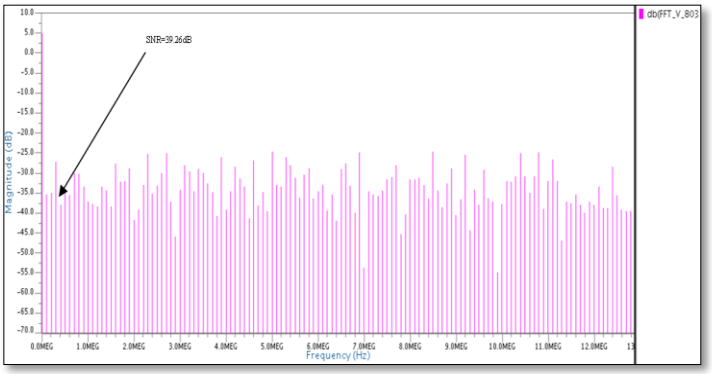

Figure 21. SNR plot of the 8-Bit Pipelined ADC with the SNR value of 39.26 dB

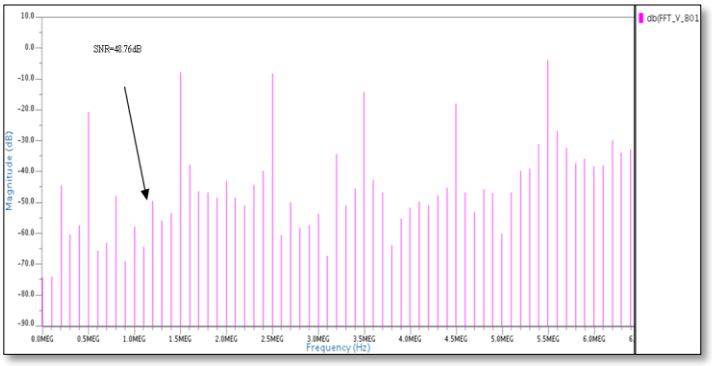

Figure 22. SNR plot of the 8-Bit Pipelined ADC with the SNR value of 48.76 dB

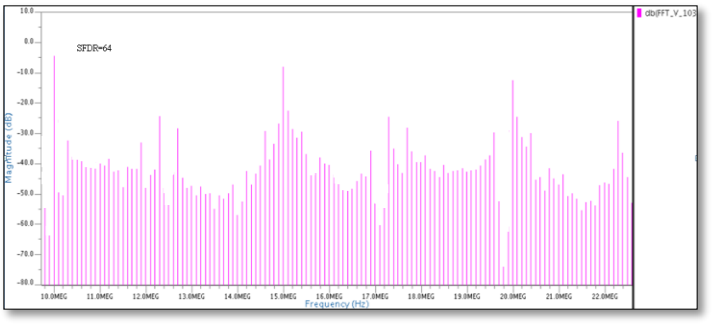

Figure 23. SFDR Plot of 8-Bit Pipelined ADC with the SFDR value of 64dB

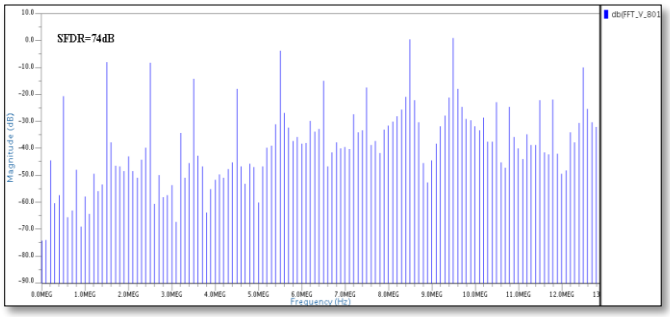

Figure 24. SFDR Plot of 8-Bit Pipelined ADC with the SFDR value of 74dB

Simulation Results of 8 Bit 200MSPS Pipelined ADC

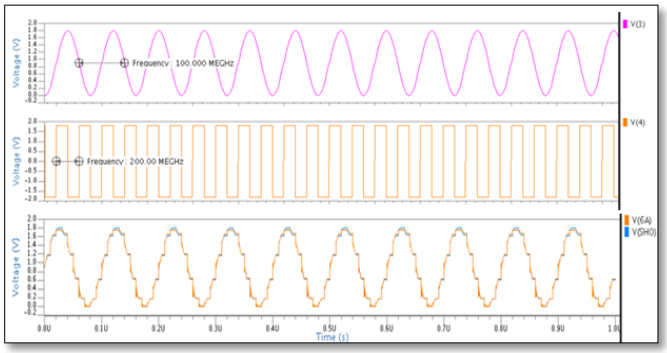

Figure 25. Sample and Hold in 8 Bit 200MSPS Pipelined ADC using 0.18µm Technology

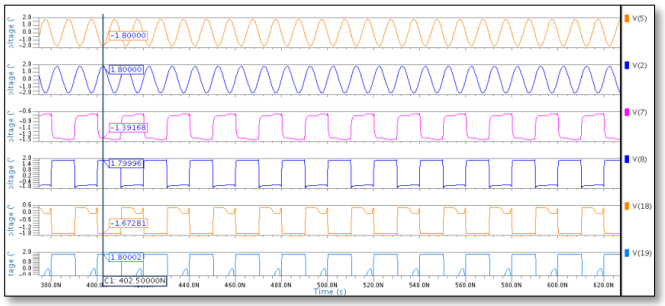

Figure 26. Dynamic Charge Sharing Comparator in 0.18µm Technology

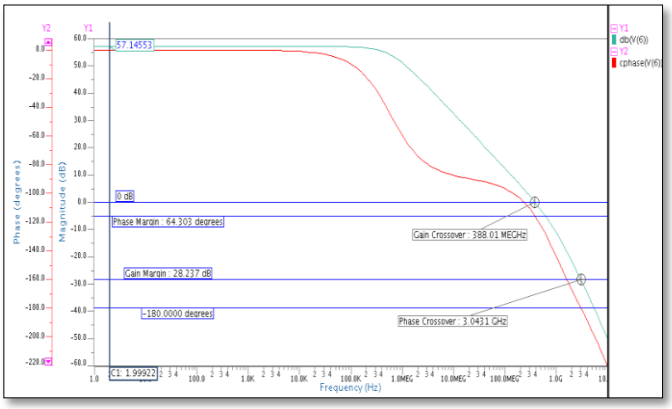

Figure 27. AC Analysis of Dynamic Charge Sharing Comparator in 0.18µm Technology

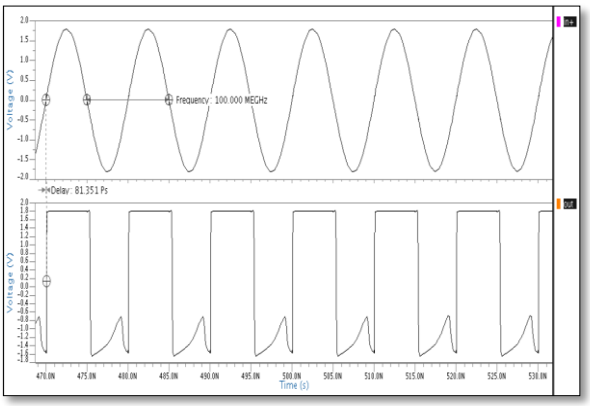

Figure 28. Output of Dynamic Charge Sharing Comparator in 0.18µm Technology

Table 2. Power analysis of Two Topologies

Topologies	Power Dissipation
8 Bits 100MS/s	82mW
8 Bits 200MS/s	56mW

Table 3. Speed Analysis of Two Topologies

Topologies	Power Dissipation
OPAMP as a Comparator	100MS/s
Dynamic Charge sharing Comparator	200MS/s

Table 4. Comparison of Two Topologies

Parameters	8 Bits 100Ms/s	8 Bits 200Ms/s
Power Dissipation	82mW	56mW
Speed	100MS/s	200MS/s
DNL	0.5LSB	0.3LSB
SNR	39.26dB	48.76dB
SFDR	64dB	74dB
ENOB	7.56dB	7.8dB

IV. CONCLUSION

In this paper, development of high performance pipelined ADC with few implementations of the key building blocks such as sample and hold, comparator, switch, amplifier is discussed. 8-Bit 100MSPS and 8-Bit 200MSPS low power pipelined ADC is designed in TSMC 0.18 μm digital CMOS process. This is based on one bit stage using DAC architecture. This design is supported by necessary simulation results of selected building blocks and whole ADC. The main block - amplifier is characterized by gain, phase margin, settling time and power dissipation. The designed pipelined ADC can be characterized by INL, DNL SNR and SFDR. With reference to that effect of stage resolution and Op-Amp topology on power is observed by modification in the designed pipelined ADC. For example, to reduce the area, lower stage resolution is preferred while to reduce power if power of amplifier is larger than the comparator than lower stage resolution is preferred. While for higher accuracy higher resolution is used.

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