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Design and Analysis of High Gain Quasi Y - Source Impedance Network

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ABSTRACT

In this paper, performance of a high gain quasi Y-source impedance network converter is analysed. This converter has a high voltage gain while using a small duty ratio. Compared to other impedance source converters, Y-source converter operates with lower shoot-through duty cycle for the same boosting gain. To achieve that, a three windings transformer with very low leakage inductance is employed. In turn, the switching losses and heating are low at the same boosting gain. Moreover, in this type of converter, the boosting gain depends on number of variables, and hence more degrees of freedom for meeting design constraints. The voltage and current of the switching elements are analysed during shoot and non-shoot through. The analysis shows that for high boosting gain some components have high voltage stress compared to conventional converters. Moreover, fast switching diodes are required to achieve high boosting gain. The performance of the proposed converter is analysed using numerical simulation and experimental testing.

Keywords: DC/DC Converter- High Gain Boosting Converter- Impedance Network, Y-Source Converter.

I. INTRODUCTION

In this paper, the quasi Y source impedance converter performance is analysed. Mathematical model and boosting gain equations are derived during the two operating states. The stress across different elements of the converter is analysed. Finally, the capability of the proposed converter has been demonstrated by numerical simulation using MATLAB/Sim-Power system package and it has been proven using experimental testing.

In spite of several advantages of the conventional voltage/current source inverter, the limited ac output voltage/current and dead time are its main drawbacks. The conventional DC/AC converters are generally buck converter type and cannot operate with low variable DC sources like renewable energy sources. In addition, to avoid short circuits across the DC source, dead time compensation algorithm is required which increases the total harmonic distortion of the output voltage/current converters using coupled inductors increases its power densities. Coupled inductors are different from high-frequency transformers since their magnetizing inductances are designed to be finite. Z-source converter, quasi Z-converter, embedded Z-converter and series Z-converter use two inductors and two capacitors for increasing the converter gain. However, the boosting gain of these types is still lows. To overcome this problem, different types are developed, i.e., switched inductor, tapped-inductor, cascaded, T source, Trans-Z-source, Γ-source and T Z source networks.

Recently, new type source impedance called Y-source converter is proposed. In this type, three winding coupled inductor is designed for deciding different gain values, which is presently not matched by related converters. For simplicity, the number of components used is kept small to allow the converter to be implemented compactly without compromising its performance. However, the conventional Y-source converter has some drawbacks such as discontinuous input current. Discontinuous input current made the Y-source converter unsuitable for renewable energy applications. A quasi Y converter with input inductor has been designed to overcome this problem.

II. MATHEMATICAL MODEL OF QUASI Y-CONVERTER

Figure 1 shows he configuration of the quasi Y-source impedance network. As shown in the figure, the converter consists of a three-winding transformer (N_1, N_2, and N_3), switch SW (MOSFET or IGBT), two diodes D_1 and D_2, input inductor L_{in}, and two capacitors C_1 and C_2. For minimum leakage inductances, the transformer is tied directly to SW and D_1. High leakage inductance of the transformer windings may reduce the converter gain. When supplying an inductive load, the converter may experience voltage spikes.

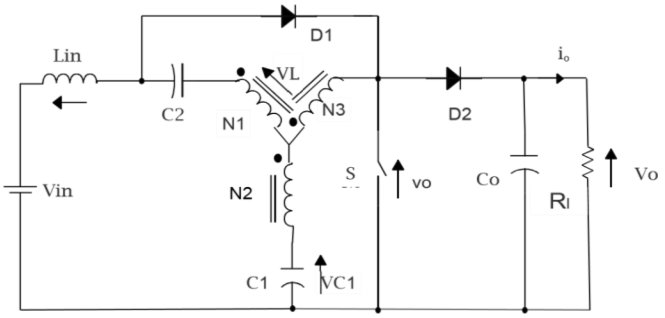


Fig.1 configuration of the quasi Y-source impedance network.

Figure 1.b and 1.c represent the equivalent circuit the quasi Y-source impedance network when it is in two different operating states (shoot and non-shoot through states). The capacitor Co supplies the load with power while C_1 and the source supply the magnetizing current to the transformer. Figure 1.b shows a shoot through (SW turned on) equivalent circuit where the switch SW is turned on while D_1 and D_2 are reversed biased. The source supplies the magnetizing current of the transformer, where C_1 and C_2 reduce biased magnetic core saturation. Figure 1.c shows a non-shoot through (SW turned off) equivalent circuit where the switch SW is turned off with D_1 and D_2 are forward biased. The source supplies the load and recharges the output capacitor Co through D_1 and D_2.

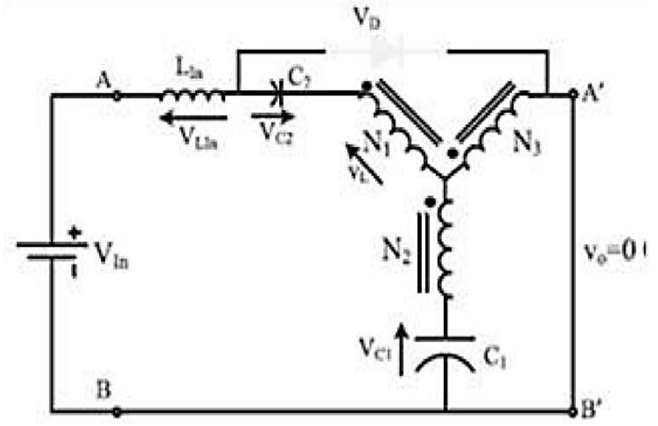


Fig.1 (b) equivalent circuit the quasi Y-source impedance network in shoot state.

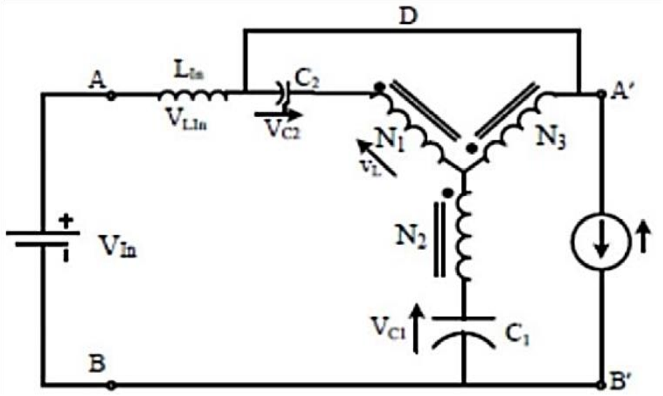


Fig.1 (c) equivalent circuit the quasi Y-source impedance network in non-shoot state.

During shoot-through, the SW is turned on with D1 reversebiased naturally like in Fig. 1(a). Relevant circuit expressions for this state can then be written as

$$V_{C1} + \frac{N_2-N_3}{N_1}V_L = 0 \qquad (1)$$

$$V_{In} - v_{LIn} + V_{C2} - (1 + \frac{N_2}{N_1})\, v_L - V_{C1} = 0 \qquad (2)$$

From (2), the input inductor voltage equation can be written as

$$v_{LIn} = v_{LIn} + V_{C2} - V_{C1} - \frac{N_1-N_2}{N_1}V_L = 0 \qquad (3)$$

Where N_1, N_2 and N_3 are the winding turns of the coupled inductor (three winding transformer).

During the non-shoot-through state, the SW is turned off and D_1 is turned on. The equivalent circuit is shown in Fig. 1(b).

The voltage equations for this case can be written as follows:

$$V_{C2} + \frac{N_1+N_3}{N_1}V_L = 0 \quad (4)$$

$$v_{Lln} = v_{ln}+V_{C2}-V_{C1} - \frac{N_1+N_2}{N_1}V_L = 0 \quad (5)$$

$$v_O = V_{C1}-V_{C2} + \frac{N_1+N_2}{N_1}V_L = 0 \quad (6)$$

Based on volt-sec balance of the inductor, using (1) and (4) results in (7) and using (2) and (5) results in (8):

$$\left(\frac{-N_1}{N_2-N_3}V_{C1}\right)d_{st} + \left(\frac{N_1}{N_1+N_3}V_{C2}\right)(1-d_{st})=0 \quad (7)$$

$$\left(v_{ln}+V_{C2}-V_{C1} - \frac{N_1+N_3}{N_1}V_L\right)d_{st}+\left(v_{Lln}+V_{C2}-V_{C1} - \frac{N_1-N_2}{N_1}V_L\right)(1-d_{st})= 0 \quad (8)$$

Where d_{ST} represents the duty ratio of the switch for introducing the shoot-through state. Using (7) and (8), the capacitor voltages can be derived as:

$$V_{C1}= \frac{(1-d_{st})V_{ln}}{1-\frac{n_{12}}{n_{23}}d_{st}} \quad (9)$$

$$V_{C2}= \frac{\left(\frac{n_{13}}{n_{23}}d_{st}\right)V_{ln}}{1-\frac{n_{12}}{n_{23}}d_{st}} \quad (10)$$

Where $n_{13}=N_1+N_3$ and $n_{23}=N_2-N_3$

Using (3), (5), (9) and (10), the output voltage of the converter can be given as

$$V_O=V_{C1} - \left(1 +\frac{N_{12}}{N_{13}}\right) V_{C2} \quad (11)$$

$$V_0=\frac{1}{1-\frac{n_{12}}{n_{23}}d_{st}}\left((1 - d_{st}) - \left(\frac{N_{13}-N_{12}}{N_{23}}\right)d_{st}\right)V_{ln} \quad (12)$$

The range of shoot-through state (on state) can be deduced as

$$0 \le d_{st} < \frac{1}{\delta} \text{ and } d_{st}^{max} = \frac{1}{\delta}$$

As shown in (12), the boosting gain the quasi Y-converter depends on the three winding number (N_1, N_2, N_3) and the duty ratio (d_{st}). Examples of the gain of (13) and its related turn's ratio are given in Table 1.

For the same shoot-through state period, the boosting gain of the quasi Y-converter is larger than that of the Z-converter and conventional boost converter. The voltage across D_1 and D_2 during the shoot through state can be expressed as:

$$V_D=V_{ln}-v_{Lln} \quad (13)$$

$$V_{D2}=-V_O \quad (14)$$

It is shown that the voltage drop across D_1 during shoot through is very high. The voltage across SW during the non-shoot through state can be expressed as:

$$V_{SW}=-V_O \quad (15)$$

Assuming lossless converter, the input current of the converter can be expressed as

$$I_{Lln}=\frac{1}{1-\delta d_{st}}I_O \quad (16)$$

The inverter output voltage equals

$$V_{inv}= \frac{BWV_{ln}}{2} \quad (17)$$

Where M is the modulation index.

During shoot through period ($t_{sh} = d_{st}T_s$), the capacitor C_1voltage equation can be written as

$$\Delta V_{c1}=\frac{I_O\delta d_{st}^2}{f_sC_1(1-\delta d_{st}}=\frac{V_OK_2d_{st}^2}{f_sC_1R_L(1-\delta d_{st})} \quad (18)$$

Based on (19), the value of C_1 can be determined by the permitted voltage ripple (ΔV).

Also, the voltage across C_2 during shoot through period can be expressed as

$$\Delta V_{c2}=\frac{I_Od_{st}T_s}{C_2(1-\delta d_{st}}=\frac{V_Od_{st}}{f_sC_2R_L(1-\delta d_{st})} \quad (19)$$

Based on (19), the value of C_2 can be determined by the permitted voltage ripple (ΔV_{C2}).

For the same voltage ripple percentage ($\Delta V_{c1} = \Delta V_{c2}$) , the relation between the two capacitance can be deduced as

$$C_1=\delta d_{st} C_2 \tag{20}$$

During non-shoot through period ($t_{n\_sh}=(1-d_{st})T_s$), the voltage across the input inductor equals.

$$V_{LIn}=V_{In}-V_O=L_{IN}\frac{\Delta I_{LIN}}{T_s(1-\delta d_{st})} \tag{21}$$

$$L_{Lin}=\frac{(1-\delta)\delta K_2 V_O}{f_s \Delta I_{LIN}} \tag{22}$$

Based on (22), the value of L_{LIN} can be determined by the permitted current ripple (ΔI).

TABLE-I GAIN OF QUASI Y-SOURCE BOOST DC-DC CONVERTER WITH DIFFERENT WINDING FACTOR AND TURNS RATIO (N_1:N_2:N_3)

(N1:N2:N3)		**Gain**
(1:3:1),(1,5,2),(2:4:1),(3:5:1)	2	$(1-2d_{st})^{-1}$
(1:5:3),(2:4:2),(3:3:1),(1:2:1)	3	$(1-3d_{st})^{-1}$
(1:3:2),(2:2:1),(5:3:1),(4:4:2)	4	$(1-4d_{st})^{-1}$
(3:2:1),(5:5:3),(6:4:2),(1:3:4),(7:3:1),	5	$(1-5d_{st})^{-1}$
(4:2:1),(3:3:2),(2:4:3),(1:5:4), (6:6:4)	6	$(1-6d_{st})^{-1}$
(5:2:1),(4:3:2),(3:4:3),(2:5:4),(1:6:5)	7	$(1-7d_{st})^{-1}$
(6:2:1),(5:3:2),(4:4:3),(3:5:4), (2:6:5)	8	$(1-8d_{st})^{-1}$
(7:2:1),(6:3:2),(5:4:3),(4:5:4),(3:6:5)	9	$(1-9d_{st})^{-1}$
(8:2:1),(7:3:2),(6:4:3),(5:5:4),(4:6:5)	10	$(1-10d_{st})^{-1}$

III. RESULTS

To evaluate the performance of the proposed quasi Y converter, simulations are carried out using MATLAB/SimPower system Package. Figure 2 shows the simulation block diagram of the proposed converter. Table II contains the values of the converter components and parameters used in simulation and experimental work. The turns ratio of the transformer (N_1:N_2: N_3) is 45:30:15 then δ =5. The input voltage is 50V and the shoot through period is 15%. The boosting gain is B = 4 and the output voltage is nearly 200V. The simulation waveforms are shown in Fig. 2 and 3.

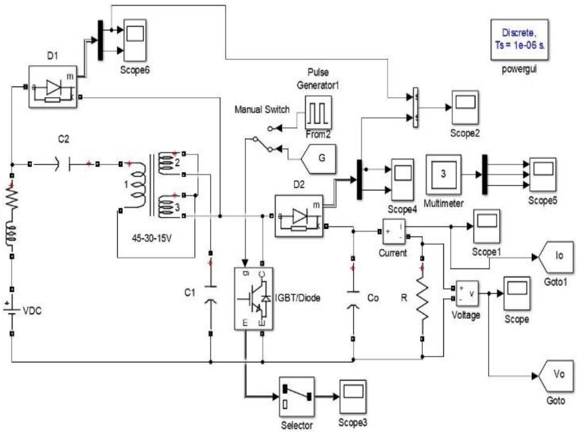
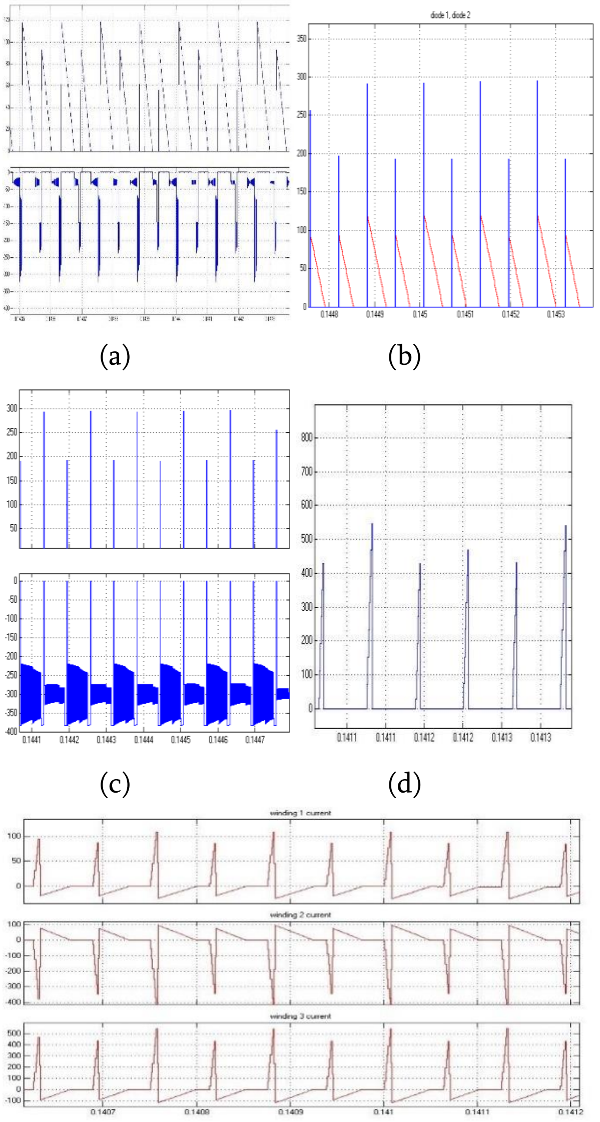


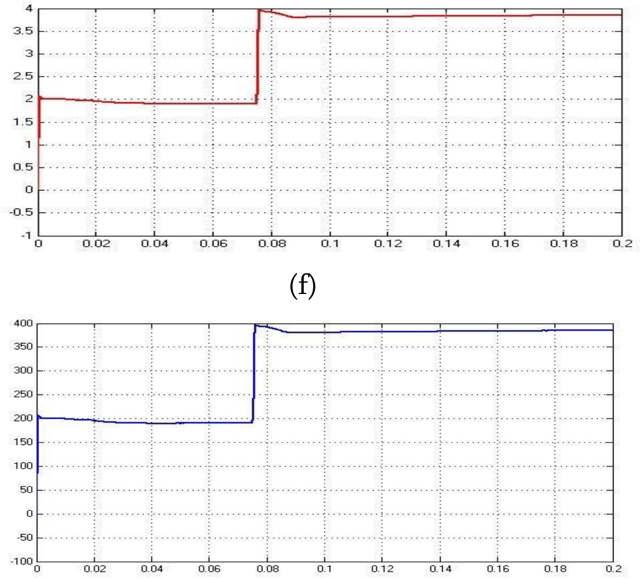
Fig. 2. Simulation block diagram of the Quasi Y-converter.



(a) (b)

(c) (d)

(e)



(f)

(g)

Fig.3 Waveform of simulation model (a) input current diode d1 voltage

(b) d_1d_2 current (c) d_1d_2 voltage. (d) Switching voltage. (e) Winding current (f) output current (g) output voltage.

As shown in the figure, the input current (I_{in}) is continuous and its average value is about 6A. During shoot through state, the transformer draws the magnetizing current and the capacitor C_1 charges, so the input inductor current increases. Figure 3.c shows that the voltage across D_1 is high ($4V_o$) during non-shoot through which mains high stress on this element while the voltage across the switch SW equals output voltage as shown in Fig.3(d). Figure 4 shows current waveforms of the transformer winding and diodes. Figure 4.a shows the current through winding N1 centred along the horizontal zero-axis. This is expected because of the dc-blocking capacitor C2 connected in series with N_1. Windings $N_2$and N_3 discharge their storage energies through D_2 to C_o and R_{load} while winding N1 discharge its storage energy through diodes D1 then D2. So, diode D_2 conducts, as seen in Fig. 4.d, from its zero voltage when $\Delta \neq 0$. The discharging of N_2 and N_3 (or charging of C_O) ends only when current through D_2 falls to zero, at which Δ also falls to zero and a reverse voltage begins to appear across D_2.

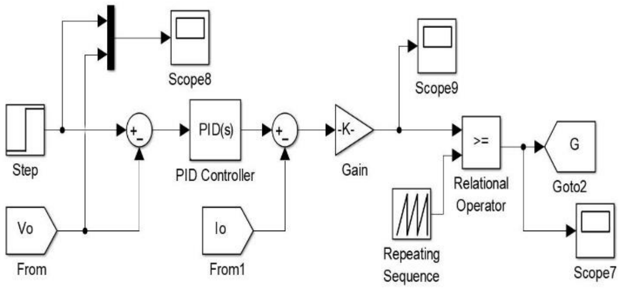
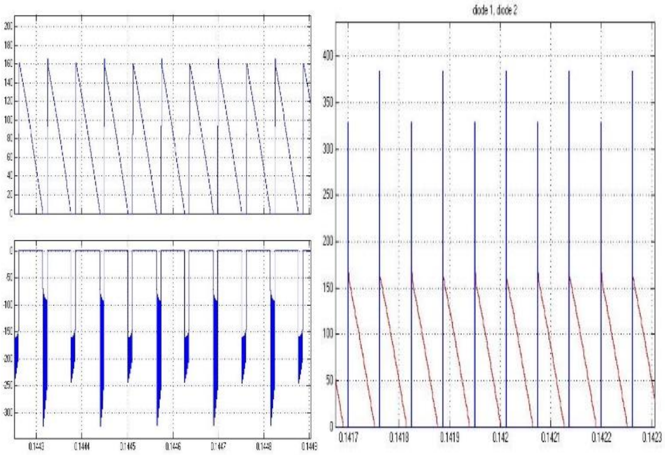
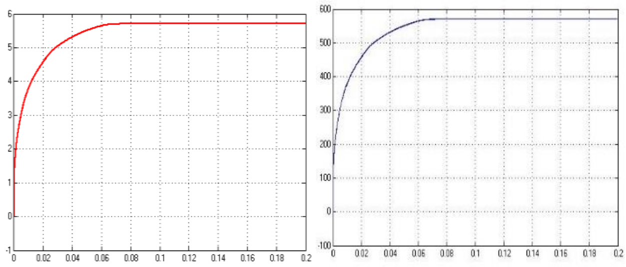


Fig.4 Simulation block diagram of control loop



(i)Control loop input current (ii) control loop D_1D_2 current



(iii) Output current control loop (iv) Output voltage control loop.

Component/Parameter	Value
Capacitor C1	470 µF/400V
Capacitor C2	150 µF/400V
Output capacitor C0	470 µF/450V
Input inductor (Lin)	1.5 mH
Switching frequency (Fs)	16 kHz
Shoot-through duty cycle(dst)	15%
Winding factor (δ)	5
Turns ratio (N1 : N2 : N3)	45:30:15

Transformer Core (Ferrite ring core)	TX36/23/10-3E10 core
Switch SW	IGBT HGTG20N60B3D
Diode D1	VS-ETX1506-M3

IV. CONCLUSION

In this paper, the performance of the quasi Y-source is analysed and evaluated. The converter is modelled in the shoot and non-shoot through states. The boosting gain and voltage stress on different components equations are deduced. Quasi Y-converter is modelled using MATLAB/Sim-power system and implemented experimentally. The proposed converter has the following characteristic:

1- High boosting gain with small shoot through state, then the conduction loss of the switch is low.
2- The inrush current of the magnetic core is blocked using DC-blocking capacitors.
3- The input current is continuous and in turn the converter can be employed with renewable energy sources.
4- Easy and simple implementation.

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REFERENCES

[1] Fang ZhengPeng “Z-Source Inverter” IEEE Transactions on Industry Applications, Vol. 39, No. 2, pp. 504- 210, March/April 2003.

[2] Fang Lin Luo, and Hong Ye “Advanced DC/DC Converters” by CRC Press LLC, 2004.

[3] M. K. KAZIMIERCZUK “Pulse-width Modulated DC–DC Power Converters” by John Wiley & Sons, Ltd, 2008.

[4] Y. J. A. Alcazar, D. S. Oliveria, F. L. Tofoli and R. P. TorricoBascope, “DC-DC Nonisolated Boost Converter Based on the Three-State Switching Cell and Voltage Multiplier Cells,” IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4438-4449, Oct. 2013.

[5] J. Anderson and F. Z. Peng, “Four Quasi-Z-Source Inverters,” in Proc. IEEE-PESC’08, Jun. 2008, pp. 2743-2749, Rhodes, Greece.

[6] J. Anderson and F. Z. Peng, “A Class of Quasi-Z-Source Inverters,” in Proc. IEEE-IAS’08, Oct. 2008, pp. 1-7, Edmonton, Alberta, Canada.

[7] P. C. Loh, F. Gao and F. Blaabjerg, “Embedded EZ-Source Inverters,” IEEE Trans. Ind. Applicant., vol. 46, no. 1, pp. 256-267, Jan/Feb. 2010.

[8] Y. Tang, S. Xie and C. Zhang, “An Improved Z-Source Inverter,” IEEE Trans. Power Electron., vol. 26, no. 12, pp. 38653868, Dec. 2011.

[9] M. K. Nguyen, Y. C. Lim and G. B. Cho, “Switched-Inductor Quasi-Z-Source Inverter,” IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3183-3191, Nov. 2011.

[10] M. Zhu, K. Yu and F. L. Luo, “Switched Inductor Z-Source Inverter,” IEEE Trans. Power Electron., vol. 25, no. 8, pp. 21502158, Aug. 2010.

[11] D. Li, P. C. Loh, M. Zhu, F. Gao and F. Blaabjerg, “EnhancedBoost Z-Source Inverters with Alternate-Cascaded Switched- and Tapped-Inductor Cells,” IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3567-3578, Sep. 2013.

[12] D. Li, F. Gao, P. C. Loh, M. Zhu and F. Blaabjerg, “Hybrid source Impedance Networks: Layouts and Generalized Cascading Concepts,” IEEE Trans. Power Electron., vol. 26, no. 7, pp. 20282040, Jul. 2011.

[13] R. Strzelecki, M. Adamowicz, N. Strzelecka and W. Bury, “New Type T-Source Inverter,” in Proc. CPE’09, May 2009, pp. 191195, Badajoz, Spain.

[14] S. P. Kumar and P. Shailaja, “T-Shaped Z-Source Inverter,” Int. Journal Eng. Research & Tech., vol. 1, no. 9, pp. 1-6, Nov. 2012.

[15] W. Qian, F. Z. Peng and H. Cha, “Trans-Z-Source Inverters,” IEEE Trans. Power Electron., Vol. 26, no. 12, pp. 3453-3463, Dec. 2011.

[16] P. C. Loh, D. Li and F. Blaabjerg, “Γ-Z-Source Inverters,” IEEE Trans. Power Electron., Vol. 28, no. 11, pp. 4880-4884, Nov. 2013.

[17] M. K. Nguyen, Y. C. Lim and Y. G. Kim, “T Z-Source Inverters,” IEEE Trans. Ind. Electron., Vol. 60, no. 12, pp. 56865695, Dec. 2013.

[18] M. K. Nguyen, Y. C. Lim and S. J. Park, "Improved Trans Z Source Inverter with Continuous Input Current and Boost Inversion Capability" IEEE Trans. Power Electron., Vol. 28, no. 10, pp. 45004510, Oct. 2013.

[19] Yam P. Siwakoti, Poh Chiang Loh, FredeBlaabjerg, Graham E. Town “Magnetically coupled high-gain Y-source isolated DC/DC converter” IET Power Electron., Vol. 7, Iss. 11, pp. 2817– 2824, 2014.

[20] Yam P. Siwakoti, Poh Chiang Loh, FredeBlaabjerg, and Graham E. Town “Y-Source Impedance Network” IEEE Transactions on Power Electronics, Vol. 29, No. 7, pp. 3250-3256, July 2014.

[21] Yam P. Siwakoti, Poh Chiang Loh, FredeBlaabjerg, SørenJuhlAndreasen and Graham E. Town “Y-Source Boost DC/DC Converter for Distributed Generation” IEEE Transactions on Industrial Electronics, Vol. 62, Iss. 2, pp.1059 – 1069, August 2014.

[22] Yam P. Siwakoti, FredeBlaabjerg, Poh Chiang Loh”QuasiYSource Inverter” 2015 Australasian Universities Power Engineering Conference (AUPEC), 27-30 Sept. 2015, pp. 1-5.

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