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Implementation of High-Performance EEG Based Seizure Detection And Analysis On Multicore Platform

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ABSTRACT

About 50 million people worldwide suffer from epilepsy, the neurological disorder characterized by seizures. The primary tool for diagnosis of an epileptic seizure is an electroencephalography (EEG) which records the brain's spontaneous electrical activity. This requires the placement of a minimum of 16 electrodes on the scalp with each electrode being interpreted as a channel. The classification of seizure detection and analysis techniques mainly work in two stages , where features are extracted from raw EEG data in the first stage and then the obtained features are used as input for the classification process in the second stage. Traditionally the Seizure detection algorithms were implemented using DSP Processor or FPGAs. But these single core platforms are constrained with respect to speed of operation and power consumption. There is a greater need to reduce the power consumption as well to increase the speed of EEG seizure detection system. This problem can be addressed using the Multicore Processors, which process data simultaneously. This project presents a high performance multicore platform for EEG based seizure detection and analysis. This platform performs continuous multichannel detection and analysis of seizures for epilepsy patients. The detection unit detects seizures based on feature extraction process once seizure detection is done enables the analysis circuit that process the data based Uridva Triyabhakyam based 128 point FFT and transmits energy and frequency contents of EEG data. All proposed blocks are simulated and synthesized using Xilinx ISE and coding is done in Verilog.

Keywords : Electroencephalography, FPGA, FFT, Xilinx ISE, Vedic Multiplier

I. INTRODUCTION

So as to meet execution necessities of single center plans were pushed to higher clock speeds, in this manner the power prerequisite developed at a quicker rate than the recurrence. Power issue was exacerbated by plans that endeavored to powerfully extricate additional presentation from the guidance stream, as note that this prompted structures that were intricate, unmanageable, and more power utilization. To meet these prerequisites, chip architects went to multi-center processors. A multi-center processor is one which comprises of numerous number of processors on a solitary chip, every one of these processors work in parallel in this manner the general execution of the multi-center processor increments. Between center correspondence assumes a significant job to adjust the power and execution in a multi-center processor. At the point when certain issue is given to an inserted processor the throughput relies upon both figuring capacity and correspondence proficiency between centers. Conventional single center DSP processors are not appropriate for parallelization though FPGAs are awkward to program. ASICs are the ideal stage regarding territory, speed, and power, however the long advancement time and high assembling expenses are restrictive. A developing zone of intrigue is utilizing many-center stages to cross over any barrier among ASICs and FPGA/DSP processors. This undertaking executed a many-center stage supporting 64 low power adjusted RISC centers with an accentuation on low power and zone. To show a use of Electroencephalogram in the therapeutic stage, the centers are customized to actualize seizure recognition and examination of patient. This task executed with a low power , territory and compact gadget that supports 16 channels of EEG sources of info and performs post recognition seizure examination. Location of seizures is practiced utilizing a low power circuit. To counteract false positives, numerous channels are examined to separate a seizure from irregular spikes in mind action. Endless supply of a seizure, the gadget utilizes the EEG information to perform seizure examination. The information is isolated into various recurrence groups for a nervous system specialist to decide the sort and area of the seizure. To diminish control utilization, ghostly investigation is just performed after the discovery of a seizure.

II. LITERATURE SURVEY

Booth Multiplier

It is a ground-breaking calculation for marked number duplication, which treats both positive and negative numbers consistently .For the standard include move task, every multiplier bit creates one numerous of the multiplicand to be added to the halfway item. On the off chance that the multiplier is enormous, at that point countless multiplicands must be included. For this situation the postponement of multiplier is resolved primarily by the quantity of increases to be performed. On the off chance that there is an approach to decrease the quantity of the increments, the exhibition will show signs of improvement. Stall calculation is a strategy that will decrease the quantity of multiplicand products. For a given scope of numbers to be spoken to, a higher portrayal radix prompts less digits. Since a k-bit parallel number can be deciphered as K/2-digit radix-4 number, a K/3-digit radix-8 number, etc, it can manage more than one piece of the multiplier in each cycle by utilizing high radix augmentation Focal points simple to create dependent on engineering and corner encoder and It is executed for marked and stretched out to genuine numbers, detriments increasingly fractional items, Inefficiency of the calculation when detached one are available, Difficulty in structuring parallel multipliers as no. of move – include tasks may fluctuate.

Vedic Multiplier

Vedic arithmetic is primarily founded on sixteen standards or word-formulae which are named as sutras. This is an exceptionally fascinating field and displays some compelling calculations which Cases Operation 00 0 01 +1 10 - 1 11 0 can be connected to different parts of building, for example, registering and computerized sign handling. Coordinating increase with Vedic Mathematics systems would result in the sparing of computational time . Along these lines, coordinating Vedic arithmetic for the multiplier configuration will improve the speed of duplication task. The multiplier design depends on Urdhva Tiryagbhyam (vertical and across calculation) sutra.

Real highlights are High speed low power multipliers, least deferral and utilized for duplication of a wide range of numbers constraint relies upon explicit applications

III. PROPOSED METHOD

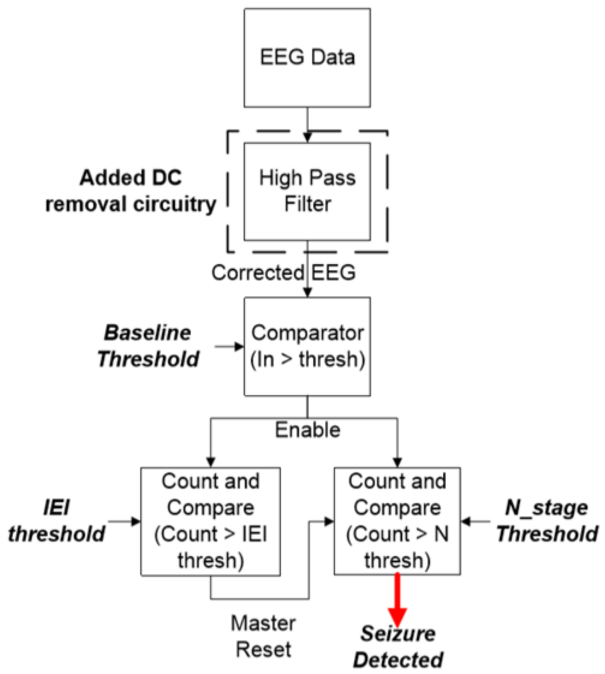

Fig 3.1seizure detection algorithm

Single-divert seizure recognition calculation in fig 3.1 shows how EEG information is processed to get seizure discovery. A 4Hz high pass filter added to expel DC part from approaching EEG signal. At the point when the filtered EEG information outperforms the standard thereshold N times inside the IEI time edge, a seizure is distinguished. Proposed single-channel seizure identification calculation. A 4Hz high pass filter added to expel DC part from approaching EEG signal. At the point when the filtered EEG information outperforms the pattern thereshold N times inside the IEI time limit, a seizure is recognized.

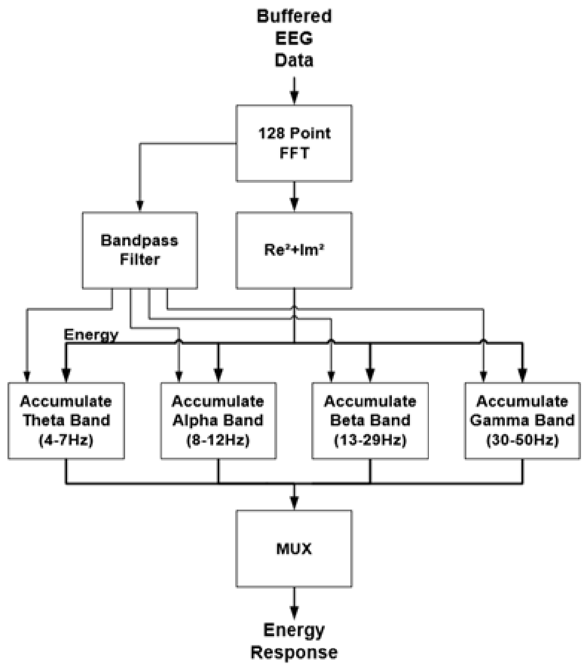

Fig 3.2 Seizure analysis block diagram

Mapping of Seizure Detection and Analysis

To show the usefulness of the many-center stage for fixed point DSP applications, the multi-channel seizure location and investigation is mapped onto the stage. The low power seizure recognition engineering was at first proposed by the creators and more subtleties are found. Delineates the abnormal state square outline of the equipment square. Seizure information is changed over from simple to advanced over the 16 channels and is sequentially passed to the many-center stage. Each channel has its own devoted seizure discovery square which likewise incorporates a 33 tap high pass FIR channel to evacuate any DC balance. The recognition square analyzes information to a preset limit.

Seizure Data Analysis:

Materials The EEG information utilized were a subset of EEG information relating to both ordinary and epileptic subjects, made accessible by Dr. Ralph from the Epilepsy Center at the University of Bonn . Three EEG informational collections from three distinct gatherings were examined: solid subjects with ordinary EEG information, epileptic subjects during a without seizure interim with interictal EEG information, and epileptic subjects during a seizure with ictal (epileptic) EEG information. Every datum set recorded with a 128-channel enhancer framework contained 100 single-channel EEG fragments inspected at 173.61 Hz, every one of 23.6 sec span. These fragments were chosen and cut out from the consistent multi channel EEG accounts after visual review for ancient rarities (for example because of muscle action or eye development). Also, the portions needed to satisfy a stationarity paradigm portrayed in point by point. The principal EEG informational collection relating to sound subjects was taken from the surface EEG chronicles of five solid subjects, who were loose in a stir state, utilizing the institutionalized anode situation system. The second and third informational collections got from five diverse epileptic subjects during a sans seizure and seizure interim, separately, were taken from the intracranial EEG accounts during presurgical determination.

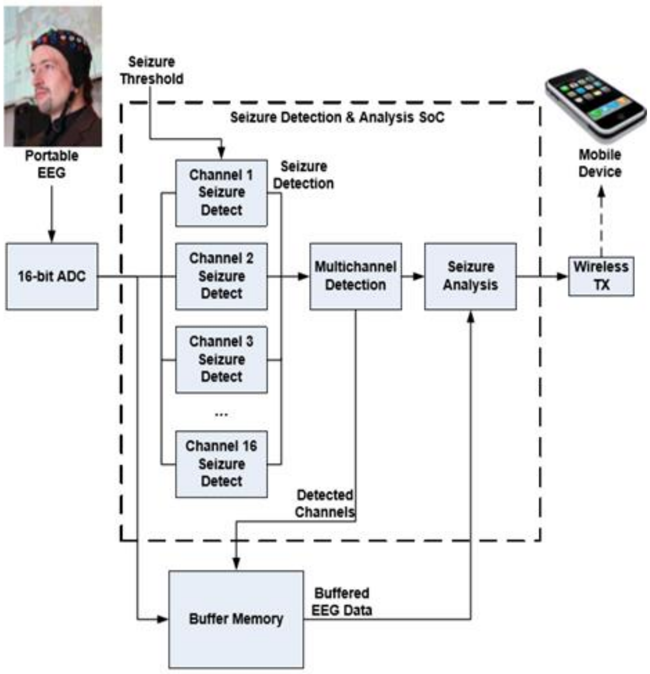

Fig 3.3 Multi-channel seizure detection architecture

IV. RESLTS

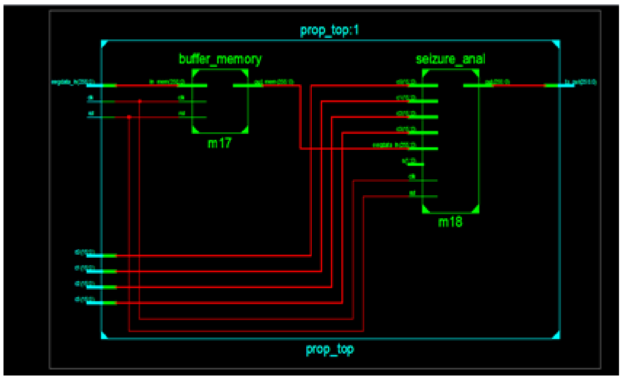

Fig 4.1 RTL Schemetic of Booth Multiplier system

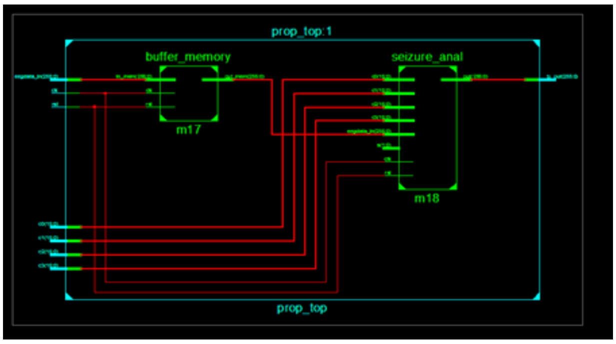

Fig 4.2 RTL Schematic of Vedic Multiplier system

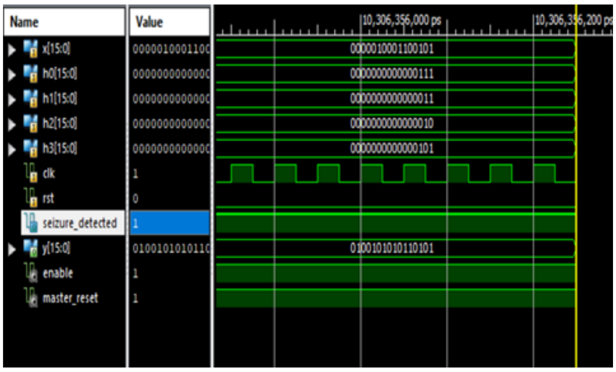

Fig 4.3 Simulation Result of single channel seizure detected system

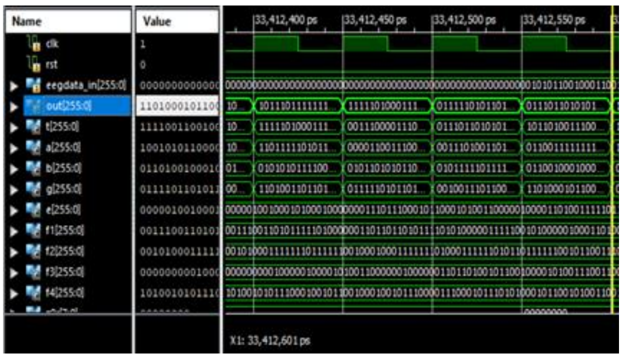

Fig 4.4 Simulation Result of single channel no seizure detected system

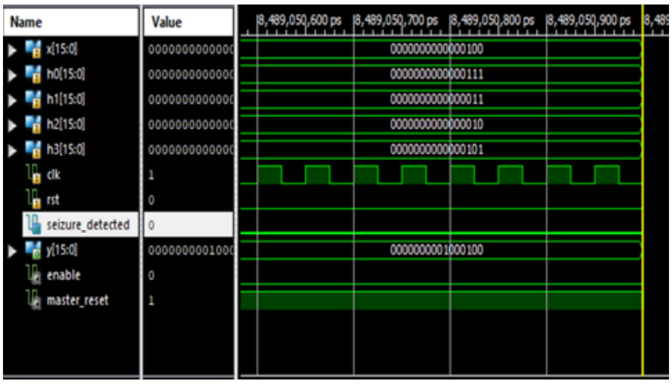

Fig 4.5 Simulation Result of 16 channel seizure detection of Booth based system

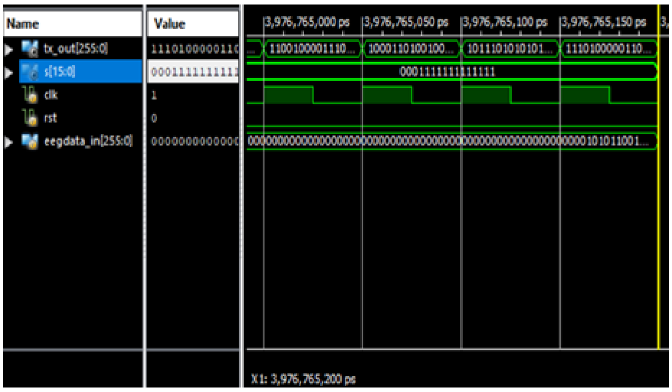

Fig 4.6 Simulation Result for 16 channel seizure detected Modified system

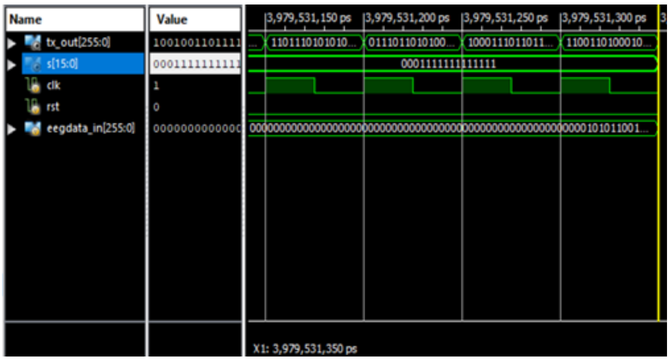

Fig 4.7 Simulation Results for Seizure Analysis of Booth Based System

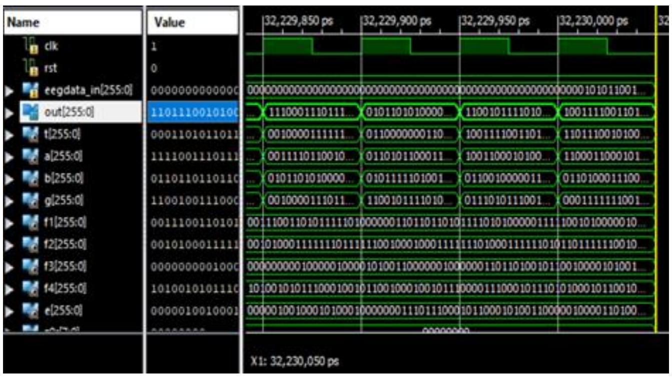

Fig 4.8 Simulation Results for Seizure Analysis of Vedic Based System

Table 4.1 Comparison of slices, LUTS, FF, delay Booth Multiplier and Vedic Multiplier based system along values

Specifications	Booth Multiplier system	Vedic Multiplier system
No of slices	21396	15944
No of LUT's	5296	3280
No of FF	38365	29405
Delay	73.58ns	72.2ns

V. CONCLUSION

This project Implements high performance EEG based seizure detection and analysis on multicore platform. Seizure detection is done in Time domain, where energy parameter is used as seizure detection feature and analysis is done in Frequency domain. Time domain is converted to frequency domain using 128 point FFT. For enhancing the speed of the existing seizure detection and analysis, hardware is implemented by Urdhva Triyakbhyam based Vedic multiplier in the seizure analysis block.

The results obtained show that the 128 point FFT block designed using UT based multiplier reduced areadelay product by 31% when compared to the Booth multiplier based FFT block. This speed enhancement in FFT also improves overall system speed.

VI. FUTURE SCOPE

In Future, project can be extended to implement fixed point signed and floating point numbers data and also the project can be extended by extending its functionality to wider network topology.

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