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An Optimized Three-Phase Multilevel Inverter Topology with Separate Level and Phase Sequence Generation Part

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ABSTRACT

This paper presents an optimized, 3-φ, multilevel inverter (MLI) topology. The proposed system is derived by cascading the level generation part with the phase sequence generation part. Further, it can be operated at any required level depending upon the configuration of the level generation part. Thus, for higher level operation extra components are required at the level generation part only. Therefore, number of components required for the proposed MLI is lower than the conventional 3-φ MLI topologies for higher level operation. Further, the level generation part is shared by the three phases equally. This eliminates the possibility of phase unbalance. The working principle and the operation of the proposed MLI are supported with the simulation and experimental validations. Further, the proposed optimized MLI is also compared with the conventional 3-φ MLIs to prove its advantage.

Keywords : Common Mode Voltage, Multilevel Inverter, Topology, Flying Capacitor.

I. INTRODUCTION

MULTILEVEL inverters consist of a group of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Different topologies and wide variety of control methods have been developed in the recent literature. The most common multilevel inverter configurations are neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB are considered the main drawbacks of these topologies. Apart from these three main topologies, other hybrid multistage topologies are becoming one of the most interested research areas. In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed. On the other hand, for the purpose of improving the performance of the conventional single- and three-phase inverters, different topologies employing different types of bidirectional switches have been suggested. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels. Based on this

technical background, this paper suggests a novel topology for a three phase five-level multilevel inverter.

II. WORKING PRINCIPLE OF PROPOSED TOPOLOGY

The proposed optimized MLI configuration for m-level operation consists of two parts, (i) level generation part (LGP) and (ii) phase sequence generation (PSGP).The LGP is realized using two identical basic units (BUs) connected in series, BUs used in LGP consists of "*n*" number Each subunit/cell again consists of dc voltage source and a pair of complementary switches. Further, it can be observed from Fig. 1

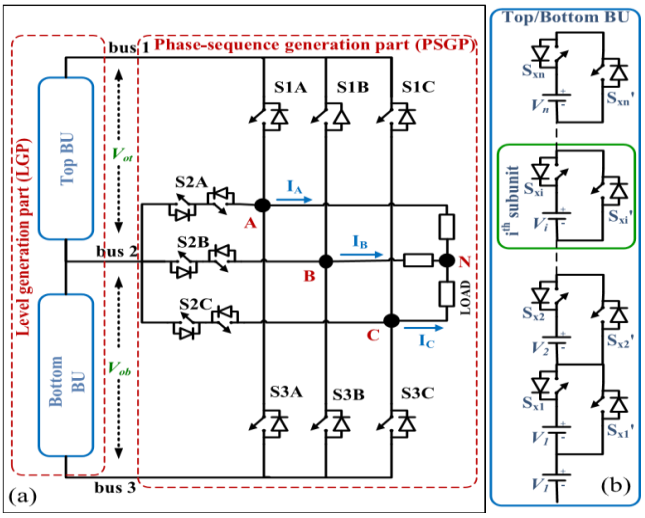


Fig.1 (a) Circuit schematic for the proposed *m*-level MLI. (b) Configuration of top/bottom BU

That the LGP has three output buses/terminals which are referred as bus 1, 2, and 3. The top BU of LGP is connected between buses 1 and 2, whereas the bottom BU is connected between buses 2 and 3. These three buses are also the common link between LGP and PSPG. The PSGP consists of a T-type inverter with three input and output terminals. The input terminals are directly connected to three buses 1, 2, and 3. And the output terminals are connected to 3-φ, *Y*-connected load. Thus, any phase *P* can be connected to bus *Q* (where *P* (*A, B, C*) and *Q* (1, 2, 3)) using power switch SQP. Further, the switches connecting bus 1 and 3, i.e., S1P and S3P are realized with single MOSFETs. And the switch S2P is realized using the anti-series connection of two MOSFETs as indicated in Fig. 1(a). Thus, PSGP is realized using 12 MOSFETs, which remains fixed for any level operation of the proposed MLI.

Therefore, the total number of the switches "N_{SW}" required for the realization of proposed MLI with "*n*" number of subunits in each BU is given by

$$N_{sw} = 4n + 12 \quad (1)$$

Similarly, the total number of dc voltage sources "N_{SRC}" required by the proposed MLI is given by

$$N_{src} = 2(n+1) \quad (2)$$

Now with the increasing value of "*n*", the number of voltage levels at the output will increase and it also depends upon the magnitudes of the dc voltage sources. Depending upon the magnitudes of the dc voltage sources, the proposed MLI can have two types of configurations, as described in the following sections.

1. Symmetrical Configuration

In this configuration, all dc voltage sources have equal magnitude, i.e.

$$V_1 = V_{dc}. \quad (3)$$

In the case of symmetrical configuration, the maximum number of levels "N_{LS}" generated by the proposed MLI is given as

$$N_{LS} = n + 3. \quad (4)$$

The advantage of symmetrical configuration is that it has huge number of redundant states, which increases exponentially with the number of levels.

2. Asymmetrical Configuration

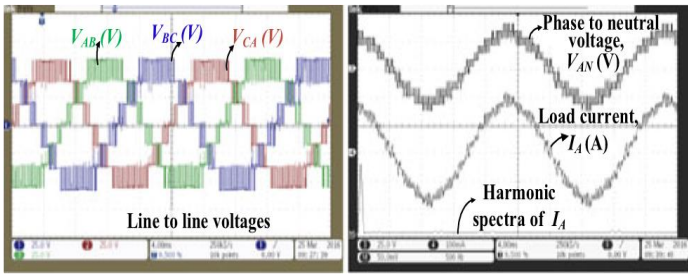
In this configuration, the magnitude of the dc voltage source in *i*th subunit is given by

$$V_i = 2^{i-1} V_{dc}. \quad (5)$$

Further, the maximum number of levels, "N_{LA}" generated by the MLI in case of asymmetrical configuration is given as

$$N_{LA} = 2^{n} + 2. \quad (6)$$

To justify the number of levels, the space vector (SV) diagram of the proposed inverter with $n = 3$ for both symmetrical and asymmetrical configurations is shown in Fig. 2. The thick red line in Fig. 2 shows the operating boundary of the proposed MLI.



(a) (b)

Fig. 2 SV diagram of proposed MLI in Symmetrical operation and (b) asymmetrical operation for $n = 3$.

III. RESULTS

A laboratory prototype of the proposed optimized system is fabricated to verify its performance. The system parameters taken for the laboratory prototype are given in Table I.The SV diagram of the MLI prototype for n = 1 is shown in Fig. 6. The thick red line denotes the four-level operating boundary of the proposed MLI. It can be observed that the MLI prototype will generate four-level output for both symmetrical and asymmetrical operation as n = 1. This can also be obtained by putting n = 1 in (4) and (6).

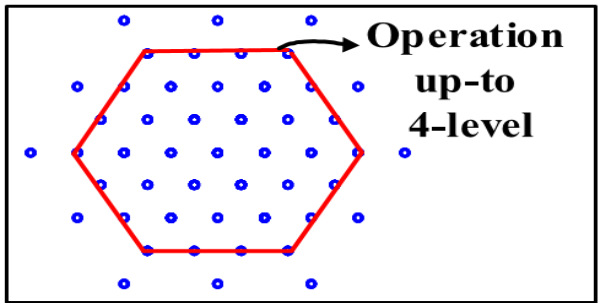


Fig. 3 SV diagram of the proposed MLI for n=1

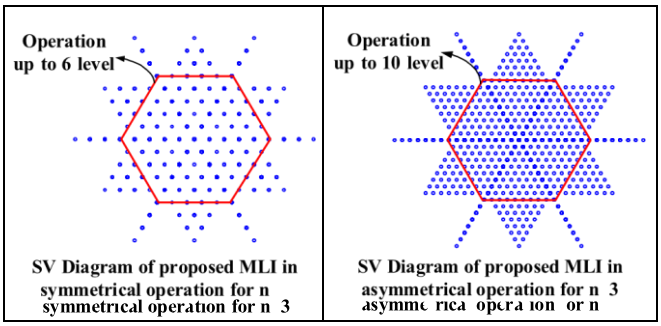


Fig. 4 Experimental results showing (a) line-to-line voltage (b) phase-to neutral voltage, load current and harmonic spectra of the load current of the proposed MLI.

TABLE- I

LABORATORY PROTOTYPE PARAMETERS SUMMERY

S.no.	Parameters	Italic
1	Optimised voltage frequency	50 Hz.
2	Switching frequency	2 KHz.
3	Per phase load resistance	185 Ω
4	Per phase load inductance	0.01H
5	MOSFET	IRF840
6	controller	TMS320LF28069
7	Data acquisition	Tektronix DPO 3034
8	Number of sub-units	1

A. *SIMULATION RESULTS*

The performance of the proposed 3-φ, MLI has been analysed with the help of a simulation model, developed in MATLAB/Simulink software integrated with PLECS block-set. Simulation results are given for both symmetrical and asymmetrical operation in the following sections.

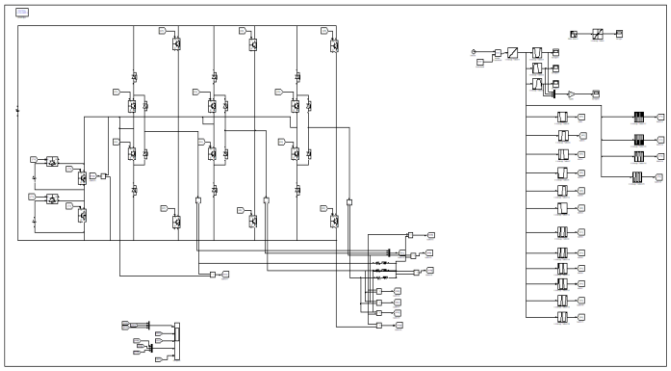


Fig. 5 simulation model of proposed topology

1) *Symmetrical Configuration*: The proposed MLI operates at 6-level in a symmetrical configuration for n = 3. This can be justified from the simulation results showing the line-to-line voltage waveform in Fig. 6(a) for symmetrical configuration of the proposed MLI. Further, the output voltages of top and bottom BUs, "V_{ot}" and "V_{ob}". It can be observed that four voltage levels are present in the waveforms of "V_{ot}" and "V_{ob}." Therefore, the operation in symmetrical configuration using three subunits in each BU is also supported by the simulation results. Moreover, the simulated three phase-to-neutral voltages and load currents are also shown in Fig. 6(d) and (e), respectively

2) *Asymmetrical Configuration*: The proposed MLI is also simulated for asymmetrical configuration with n=3. In this condition, the proposed MLI operates at 10-level, according to (5).This also supported by the simulated line-to-line voltage voltage waveforms as shown in Fig.6 (a).Further ,for asymmetrical configuration the output voltages of top and bottom Bus are presented. The presence of eight voltage level in the waveform of "V_{ot}" and "V_{ob}." Supports the operation of the proposed MLI in asymmetrical configuration.

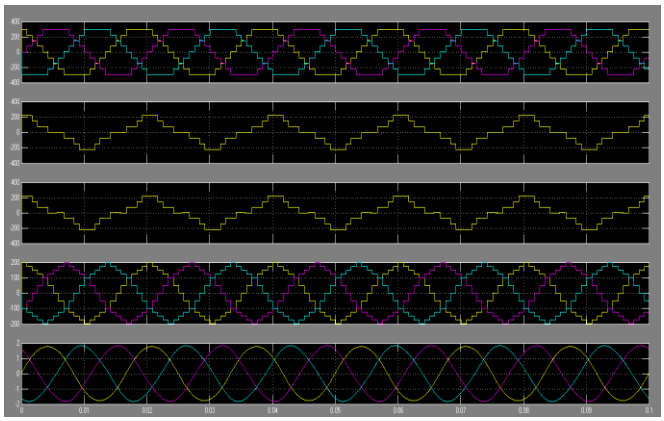


Fig. 6 Simulation results showing (a) line-to-line voltages, (b) output voltage of top BU, (c) output voltage of bottom BU, (d) phase-to-neutral voltages and(e) load current waveforms of the proposed 3-φ MLI in symmetrical operation

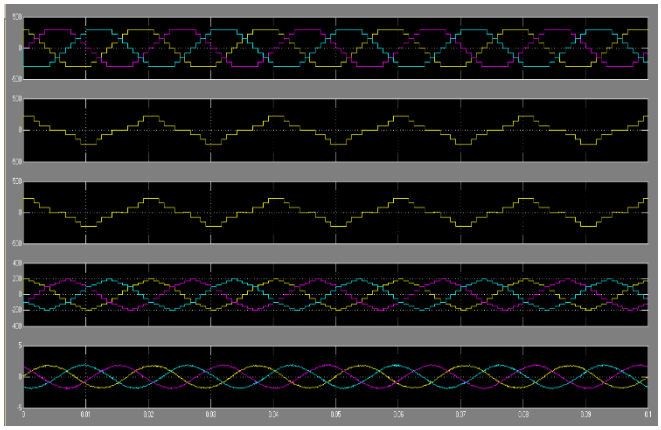


Fig. 7 Simulation results showing (a) line-to-line &&voltages, (b) output voltage of top BU,(c) output voltage of bottom BU, (d)phase-to-neutral voltages and (e) load current waveforms of the proposed 3-φ MLI in asymmetrical operation.

IV. CONCLUSION

This paper presents an optimized 3-φ MLI configuration with reduced number of component. The prominent features of the proposed MLI are as follows.

1) The proposed MLI configuration is built by cascading LGP and PSGP.
2) For higher level operation, only switches required are at the BUs only, which resides in the LGP. This reduces the requirement of extra devices compared to conventional topologies.

3) Also, each dc voltage source in the presented MLI topology is equally shared by all the phases. Thus, any chance of inter-phase asymmetry is avoided.

The above-mentioned points support that the proposed MLI is an optimized configuration for 3-φ operation with reduced number of switches. However, the proposed configuration is operated by using the SVs up to the red line only. The further work with an improved PWM strategy, which takes all the SVs in account, will be presented in the regular paper. This will further increase the number of levels at the output and linearity can be maintained in the over-modulation region with improved dc-bus utilization.

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