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Leakage Current Reduction in CMOS Circuits Using Stacking Technique

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ABSTRACT

This paper deals with The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk there by evolution of Deep Sub-Micron (DSM) technology. There by the extremely complex functionality is enabled to be integrated on a single chip. So, transistor size is reduced to few nanometers. By reducing the size drastically some problems are occurred. In that leakage power is one of the disadvantage. By using this stacking technique we are going to reduce the leakage currents.

Keywords : Low power, Power dissipation, Sub-threshold leakage current, Stacking effect, Cadence Virtuoso Tool.

I. INTRODUCTION

Over the past decades, the MOSFET has continually been scaled down in size. Typical MOSFET channel lengths were once several micro-meters, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometer. Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip.

Lowering the supply voltage (VDD) is the most effective way to reduce the power dissipation as it depends quadratically on VDD. But as VDD reduces, circuit delay will increase and thus degrades its performance. At the same time it is possible to maintain the performance by decreasing the threshold voltage (VTH) but then sub-threshold leakage current increases exponentially. Therefore, VDD and VTH have to be optimized to achieve the required performance and low power. As the feature size reduces shorter channel length results in sub threshold leakage current through a transistor when it is off. Thinner gate oxides have led to an increase in gate leakage current. By using Stacking technique we can reduce leakage current up to 50-60% .

II. SOURCES OF POWER CONSUMPTION

The two sources of power consumption in digital CMOS circuits are Active power and Static power. Active power can be further classified into i) Switching power or dynamic power and ii) Short-circuit power. Switching power consumption occurs due to charging and discharging of load capacitances. Short-circuit power consumption takes place when there exists direct path from supply to the ground

terminal. The static power occurs due to all inputs are held at some valid logic level and the circuit is in charging and discharging state.

The downscaling of gate oxide thickness increases the field oxide across the gate resulting to electron tunneling from gate to substrate or substrate to gate. The resulting current is called as leakage current in the CMOS circuits.

III. TECHNIQUES TO REDUCE LEAKAGE CURRENT

A. SVL TECHNIQUE

Self- Controllable-Voltage level circuit (SVL) has been developed, that not only reduces leakage power but also retains data during stand by period. Self-Voltage Level (SVL) controllable switch is a technique which allows full supply voltage to be applied in active mode, and reduced supply voltage in inactive mode. Also this appears to be particularly promising for reducing gate / sub-threshold leakage currents.

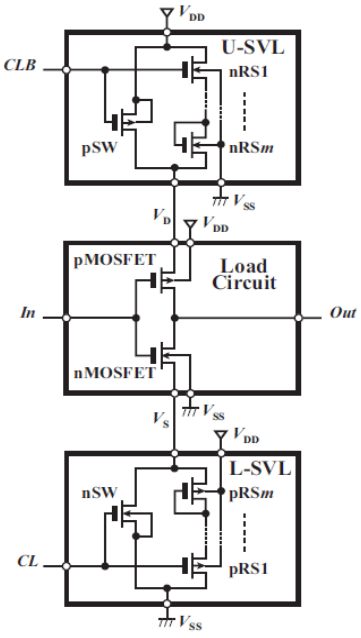

Figure 1 : SVL technique applied to CMOS inverter

Here self-controllable switch can be used either at the upper side of the standard cell to reduce supply voltage (USVL scheme) or at the lower end of the cell to raise the potential of the ground node (LSVL scheme). From fig.1, the upper SVL (U-SVL) circuit contains two or more PMOS transistors connected in series and one NMOS in parallel of these series PMOS transistors. Similarly, the L-SVL circuit contains two or more NMOS transistors connected in series and one PMOS in parallel of these series NMOS transistors. The limitations of SVL technique is huge circuitary, Cost is very high, It consumes more area, leakage currents can be reduced up to 30% only.

B. PROPOSED METHOD

The proposed method is Stacking Technique. By using the Stacking Technique we simulate basic logic gates like NOT, NOR, NAND gates. In Stacking Technique we have two types. They are forced PMOS and forced NMOS techniques.

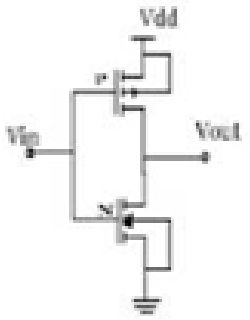

Figure 2 : CMOS Inverter

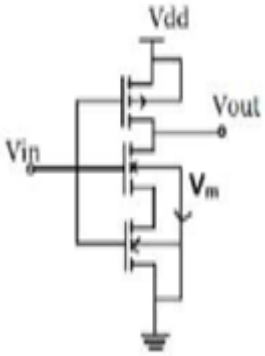

Figure 3 : Forced NMOS Stacking Technique

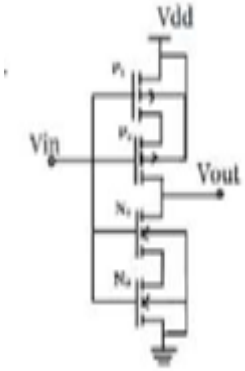

Figure 4 : Forced PMOS and NMOS Stacking Technique

IV. RESULTS

We have observed that the leakage currents are reduced by using Stacking technique. The reduced leakage currents are shown in table1.

Table 1 : Simulation results for different Stacking techniques

Output Current(A)				
S. No	Input Voltage(V)	CMOS Inverter	Forced NMOS Stacking Technique	Forced PMOS and NMOS Stacking Technique
1	0	5.661(pA)	2.84(pA)	2.84(pA)
2	0.1	57.09(pA)	13.1(pA)	13.1(pA)
3	0.2	1.01(nA)	215.1(pA)	215.1(pA)
4	0.3	15.63(nA)	3.6(nA)	3.54(nA)
5	0.4	149.04(nA)	40.5(nA)	39.92(nA)
6	0.5	836.49(nA)	260.4(nA)	260.5(nA)
7	0.6	684.13(nA)	668.4(nA)	233.7(nA)
8	0.7	122.5(nA)	120.5(nA)	39.01(nA)
9	0.8	14.6(nA)	14.6(nA)	4.19(nA)
10	0.9	953.05(pA)	952.6(pA)	253.2(pA)
11	1	82.04(pA)	82.04(pA)	23.01(pA)

V. CONCLUSION

Continuing to shrink the dimensions of electronic devices is important in order to increase speed, reduce device switching energy, increase system functionality, and reduce manufacturing cost per bit. With reduced gate length, leakage currents increases proportionally. In this project, stacking technique is employed to reduce leakage currents below 100nm. Simulation results show that this technique efficiently reduces leakage currents.

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