Design and Construction of 3 x 3 Bits Programmable Logic Array (PLA) Circuit

Sanda Win*, San San Htwe, Sandar Win, Myint Myint Swe

Natural Science Department, UCSTaungoo, Taungoo, Bago, Myanmar

ABSTRACT

A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented to produce an output. It has 2^N AND gate s for N input variables and for M outputs from PLA, there should be M OR gates, each with programmable inputs from all of the AND gates. This layout allows for many logic functions to be synthesized in the sum of products canonical forms. The Programmable Logic Array (PLA) has a programmable AND array followed by a programmable OR array. Programmable Logic Array (PLA) circuit is built by using AND gates and OR gates. The 3x 4 bits data can be stored in this circuit. The large storage data bits of PLA circuit store by a using large AND-OR array with lots of inputs and product terms, and programmable connections. Programmable Logic Array circuit functions as ROM circuit.

Keywords : Programmable, Array, Data, Logic, Bit

I. INTRODUCTION

A Programmable Logic Array (PLA) is a type of logic device that can be programmed to implement various kinds of combinational logic circuits. The device has a number of AND and OR gates which are linked together to give output or further combined with more gates or logic circuits. PLAs have numerous unique applications. A micro-processor chip uses many PLAs because of easy of design change and check. In particular, PLAs are used in its control logic, which is complex and requires many changes, even during its design. Also PLA are used for code conversions, micro program address conversions, decision tables, bus priority resolvers, and memory overlay.

II. FUNDAMENTAL CIRCUIT THEORY

A. Memory

Memory is the portion of a system for storing binary in large quantities. Each storage element in a memory can retain either a 1 or a 0 and is called a cell. Memories are made up of arrays of cells and its location can be identified by specifying a row and a column.

B. Read only Memory (ROM)

Read Only Memory (ROM) is the primary memory unit of any computer system along with the Random Access Memory (RAM), but unlike RAM, in ROM, the binary information is stored permanently. Now, this information to be stored inside the ROM. One, it is stored which it remains within the unit, even when power is turned off and on again. The information is embedded in the ROM, in the form of bits, by a process known as programming the ROM. Here, programming is used to refer to the hardware procedure which specifies the bits that are going to be inserted in the hardware configuration of the device.

C. Programmable Logic Device

Programmable logic device works like a ROM but is a more efficient solution for implementing sparse output functions. There are two types of programmable logic devices:

(1) Programmable Logic Array (PLA)
(2) Programmable Array Logic (PAL)

D. Programmable Logic Array (PLA)

A Programmable logic array (PLA) has a programmable AND array at the inputs and programmable OR array at the outputs. The PLA has a programmable AND array instead of hard-wired AND array. The number of AND gates in the programmable AND array are usually much less and the number of inputs of each of the OR gates equal to the number of AND gates. The OR gate generates an arbitrary Boolean function of minters equal to the number of AND gates. Figure 1 is block diagram of Programmable Logic Array.
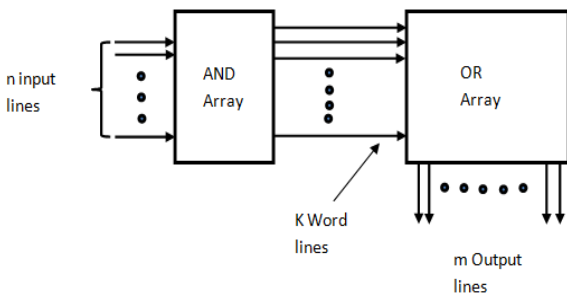

Figure 1. Block diagram of Programmable Logic Array Circuit (PLA)

E. Programmable Array Logic (PAL)

Programmable Array Logic (PAL) is a type of Programmable Logic Device (PLD) used to realize a particular logical function. PALs comprise of an AND gate array followed by an OR gate array as shown by Figure 2. However it is to be noted that here only the AND gate array is programmable unlike the OR gate array which has a fixed logic. This is Programmable-AND and fixed OR structure of PALs make them less flexible from programming point of view when compared with Programmable Logic Arrays (PLAs). However due to the same reason PALs is less expensive than PLAs.
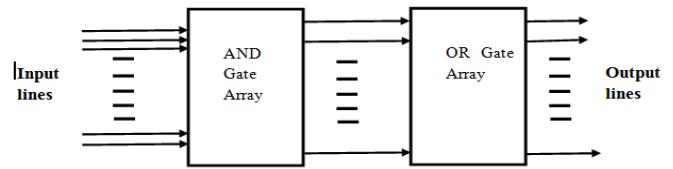

Figure 2. Block diagram of Programmable Array

F. Difference between PLA and PAL

The PLA is PLD, comprised of two levels of programmable logic AND plane and OR plane. PAL contain only programmable AND plane and fix OR plane. When it comes to availability, the PAL is more readily, the PAL is more readily available along with easy production. In contrast, the PLA is not easily available. The PLA is more flexible than a PAL.PLA is costlier as compared to the PAL.A number of functions provided by PLA are more relatively because it enables the programming of the OR plane also. PLA works faster while PLA is slower comparatively. Programmable Logic Array (PLA) and Programmable Array Logic (PAL) are the PLD (Programmable Logic Devices) where PLA is more adaptable and flexible than PAL. However, PAL can easily produce a combination logic circuit. Figure 3 is circuit diagram of Programmable Array Logic (PAL). Figure 3 shows the internal structure of a PAL with m inputs and n outputs. Each of the input line is showed to pass through the buffers and/or inverters. All of these inputs are connected each and every AND gate present in the PAL.

G. Logic Gates

Digital systems are said to be constructed by using logic gates. A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low 0 or high 1 represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately 0V, while the high state is approximately positive 5V. These gates are the AND, OR, NOT, NAND, NOR, EXOR, and EXNOR gates.
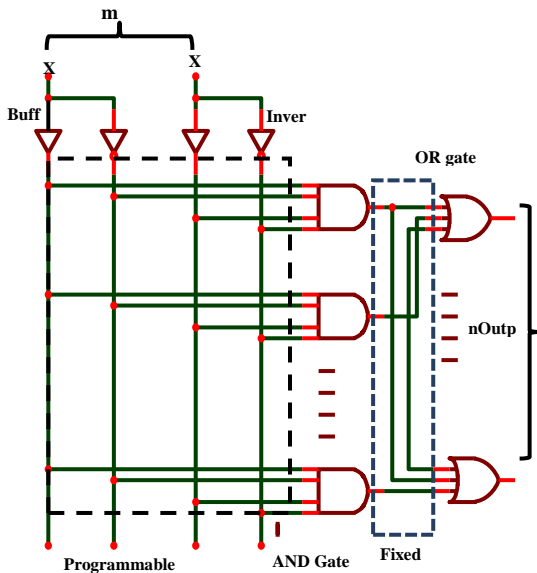
Figure 3. Circuit diagram of Programmable Array Logic (PAL)

H. AND Gates

The AND gates is an electronic circuit that gives a high output 1 only if all its inputs are high. The AND gate is so named because, if 0 is called false and 1 is call true ,the gate acts in the same way as the logical and operator .The following illustration and table show the circuit symbol and logic combinations for an AND gate. The output is true when both inputs are true. Otherwise, the output is false.

I. OR Gates

The OR gates is an electronic circuit that gives a high output 1 if one or more of its inputs are high. The OR gate gets its name from the fact that it behaves after the fashion of the logical inclusive OR. The output is true if either or both of the inputs are true .If both inputs are false, then the output is false.

J. CD 4073 Triple 3-Input AND Gate IC

CD 4073 Triple 3-input AND gate provides the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates. This IC is medium speed operation: t_{PLH}, t_{PHL} = 60 ns at V_{DD} = 10V .It is 100% tested for quiescent current at 20V. Maximum input current is 1μA at 18V over full package–temperature range 100nA at 18V and 25°C. This IC is standardized and symmetrical output characteristics. Figure 4 is pins diagram of CD 4073 triple 3-input AND gate IC.

K. CD 4072 Dual 4-Input OR Gate IC

The 4072 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4072B DUAL 4 INPUT OR GATE provides the system designer with direct implementation of the positive logic OR function and supplement the existing family of CMOS gates. Figure 5 is pins diagram of CD 4072 dual 4-input OR gate IC.

L. 4049 Hex NOT Gate IC

These ICs are usual because their gate inputs can withstand up to +15V even if the power supply is lower voltage. These ICs are unusual because they are capable of driving 74LS gate inputs directly. To do this they must have a +5V supply (74LS supply voltage). The gate output is sufficient to drive four 74LS inputs. Figure 6 is pins diagram of CD 4049 NOT gate IC.
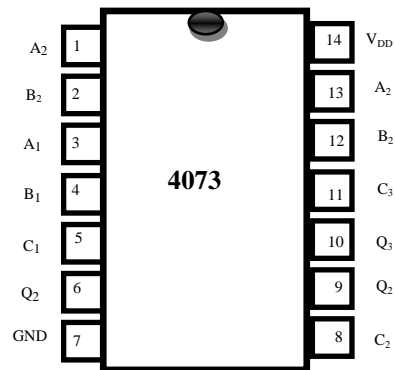

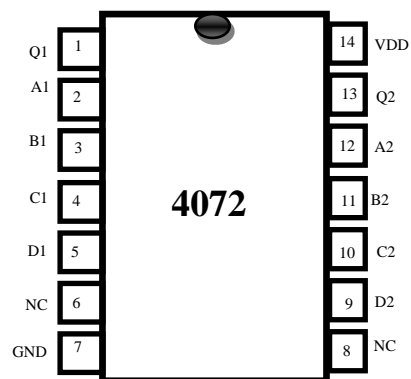Figure 4. Pins diagram of CD 4073 triple 3-input AND gate IC

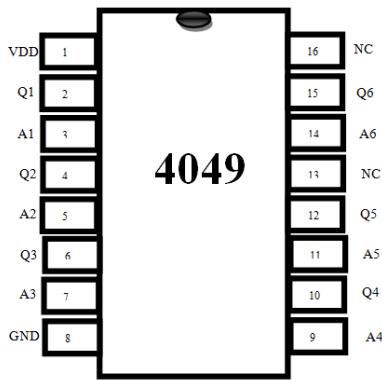Figure 5. Pins diagram of CD 4072 dual 4-input OR gate IC

Figure 6. Pins diagram of CD 4049 NOT gate IC

III. OPERATION OF PROGRAMMABLE LOGIC ARRAY (PLA) CIRCUIT

A Programmable Logic circuit is built by using Hex-inverter IC (4049 NOT gate IC), 3-input AND gate IC (4073 IC) and 4- input OR gate (4072 IC). The definition of term PLA presents the Boolean function in the form of a sum of product (SOP).The designing of this programmable logic array can be done using the logic gates like AND, OR, and NOT by fabricating on the chip, that makes every input as well as its compliment obtainable toward every AND gate. An every AND gate's output is connected to the every OR gate. Finally, the output of the OR gate generates the outputs of this circuit. The complete circuit diagram is shown in Figure 7. The inputs and outputs action table is shown in Table I.
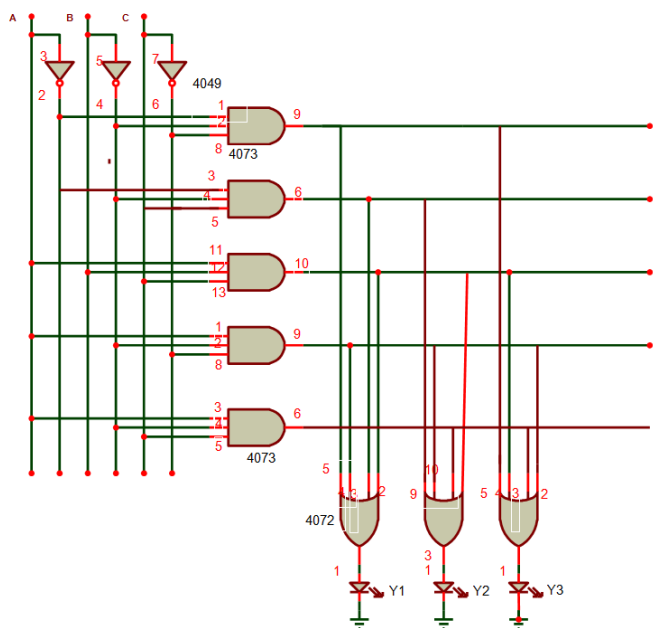

Figure 7. The complete circuit diagram of Programmable Logic Array circuit

IV. APPLICATIONS OF PROGRAMMABLE LOGIC ARRAY (PLA) CIRCUIT

Programmable Logic Array circuit is used to provide control over data path .It can also be used as a decoders. Programmable Logic Array (PLA) circuit is used as a BUS interface in programmed I/O. Programmable array logic most usually employed in FPGA (Field Programmable Gate Arrays) allow for rapid testing of digital systems created trough computer schematic editors such as systems designed in an HDL such as VHDL or Verliog. Being able to complete test and edit digital systems all within a matter of minutes has greatly accelerated the digital system design process.

TABLE. I
INPUTS AND OUTPUTS ACTION OF PROGRAMMABLE LOGIC ARRAY (PLA)

INPUTS						OUTPUTS			OUTPUTS STORAGE DATAS
A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	Y1	Y2	Y3	
0	0	0	1	1	1	1	0	1	Y1= $\bar{A}\bar{B}\bar{C}+\bar{A}\bar{B}C+$ ABC+ $_A\bar{B}\bar{C}$
0	0	1	1	1	0	1	1	0	Y2= $\bar{A}\bar{B}C+_A\bar{B}\bar{C}+$ ABC+ $_A\bar{B}C$
1	1	1	0	0	0	1	1	1	
1	0	0	0	1	1	1	1	1	Y3= $\bar{A}\bar{B}\bar{C}+$ $A\bar{B}C+$ABC+A $\bar{B}\bar{C}$
1	0	1	0	1	0	0	1	1	

V. CONCLUSION

The PLA circuit is no need for the time-consuming logic design of random-logic gate networks and even more time–consuming layout. This type of circuit design checking is easy, and design change is also easy. Circuit layout is far simple than that for random–logic gate networks, and thus is far less time–consuming. When new IC fabrication technology is introduced, can be used previous design information with ease but without change, making adoption of the new technology quick and easy. Only the connection mark needs to be custom-made. Random–logic gate networks have higher speed than PLAs or ROMs. Random–logic gate

networks occupy smaller chip areas than PLAs or ROMs, although the logic design and the layout of random –logic gate networks are far more tedious and time consuming. Also, with large production volumes, random–logic gate networks are cheaper than PLAs or ROMs.

VI. REFERENCES

[1]. Andres, kent (October 1970) "A Texas instruments Application Report: MOS programmable logic arrays Texas instruments", Bulletin CA-158.

[2]. Hayes, Monson, Schaum's "Outline of Digital Signal Processing". New York: McGraw-Hill, 1998.

[3]. Dahnoun, Naim "Digital Signal Processing Implementation Using the TMS320C6000DSP Platform" Reading, Mass: Addison-Wesley Longman, 2000.

[4]. Kuo, Sen, and Bob Lee "Real-Time Digital Signal Processing Implementations Applications and Experiments with the TMS320C55x", New York: John Wiley & Sons, 2001

Cite this article as :