International Journal of Scientific Research in Science, Engineering and Technology (www.ijsrset.com)
© 2020 IJSRSET | Volume 7 | Issue 3 | Print ISSN: 2395-1990 | Online ISSN : 2394-4099
DOI : https://doi.org/10.32628/IJSRSET207348

Robust 12T Sram Cell Using 45nm Technology

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ABSTRACT

SRAM cells are used in many applications such as micro and multi core processor. SRAM cell improves both read stability and write ability at low supply voltage. The objective is to reduce the power dissipation of a novel low power 12T SRAM cell. This method removes half-select issue in 6T and 9T SRAM cell. This work proposes new functional low-power designs of SRAM cells with 6T, 9T and 12 transistors which operate at only 0.4V power supply in sub-threshold operation at 45 nm technology. The leakage power consumption of the proposed SRAM cell is thereby reduced compared to that of the conventional six-transistor (6T) SRAM cell. 12T cell obtains low static power dissipation.

Keywords : SRAM, Micro wind Software, Power consumption, Transistors.

I. INTRODUCTION

An exceptional growth is achieved by electronics industry over the last two decades, mainly due to the expeditious advances in integration technologies, due to the emergence of VLSI. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been progressing undeviatingly, and at a very instant pace. Typically, the required computational power of these applications is the driving exertion for the fast blooming of domain. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design.

One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth. The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective services such as broadcasting), which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility. As the SRAM cells are incorporated by latch, the refresh operation isn't required to keep the data during power on condition in SRAM cells. Every one of the systems like microprocessors, hand held gadgets, workstations have the cache memory which is outlined by SRAM cells due to its transistor favorable circumstances of giving quick exchanging and low power utilization. To store a single bit of data SRAM utilizes four transistors.

The basic parameters of SRAM cells are the speed and furnishes multiple designs with the point of corrupting the power utilization during read write tasks of SRAM. By considering this need, in this paper some standard SRAM cell outlines viz. 6T, 7T,

8T, 9T and 10T have taken and every one of these circuits are composed with the different nanometer technologies to test their behaviour and conduct under various conditions to comprehend their usefulness and to discover the reasons and chances for reducing power utilization.

This paper is sorted out as follows; the survey of various existing methods of SRAM cells about their functionality during read and write operations is displayed, 12T SRAM cell characteristic behaviour in 45nm technology is exhibited as plots, additionally given the insights about their area occupation as for their layout.

II. LITERATURE SURVEY

A. 6T SRAM

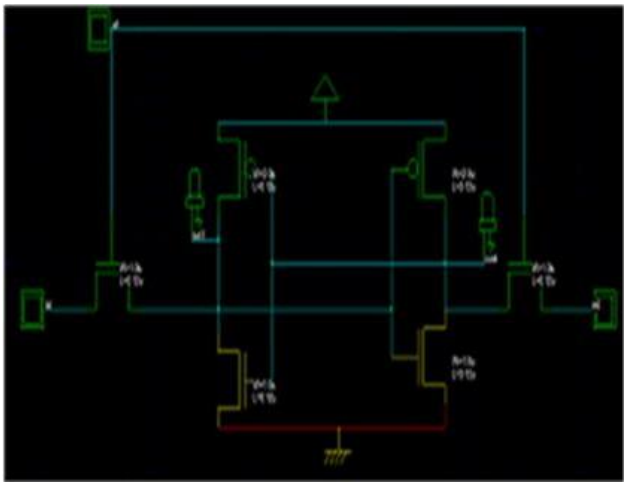

Fig 1 : 6T SRAM schematic

During read pre-charge both bit lines to high at that point turn on word line. One of the two bit lines will be pulled down by the cell either BL (bit line genuine) or BLB (bit line complement) depending upon the stored data on internal nodes. A sense enhances changes over the strange signal to a logic-level output. At that point, toward the finish of the read task BL releases and BLB remains high.

During write activity the WL line goes high and the BL is forced to either the positive supply voltage VDD (depending upon the data) over driving the data of the memory cell. During hold state the WL is held low and BL and BLB are left floating or driven to VDD.

B. 9T SRAM

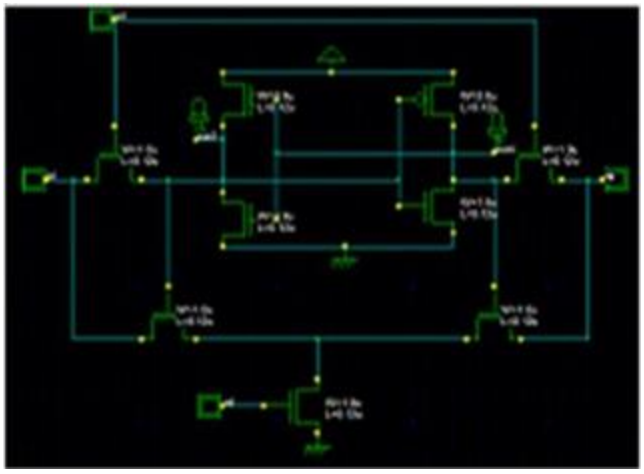

Fig 2 : 9T SRAM schematic

During write activity WL is high; M5 and M6 are equivalent to "1". N1 and N2 are the nodes of which gets to transistors M5 and M6. M9 is low and no input voltage is given to RD (M9). Subsequently exchanging M7 and M8 are low. In the event that there is any change in M9 then M7 and M8 likewise changes. To write "0" in the SRAM cell the bit lines BL and BLB are releasing and charging then "0" is constrained through SRAM cell through M3.Simultaneously,to make "0" in N2 bit lines BL and BLB are charging and releasing.

During read task RD signal is high and WR is low. M9 will be in saturation, to store "1" in N1 the bit line BL is released through M7 and M9. To store "1", bit line BLB (M6) is released through M8 and M9. In the event that the transistors M5 and M6 are in cut off mode N1 and N2 are totally isolated from the bit lines during read task.

III. PROPOSED METHOD

12T SRAM

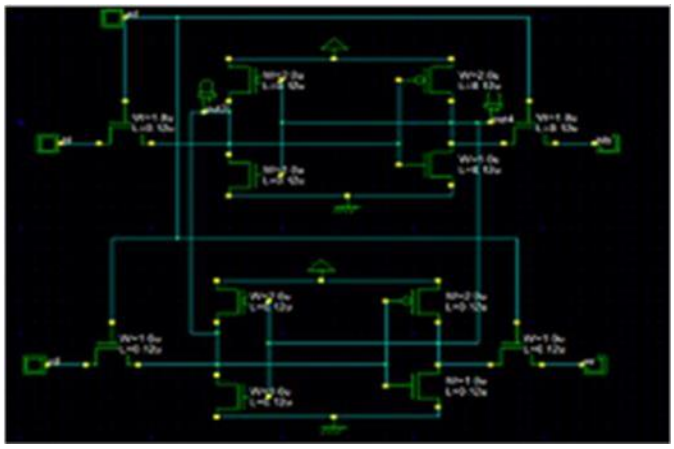

Fig 3 :12T SRAM schematic.

In the 12T SRAM when we high the WL=1 then the data passes through the M2,M11,M12 and WR the operation is out4 at high as well as the out3 at high WL=1;BL=1 and RD=1 then the trans coupling ON and data transmission possible at out3. When the WL=1 and RD=1 then both coupling half of the transistors ON and data transfer to the out4 side. When the BL=1 then the data transmission is possible only cross coupled transistor then the out3 data is high at that time BL=1 and BLB=1 then M11 is open than data possible at only one side than out3 high.

The BLB=1 and WL=1 the data transmits only cross coupled transistor than out3 is high as well as BLB=0 and WL=1 the out3is only high because trans coupled system. When WL=1 and WR=1 then the output out4 is high i.e., WL=1 then it directly transmit the data to M11 transistor as well as M12 as a WR=1 data. When WL=BL=RD=BLB=WR=1 then all data will be activated than the data transmitted to the out3.When WL=BL=RD=BLB=WR=0 then the out3 is high. Here the data transmission possible only coupling transistor and supply.

IV. SIMULATION RESULTS

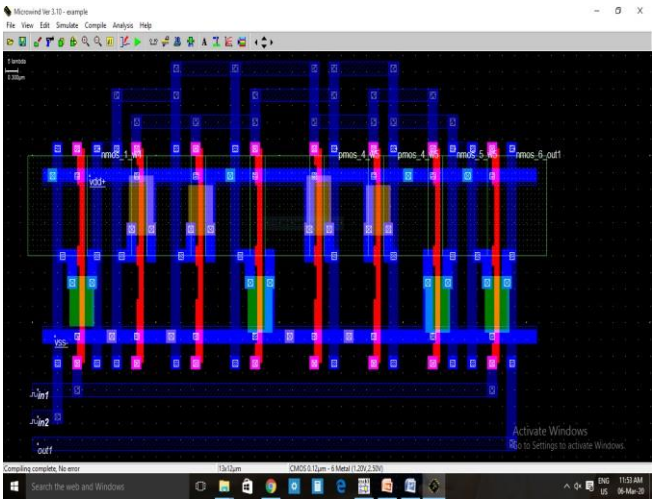

Fig 4 :Layout diagram of 6T SRAM Cell

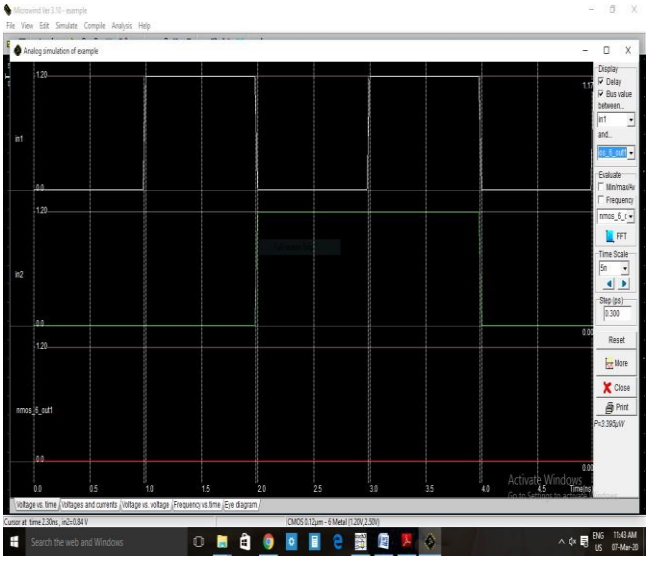

Fig 5 :Voltage Vs Time of 6T SRAM Cell

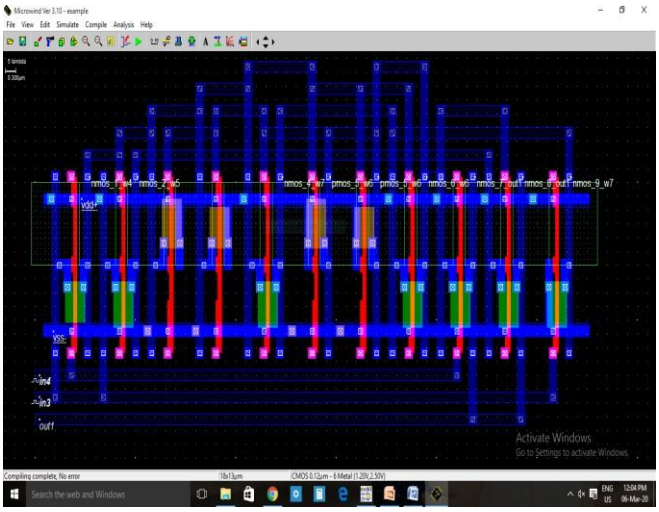

Fig 6 :Voltage Vs Time of 9T SRAM Cell

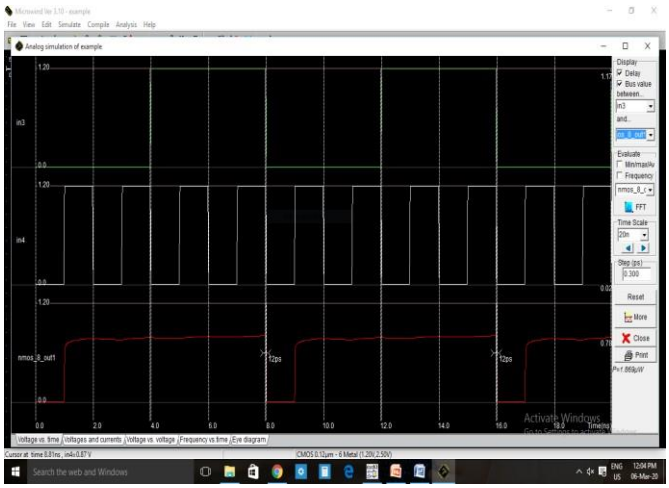

Fig 7 :Layout diagram of 12T SRAM Cell

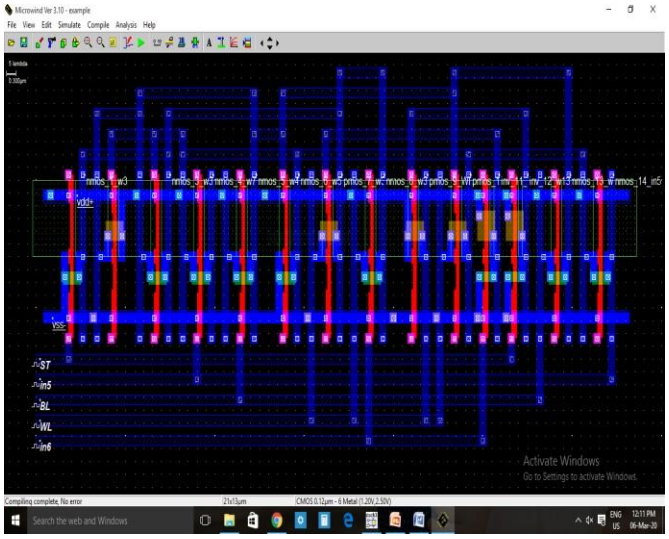

Fig 8 :Layout diagram of 9T SRAM Cell

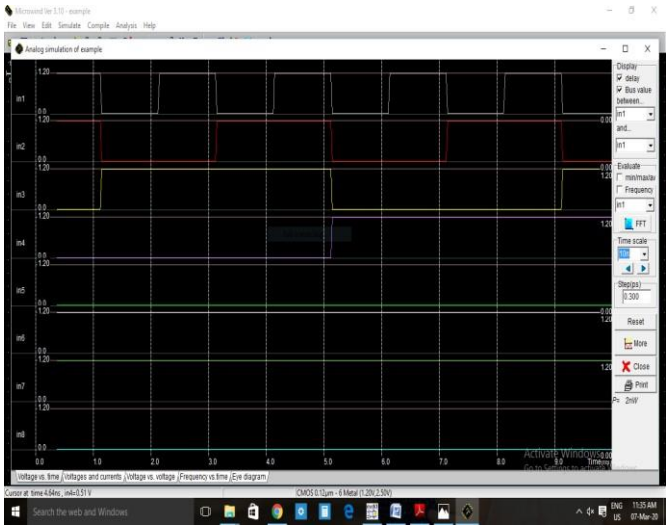

Fig 9 :Voltage Vs Time of 12T SRAM Cell

Table 1 : Comparison of power consumption of all topologies in various SRAM Cell design

SRAM Cell design	Power consumption
6T	3.39 µW
9T	1.86 µW
12T	2 nW

V. CONCLUSION

Some standard SRAM cells of 6T,9T,12T SRAM have taken and intended to test their behavior and functionality with various technologies as for their benefits and bad marks. The detailed examination of these memory cells power consumption in various SRAM cell designs technologies has talked about and their layouts has additionally designed.

VI. FUTURE SCOPE

It is well known that sub threshold circuit design where the supply voltage is less than the device threshold voltage can reduce the energy. That power reduction comes with significant performance drawback and susceptibility to process, voltage, and temperature (PVT) variations.Sub threshold circuit design performance is better than proposed 12T SRAM design in terms of power consumption and delay.

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Cite this article as :

N. Geetha Rani, N. Jyothi, P. Leelavathi, P. Deepthi Swarupa Rani, S. Reshma, "Robust 12T Sram Cell Using 45nm Technology", International Journal of Scientific Research in Science, Engineering and Technology (IJSRSET), Online ISSN : 2394-4099, Print ISSN : 2395-1990, Volume 7 Issue 3, pp. 170-174, May-June 2020. Available at doi : https://doi.org/10.32628/IJSRSET207348
Journal URL : http://ijsrset.com/IJSRSET207348