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Prominent Speed Low Power Compressor Based Multiplier for Proficient VLSI Architecture

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ABSTRACT

In the recent years the computational units are optimized to reduce the computation time. Multiplier is an electronic circuit used in digital electronics and has a significant role in vlsi applications. The 4:2 compressors have a flexibility of switching between exact and appropriate operating modes. In the appropriate mode the dual quality compressors provides higher speeds and consumes low power. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors are used in another type of multiplier and are evaluated in 45 nm standard CMOS technology. By comparing the parameters of this multiplier with those of appropriate multipliers, the results indicate a better in almost all the aspects.

Keywords : 4-2 Compressor, Dadda, Wallace

I. INTRODUCTION

Multipliers are one of the most significant blocks in computer arithmetic and generally used in different digital signal processors. There is a growing demand for high speed multipliers in different applications of computer systems. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. There are two general architectures for the multipliers, which are sequential and parallel. While sequential architectures are low power, their latency is very large. On the other hand, parallel architectures (such as Wallace tree and Dadda) are fast while having high- power consumptions.In order to reduce the high power consumption in the parallel multipliers we are designing a wallace multiplier seeking the help of a dual quality 4:2 compressor. The dual-quality 4:2 compressors has an ability of switching between the exact and approximate operating modes during the runtime. In the proposed system we overcome the problems in the existing system like area,delay,power dissipation.

II. EXISTING SYSTEM A 4-2 Compressor

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has Three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two Cascaded 3-2 compressor circuits. The conventional

implementation of a 4-2 compressor is composed of two serially connected full adders, as shown in Figure 1. Different structures of 4-2 compressors are reported in literature and these are governing by the basic equation as follow

X1+ X2 + X3 + X4 + Cin = Sum + 2·(Carry + Cout)

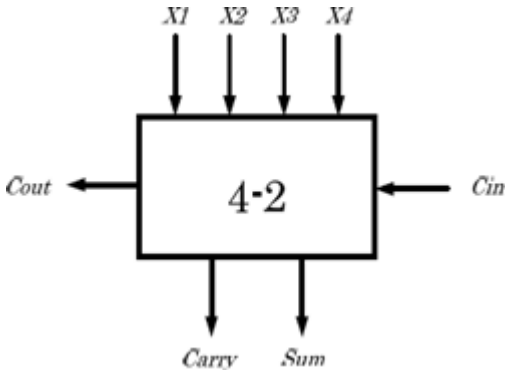

Figure-1:4-2 compressor

The common implementation of a 4-2 compressor is accomplished by utilizing two full-adder (FA) cells [8]. Different designs have been proposed in the literature for 4-2 compressor. The optimized design of an exact 4- 2 compressor based on the so-called XOR-XNOR gates ; a XOR-XNOR gate simultaneously generates the XOR and XNOR output signals.

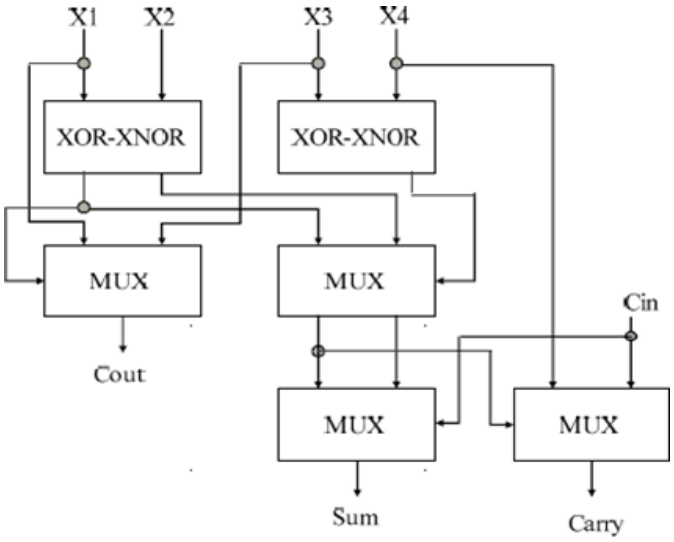

Figure-2: 4-2 compressor xor –xnor module

B Dadda multiplier

The dadda multiplier is a hardware multiplier designed and invented by computer scientist Lungi Dadda in 1965. Due to extra level of carry lookahead logic for smallest multiplier dadda multiplier requires more gates. A closer examination of delays considered at the gate level rather than at the full adder level says that the wallace multiplier yields a slightly faster design due to its smaller final adder. However both multipliers need three step procedure for the formation and reduction of partial products.

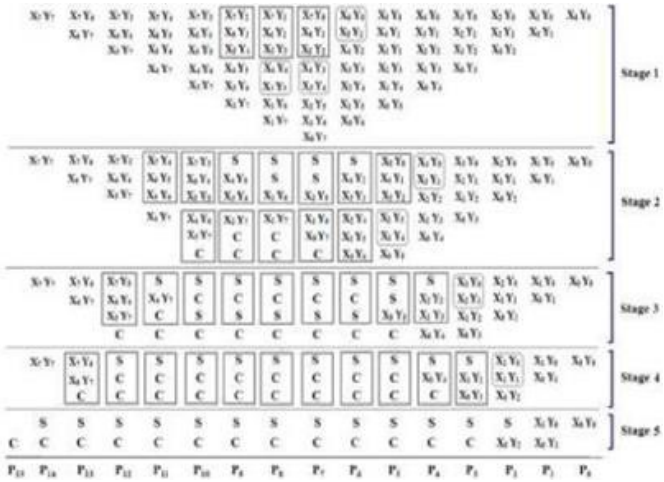

Figure-3: Dadda multiplier

C Multiplication

In this section, the impact of using the proposed compressors for multiplication is investigated. A fast (exact) multiplier is usually composed of three parts (or modules) [8].

• Partial product generation.
• A Carry Save Adder (CSA) tree to reduce the partial products' matrix to an addition of only two operands.
• A Carry Propagation Adder (CPA) for the final computation of the binary result.

In the design of a multiplier, the second module plays a pivotal role in terms of delay, power consumption and circuit complexity. Compressors have been widely used [9, 10] to speed up the CSA tree and decrease its power dissipation, so to achieve fast and low-power operation. The use of approximate

compressors in the CSA tree of a multiplier results in an approximate multiplier.

III. PROPOSED SYSTEM

A Wallace tree multiplier

The Wallace tree multiplier is considerably faster than a simple array multiplier because its height is logarithmic in word size, not linear. However, in addition to the large number of adders required, the Wallace tree's wiring is much less regular and is not much complexer.

Wallace tree styles use a log-depth tree network for reduction. Faster, but irregular, they trade ease of layout of speed. While subsequently fast than Carry-save structure for large bit multipliers. The high speed multiplier that sums up the partial product bits in parallelmultipliers using a tree of carry-save adders generally known as the "Wallace Tree". Three step processes are used to multiply two numbers.

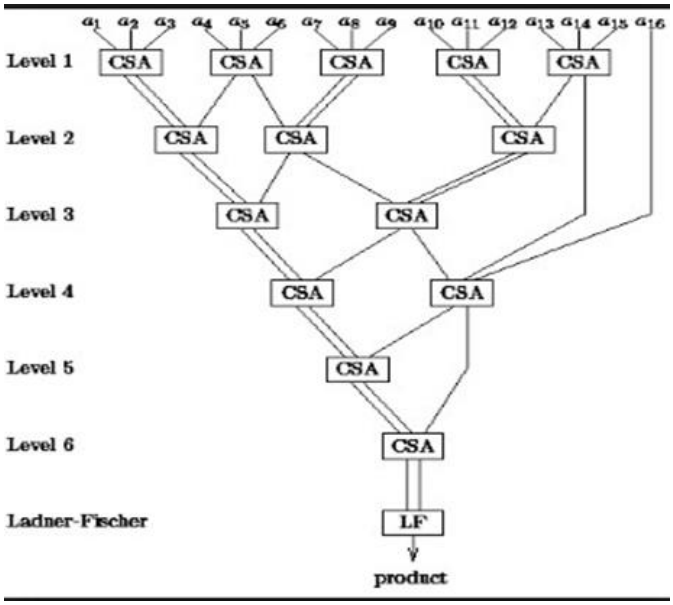

Figure-4: Wallace tree multiplier

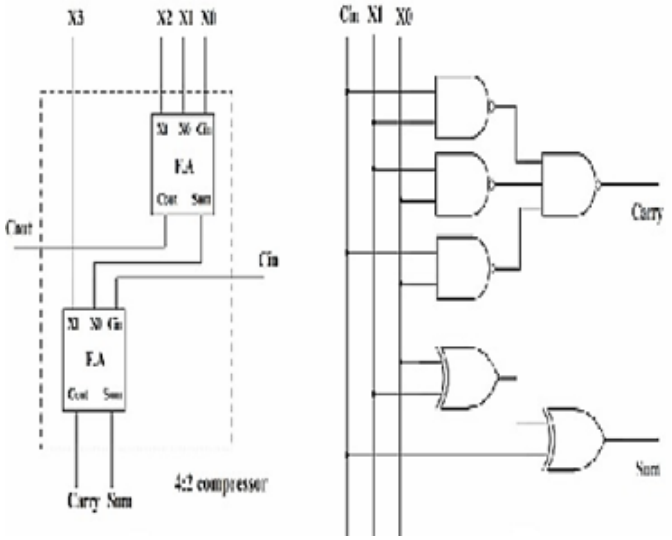

Figure-5: 4:2 compressor used in CSA's

B.Wallace tree multiplier with 4-2 compressor

A 8×8 unsigned Wallace tree multiplier is considered to assess the impact of using the proposed compressors in approximate multipliers. The proposed multiplier uses in the first part AND gates to generate all partial products.

In the second part, the approximate compressors proposed in the previous section are utilized in the CSA tree to reduce the partial products.

The last part is an exact CPA to compute the final binary result.Figure 4 shows the reduction circuitry of an exact multiplier for n=8. In this figure, the reduction part uses half-adders, full-adders and 4-2 compressors; each partial product bit is represented by a dot.

IV. RESULTS AND DISCUSSION

The proposed 8 bit architectures are developed in Xilinx platform. These are designed in verilog and are simulated in Xilinx Ism simulator and synthesized using XilinxXST.

Figure-6: Simulation output of dadda multiplier

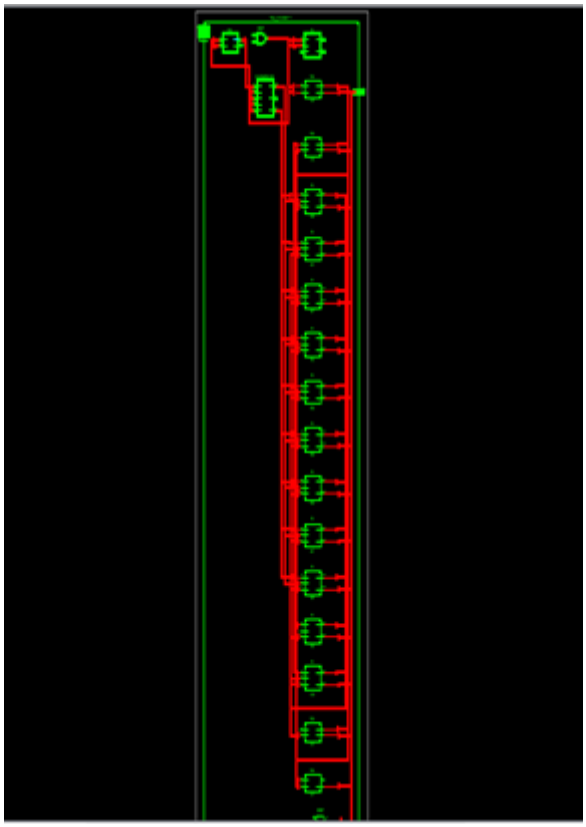

Figure-7: RTL schematic output of dadda multiplier

Figure-8: Simulation output of wallace multiplier

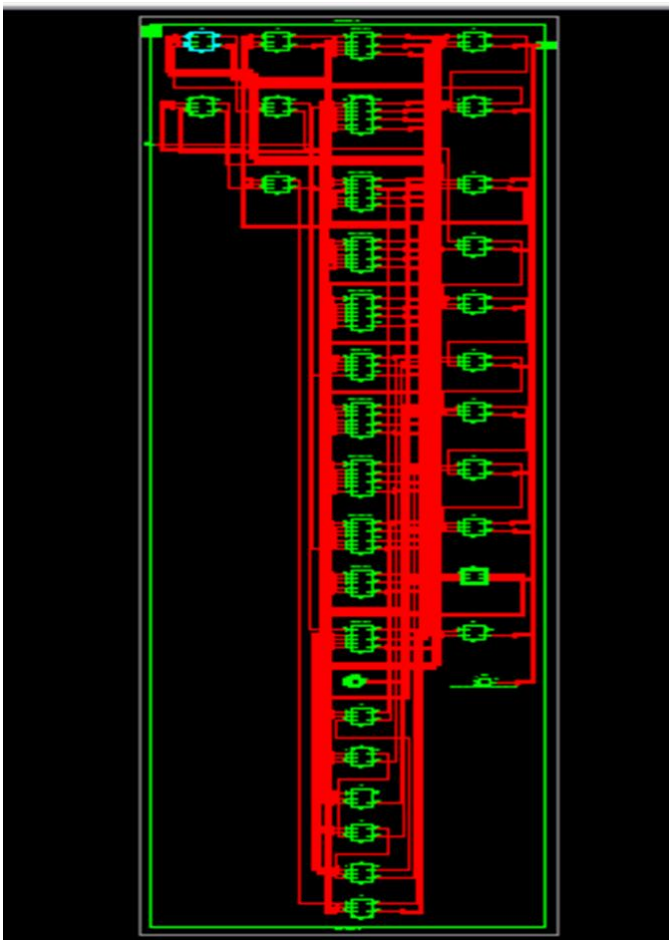

Figure-9: RTL schematic of proposed wallace multiplier

TABLE-1: SYNTHESIZE REPORT

S.No	ANALYSIS	EXISTING METHOD	PROPOSED METHOD
1	Slices	75	73
2	LUTs	132	128
3	IOs	33	33
4	IOBs	33	33
5	Delay	23.68.ns	23.028ns
6	Power consumption	48w	31w

V. CONCLUSION

The proposed wallace multiplier is using unique tree structure which gives in terms of speed when compared to the existing multiplier. The results

concluded that proposed multiplier acheived better computation speed and has less delay and low power consumption.

VI. REFERENCES

[1]. Sanjeev Kumar, Manoj Kumar —4-2 Compressor design with New XOR-XNOR Module‖, 4th International Conference on Advanced Computing and Communication technologies, pp. 106-111, 2014.

[2]. Z. Wang, G. A. Jullien, and W. C. Miller, —A new design technique for column compression multipliers,‖ IEEE Trans. Computers, vol.44, pp. 962-970. Aug 1995.

[3]. N. Weste, K. Eshranghian, Principles of CMOS VLSI Design: A System Perspective, 1993.

[4]. R. Zimmermann and W. Fichtner, —Low-power logic styles: CMOS versus pass-transistor logic,‖ IEEE Journal of Solid– State Circuits, vol.32, pp.1079-1090, July 1997.

[5]. M. Zhang, J. Gu, and C. H. Chang, —A novel hybrid pass logic with static CMOS output drive full-adder cell,‖ in Proc. IEEE Int. Symp. Circuits Syst., pp.317 -320, May 2003.

[6]. M. Shams, T. K. Darwish, and M. A. Bayoumi, —Performance analysis of low-power 1-bit CMOS full adder cells,‖ IEEE Transactions on VLSI Systems, vol. 10, pp. 20–29, Feb. 2002.

[7]. S.F. Hsiao, M.R. Jiang, J.S. Yeh, —Design of high low power 3- 2 counter and 4-2 compressor for fast multipliers‖, Electronic Letters, Vol. 34, No. 4, pp. 341-343, 1998

[8]. A. Weinberger, —4:2 Carry-Save Adder Module‖, IBM Technical Disclosure. Bulletin, Vol.23, January 1981.

[9]. S.Veeramachaneni,K.M.Krishna.L.Avinash,M.Srinivas—Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors,‖ in VLSI Design,324–329, Jan. 2007.

[10]. A.Mom eni, J.Han, P.Montushi, F.Lombardi.--Design and Analysis ofApproximate Compressors for Multiplication,vol64,no.4,989-994,Apr.2015

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