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# Power Optimization for ASIC Design (Low power ASIC)

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## ABSTRACT

The modern era of embedded system design is geared toward the design of low-power systems. One way to reduce power in an application-specified integrated circuit (ASIC) implementation is to reduce feature size. Scaling of feature sizes in semiconductor technology has been responsible for increasingly higher computational capacity of silicon. However, questions regarding the limits of scaling have arisen in recent years due to the presence of leakage. As the supply voltage is lowered to satisfy the performance requirement, the threshold voltage has to be scaled, which increases leakage. More than 40% of the total power consumption is due to leakage of the transistor is in DSM. This leakage will increase with scaling become comparable with switching power. The goal of this paper is to analyse different low power circuits and optimization techniques to improve the power dissipation with the use of power gating components, retention registers, level shifters, isolation cells etc.

**Keywords :** ASIC, Design Optimization, High- Performance, Low-Power

## I. INTRODUCTION

With the growing use of portable and wireless electronic systems, reduction in power consumption has become more and more important in today's VLSI designs. The rapid progress in semiconductor technology implies increased chip density and frequency of operation, making power consumption in a device a major concern. There is almost no design today, where low power is not a concern. Reducing power is an issue which can be tackled on many levels, from the system design to the most fundamental implementation techniques. One of the major advantages of ASICs compared to other implementation methods is the power advantage. A dedicated ASIC will have a significantly better power-performance product than a general purpose processor or regular fabrics such as FPGAs.

The requirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design. In this paper, we discuss technology, circuit and optimization techniques to improve the power dissipation. We focus on the issue of pushing ASIC performance in a power envelope by exploiting the use of multiple supply voltages (Vdd) and multiple device thresholds (Vth). The use of multiple supply voltages presents some unique physical and electrical challenges.

## II. BACKGROUND

The methodologies which are used to achieve low power consumption in digital systems span a wide

range, from device/process level to algorithm level. Device characteristics (e.g., threshold voltage), device geometries and interconnect properties are significant factors in lowering the power consumption. Circuit-level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and design of bus structures. Finally, the power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task.

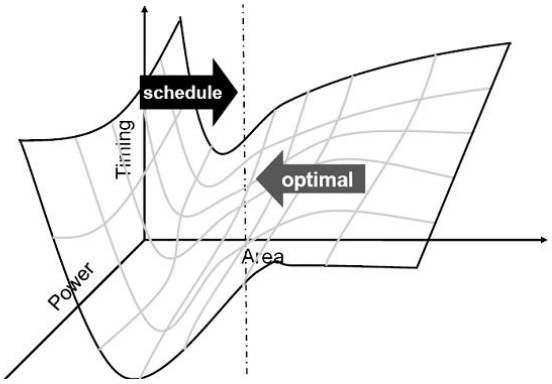



Fig. 1. 3-D view of design closure

The static power of a CMOS circuit is determined by the leakage current through each transistor. Lowered supply voltage reduces active power. However, supply voltage scaling increases the gate delays unless the threshold of the transistor is scaled down. This results in increase in leakage current. Therefore, there is a trade-off between leakage and active power for a given application. The total leakage current increases due to lowering of threshold, increased short-channel effects when reducing the channel length and reduction of oxide thickness.

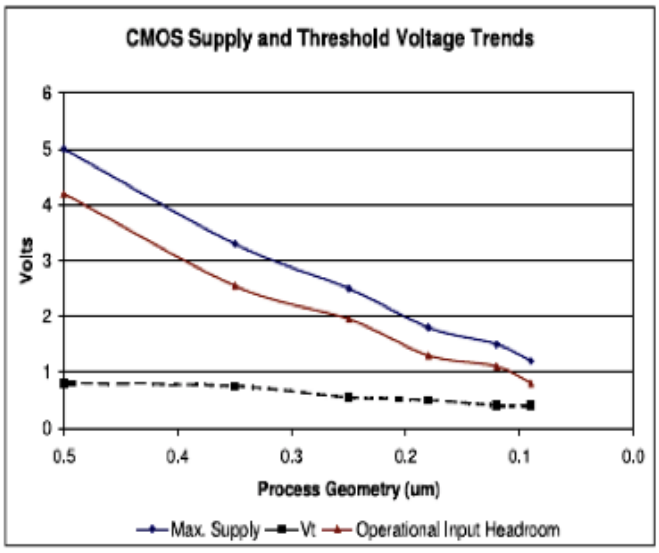



Fig. 2. CMOS operating voltage trends

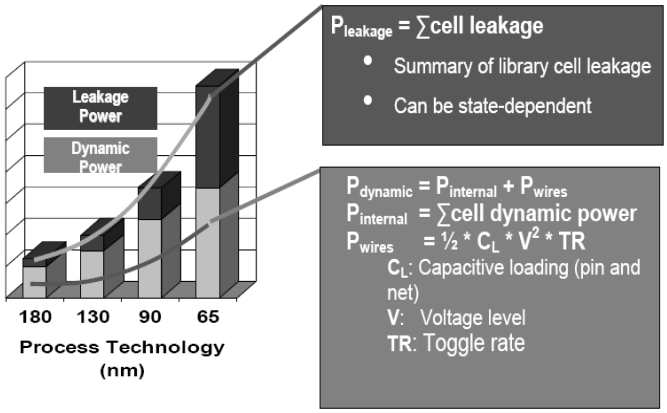



Fig.3. Process technology vs. Leakage and dynamic power

The design goal is simple: achieve the lowest possible power that will support the specified performance and functionality. Instead of using a single supply net and voltage to power the design, one of the technique is to assign separate power nets to different blocks and step the power net voltage down wherever the chip and block performance allows. This power domain technique is commonly referred to as multi-voltage design. This paper explains multi-voltage and multi-supply power domain concepts and special cells for power-domain design flow.

## III. POWER FUNDAMENTALS

There are basically two types of power consumption in CMOS

i. Dynamic Power
ii. Static Power (Leakage power)

A. Dynamic power dissipation

Dynamic power dissipation occurs in logic gates that are switching from one state to another. During the act of switching, any internal capacitance associated with the gate's transistors has to be charged, thereby consuming power. Of more significance, the gate also has to charge any external (load) capacitances, which are comprised of parasitic wire capacitances and the input capacitances associated with any downstream logic gates. Dynamic power dissipation may be reduced by minimizing the circuit activity and/or reducing the capacitance being driven and/or reducing the supply voltage. It consists of two main parts:

1) Switching power $P_{switching} = \alpha * C_L * VDD^2 * F$

Where, $\alpha$ = Switching activity constant, $C_L$ = output capacitance, VDD = Supply voltage F = Frequency.

2) Internal power($P_{Internal}$ )

Power consumed during short period when input signal is transitioning, during which both the PMOS and NMOS transistors can be conducting i.e. large current called "crowbar" or "short circuit" current flows from VDD to VSS.

$P_{Internal} = tsc * VDD * Ipeak * F$

$P_{Internal} = tsc * VDD * Ipeak * F$, Ipeak = Total internal switching current F= frequency

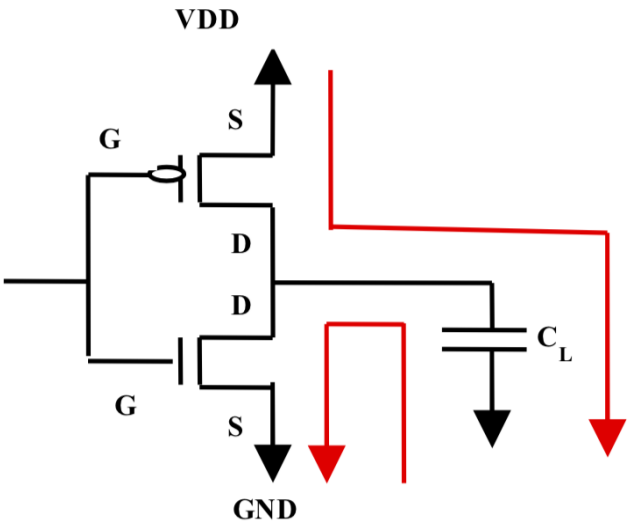



Fig. 4. Switching power dissipation

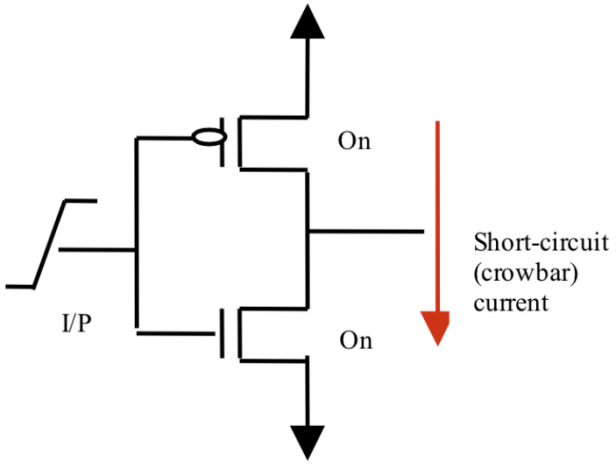



Fig. 5. Short-circuit power dissipation

B. Static power dissipation

Static power dissipation is associated with logic gates when they are inactive (static); that is, not currently switching from one state to another. In this case, these gates should theoretically not be consuming any power at all. In reality, however, there is always some amount of leakage current passing through the transistors, which means they do consume a certain amount of power.

Static power dissipation has an exponential dependence on temperature and also has an exponential dependence on the switching threshold of the transistors (Vt). In order to address low-power designs, IC foundries offer MTCMOS technologies that enable multiple Vt libraries. Each type of logic gate is available in two (or more) forms: with low-threshold transistors that switch quickly but have higher leakage and consume more power, or with high-threshold transistors that have lower leakage and consume less power but switch more slowly. The delay (switching time) associated with a transistor is affected by the switching threshold of that transistor (Vt) and the supply voltage to that transistor (Vdd).

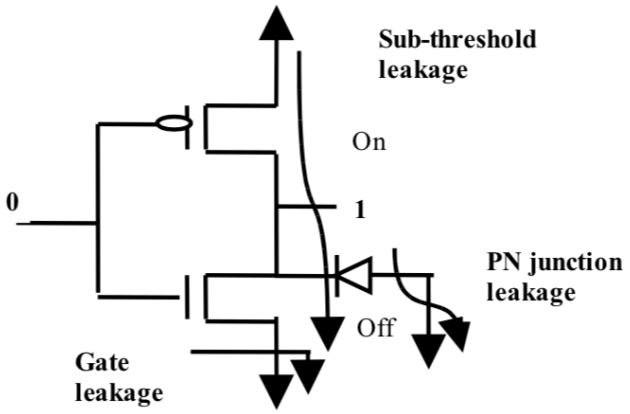



Fig. 6. Static power dissipation

Total Leakage = ISUB + IGATE +IGILD +IREV
ISUB = Sub threshold leakage
IGATE = Gate leakage
IGILD = Gate induced drain leakage IREV = Reverse bias gate leakage

Gate leakage current : The current that flows directly from the gate through the oxide to the substrate due to gate oxide tunnelling and hot carrier injection ·Sub threshold leakage current : The current that flows from drain to source of a transistor operating in the weak inversion region

Reverse bias PN junction leakage current : The current that results due to minority carrier drift and generation of electron/hole pair in the depletion regions.

The main source of leakage power is the sub-threshold leakage current. This is dependent on several factors with Vdd and gate threshold voltage being important. Leakage current reduces linearly with supply voltage. For example, to establish a design's lowest voltage bound, the designer can choose the lowest value at which a memory device operates while retaining data without completely switching off. The sub- threshold current is also dependent on the gate threshold voltage (Vth), which is generally controlled by adjusting the doping concentration under the gate. Gate threshold voltage can also be adjusted using gate oxide thickness variation and body back biasing. The Vth value influences the channel formation, which allows source to drain conduction when a gate voltage is applied. A lower Vth value has a faster transistor turn on response to the gate voltage and reduced delay at the cost of higher leakage when not switching.

## IV. MULTI-VOLTAGE CONCEPT

The multi-voltage concept is aimed at minimizing the supply voltage level wherever possible. Instead of a chip operating from a single uniform power supply, the multi-voltage device uses a range of supply voltages assigned to different areas with different levels. Taking this approach depends on being able to run different parts of the system at different clock speeds, which allows the power supply voltage to be reduced to match the needs of the lower-performance tasks. This is a linear trade- off of timing for a square-law power change.

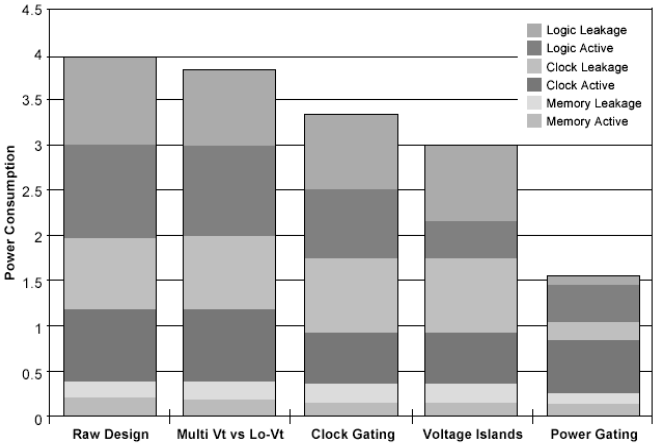



Fig. 7. Power savings during design and optimization

### A. Multi-Voltage Design Styles (Dynamic Voltage Scaling)

Dynamic voltage scaling allows the voltage level to be varied during chip operation to meet the dynamic performance needs of the system. Sleep mode may shut down one or more voltage areas. Standby mode may map to a low-voltage state. Full power mode is generally mapped to a full-voltage state for all of the voltage areas.

B. Dynamic power reduction techniques

Dynamic power is mainly a function of the supply voltage, output load (Cload), Frequency and switching activity of a cell and reducing any of the above component will result in the reduction of the dynamic power. There are several techniques as following:

1) Static Multi-Supply, No Shutdown

This design style supports the use of power domains running at multiple, fixed voltages, without shut down blocks. The blocks operate at different voltage levels, and those voltage levels are associated with specific logical partitions. Buffer- type LS cells are used to transit the signals across logic at the voltage interface.

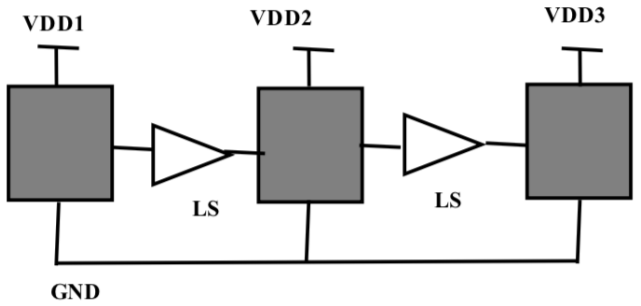



Fig. 8. Multi-voltage Design with Level Shifter

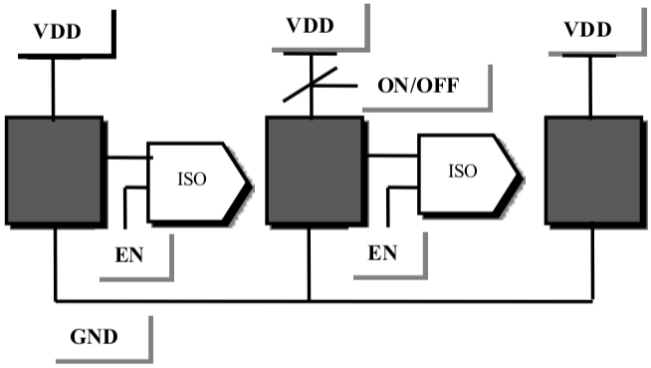



Fig. 9. Multi-Supply Design with Isolation cells

This design style may require ISO cells between the shut- down logic and the logic that remains active. MTCMOS (multi-threshold CMOS) devices can be used to shut down the blocks in multi-supply designs. These are switch cells distributed inside the design, dedicated to switching the power nets on and off.

3) Static Multi-Supply with Shutdown

This design style supports blocks operating at different voltage levels with shut down. This style requires both level shifting and signal isolation, which is accomplished using an ELS (level shifter with enable) cell. ELS cells allow the input side of the domain interface to be shut off, while driving either a steady logic '1' or '0' to the output side on a different voltage level. ESL is a combination of level shifter and isolation cells.

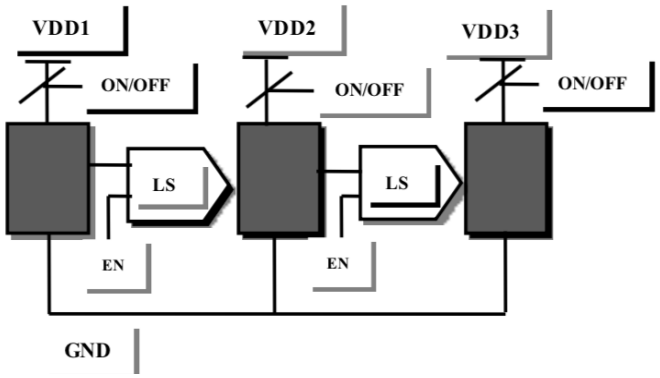



Fig. 10. Multi-Voltage Design with Enable level shifter

4) Clock gating

In digital design, clock gating is the back bone of low power design. Clock gating is used to reduce the switching activity of the clocks at selected flipflop's input and thereby reducing the dynamic power. It inserts combinational logic on clock path to conditionally stop the clock at flipflop's inputs.

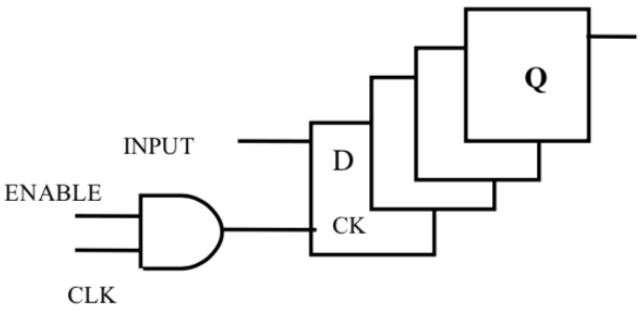



Fig. 11. Clock gating

## V. SPECIAL CELLS FOR LOW POWER TECHNIQUES

A. Level shifters

Purpose of this cell is to shift the voltage from low to high as well as high to low level and protect against sneak leakage paths. Selectively providing different voltages to different blocks depending on their performance requirement reduces the power. Here we apply lower voltages to the non-timing critical

blocks and creating voltage islands in the chip area. In this level shifters are needed at the block interface to convert the voltage levels for the receiving blocks. For signals going from low to high voltage block a low to high level shifter is needed and it should be placed in high voltage block & for signals going from high to low voltage block a high to level shifter is needed and it should be in low voltage block.

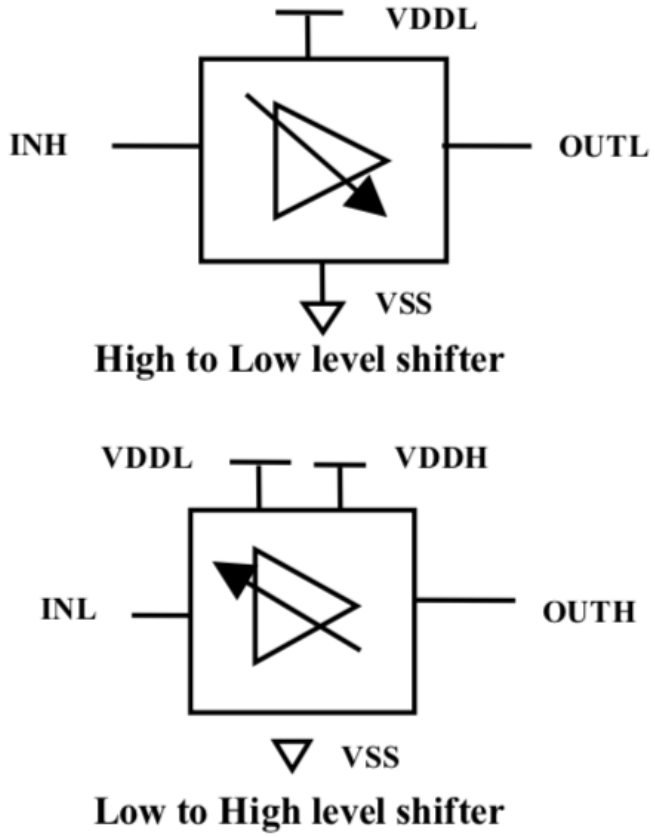



Fig. 12. Level shifters in design

B. Isolation cells

These are the special cells required at the interface between blocks which are shut down and always on. They clamp the output node to a known voltage. These cells need to be placed in an "always on" region only & the enable signal of the isolation cell needs to be "alwaya_on". The isolation cell prevents any unknown logic values to reach to the input of the always on block.

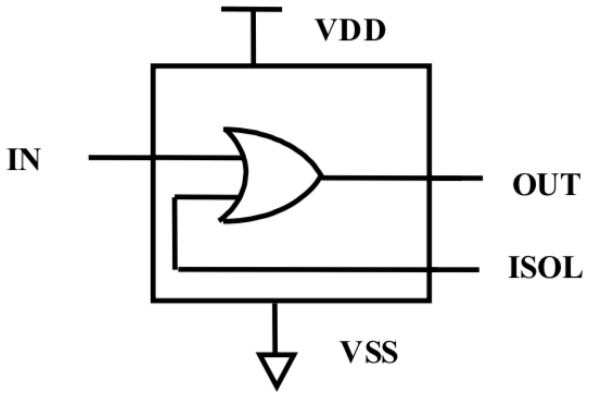



Fig. 13(a). Retain "1"

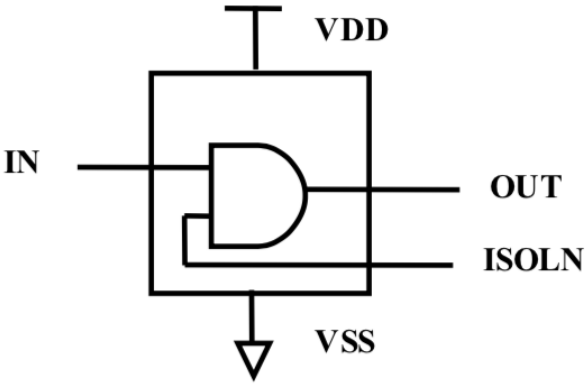



Fig. 13(b). Retain "0"

C. Retention registers

These cells are special flops with multiple power supply. They are typically used as a shadow register to retain its value even if the be "always_on". When design blocks are switched off for sleep mode, data in all flipflops contained within the block will be retain through retention register.

Full State Retention: Retaining the full state of the block - that is, replacing all registers with retention registers

Partial State Retention: Retaining the partial state means retaining only some of the internal state of the block to reduce the area.

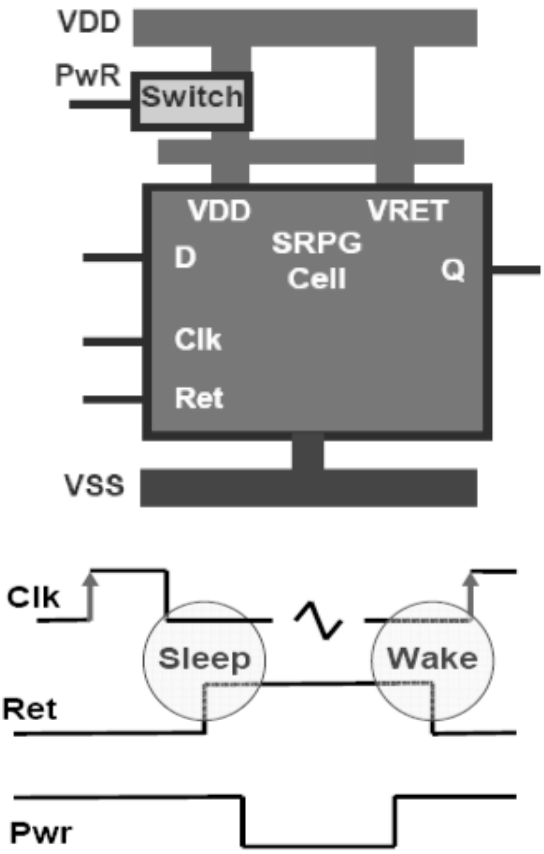



Fig. 14. Retention register

Power Cycle Sequence

For power-down, a specific sequence is generally followed:

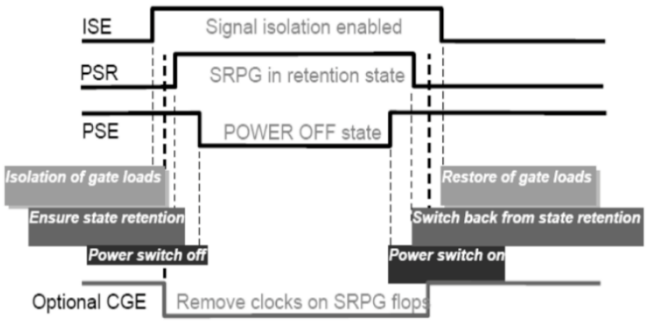



Fig. 15. Power up/down sequence

D. Power gating/MTCOMS switch

Power gating is the technique to reduce leakage power consumption. In this technique sleep transistor is used. In MTCMOS low-vt gates are used for speed and high-vt gates are used for low leakage. A sleep transistor is either PMOS or NMOS high VT transistor and is used as a switch to shut off the power supplies to parts of a design in standby mode. The PMOS sleep transistor is used to switch VDD supply and hence is called as a "Header Switch" & the NMOS sleep transistor controls VSS supply and hence is called as a "Footer switch".

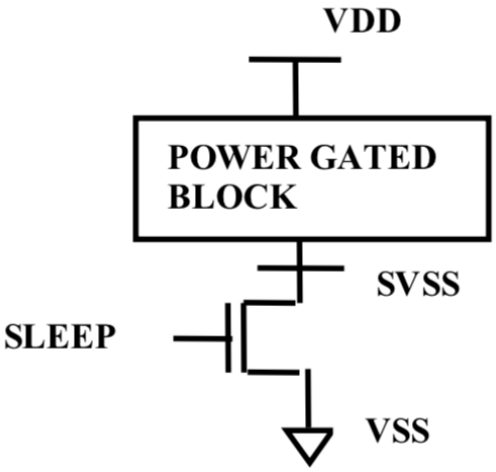



Fig. 16(a). Header switch

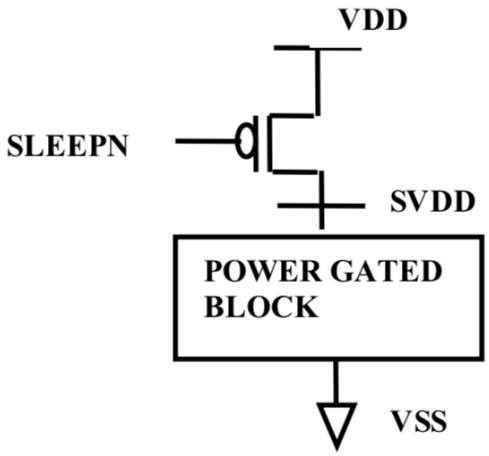
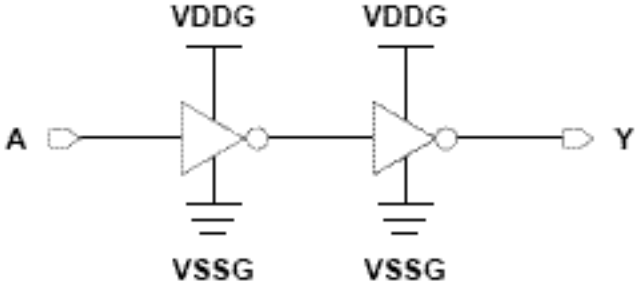



Fig. 16(b). Footer switch

E. Always on Cell

Always on cells are always on cells used to provide long wire buffering and load distributing for the control signals like SLEEP and RETN in the power gated domain during the power down state.



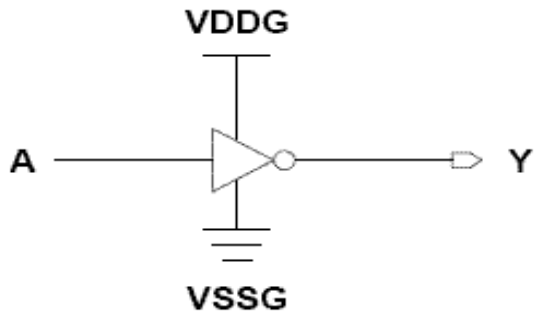



Fig. 17. Always on cell

STATIC (LEAKAGE) POWER REDUCTION TECHNIQUES

There are several techniques for the static power reduction:

1) Multi VT, Power gating, Variable threshold CMOS (VTCMOS)
2) For multiVT design we can use the low VT cells in the timing critical paths for less delay while highVT cells can be used in non critical timing paths to reduce the leakage.
3)

In VTCMOS we are applying different voltage to the body of the standard cell and changes the threshold voltage, the body bias voltage is applied to increase the Vt, which reduces the leakage. It requires special FILLBIAS cells providing supply to the n-well/p-well of the standard cell.

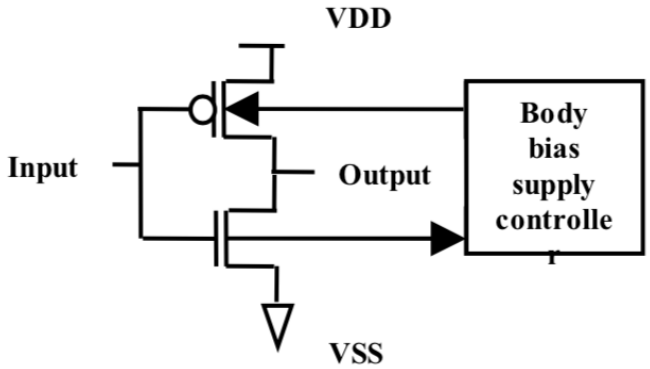



Fig. 18. VTCMOS

## VI. CONCLUSION

The need for low-power design is also becoming a major issue in high-performance digital systems. As CMOS technology is scaled to nanometer ranges, the power consumption caused by leakage current is becoming a significant part of overall power consumption. The leakage in deep submicron region is an important issue due to lowering of threshold voltage, reduction in channel length and oxide thickness. This paper has presented the description of the new methodology and various techniques for the development of low power design and to push the ASIC designs in low power envelope. Various sources of power consumption and design strategies to be introduced to reduce the power dissipation are discussed.

Every joule is scared, Every joule is great, If a joule is wasted, We all get quite irate....

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