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Minimization of Leakage Currents in Dram 4x4 Using SVL Technique

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ABSTRACT

In recent years, due to development of integrated circuits technology, power is being given comparable weight to area and speed considerations. The power consumed for any given function in any complementary metal-oxide-semiconductor (CMOS) circuit must be reduced for either of the two different reasons. One is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an Integrated Circuit (IC) chip. Any amount of power dissipation is worthwhile as long as it does not degrade overall circuit performance. The other reason is to save energy in battery operated instruments like in electronic watches where average power is in microwatts.

Low power is the major issue not only in portable devices but also in non-portable devices. So, it is apparent that one has to resolve low power design methodologies for the design of high throughput, low power digital systems. By using this SVL technique using DRAM we are going to reduce the leakage currents and also improves the performance of the circuit.

Keywords : Low Leakage Power, High Performance, Self-Controllable Voltage Level Technique, Low Cost, Low Power.

I. INTRODUCTION

DRAM designers have opted for a multiplexed addressing theme. during this model the lower and higher halves of the address words square measure given consecutive on one address bus. This approach reduces the quantity of package pin and has survived through the following memory generation. DRAMS [1]are usually made in higher volumes. Lowering the pin count reduces the value and size at the expense of performance. The presence of latest address word is declared by raising variety of strobe light signals. Raising the row access strobe light signal assert the MSB a part of the address is gift on the address bus, which word secret writing method are often initiated. The LSB a part of the address is applied next and also the column access strobe light signal is declared. Still leak current might cause some power consumption even within the sleep mode. If the circuit may well be designed such there's terribly low leak current during this mode, then the lifespan of the transportable application can increase dramatically. the world

potency of the memory array, i.e., the quantity of hold on knowledge bits per unit space, is one among the key criterion that verify the storage capability and, hence, the memory value per bit. Another necessary issue is that the access time, i.e., the time needed to store and/or retrieve a selected knowledge bit within the memory array. The interval determines the memory speed, that is AN necessary performance criterion of the memory array. Finally, the static and dynamic power consumption of the memory array could be a important issue to be thought of within the style, as a result of the increasing importance of low-power applications. within the following, we'll investigate differing types of MOS memory arrays and discuss well the problems of space, speed, and power consumption for every circuit sort Read-write (R/W) memory circuits, on the opposite hand, should allow the modification (writing) of knowledge bits hold on within the memory array, yet as their retrieval (reading) on demand. this needs that the information storage operate be volatile, i.e., the hold on knowledge square measure lost once the facility provide voltage is turned off. The read-write memory circuit is often known as Dynamic Random Access Memory (RAM), principally because of historical reasons. Dynamic random access memory (DRAM) is the foremost common reasonably random access memory (RAM) for private computers and workstations. The network of electrically-charged points during which a laptop stores quickly accessible knowledge within the style of 0's and 1's is termed memory. Random access means the laptop processor will access any a part of the memory directly instead of having to proceed consecutive from some foundation. DRAM is dynamic therein, not like static RAM (SRAM), it must have its storage cells fresh or given a replacement electronic charge each few milliseconds. That DRAM is way cheaper per cell and since every cell is incredibly straightforward, DRAM has abundant larger capability per unit of surface than SRAM. within the implementation of 3T DRAM victimisation 3 NMOS money supply, M2 and M3. money supply and money supply square measure the access junction transistor and by victimisation these management the scan and write operation. If the write operation is performed therein time money supply is on and money supply is off. the information is hold on by charging the electrical condenser. If the scan operation is performed therein time money supply is off and money supply is on, than the information additionally|is additionally} on the market therein time also. once the 3T DRAM is implementing with Self- governable Voltage Level technique one electrical converter is employed within the higher half and also the lower half. If we tend to add this electrical converter within the circuit then the leak power is a smaller amount as compared to traditional 3T DRAM.. By victimisation microwind two package, layout diagram have done. during this the word and VDD lines square measure enforced in poly, the affiliation to the MOSFETs happens once poly runs over the active n+ space transistors increase delay considerably and will limit the quality of the approach.

In standard CMOS electrical converter if input is given low as compared to threshold voltage, then at a similar time PMOS activates and NMOS turns off. And if input is given high at the gate terminal as compared to threshold voltage, then at a similar time PMOS turns off and NMOS activates.

II. EXISTING SYSTEM STACKING TECHNIQUE

A technique for leak power reduction is that the stack approach, that forces a stack result by breaking down AN existing semiconductor into 2 [*fr1] size transistors. Figure shows its structure. The leakage current flowing through a stack of series connected transistors reduces leakage currents when more than one transistor of the stack is turned OFF. Sub threshold leakage is exponentially related to the threshold voltage of the device and the threshold voltage changes due to body effect. From these two

facts, one can reduce the sub-threshold leakage in the device by stacking two or more MOS transistors serially. Stacking Technique is shown in figure 1.

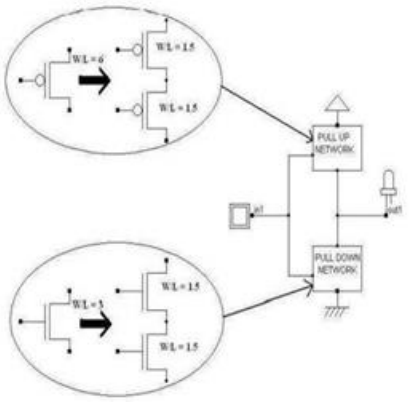


FIG 1: STACKING TECHNIQUE

From figure 2, MOS transistors (P1 and N2) are stacked in different ways. The MOS transistors above the lowest MOS transistor will experience a higherthreshol d voltage due to the difference in the voltage between the source and body. Also, the Vdd of the higher MOS transistor is decreased, since the intermediate node has a voltage above the ground. This result in reduction of DIBL affects hence better leakage savings. The two transistors square measure turned off along, evoked reverse bias between the 2 transistors ends up in sub threshold leak current reduction. However, divided

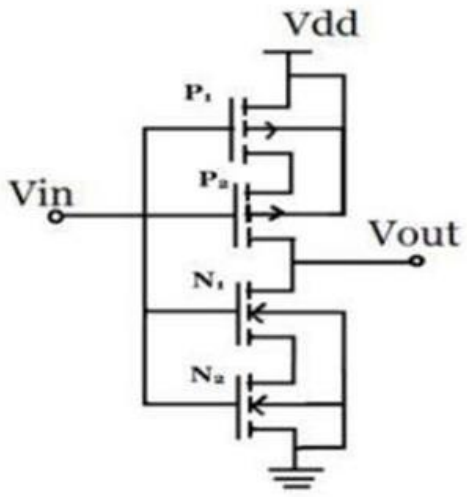


Fig 2: INVERTERS USING STACKINGMETHOD

The leak current flowing through a stack of series connected semiconductors reduces leak currents once over one transistor of the stack is turned OFF. Sub threshold leak is exponentially associated with the edge voltage of the device and also the threshold voltage changes because of body result. From these 2 facts, one will scale back the sub-threshold leak within the device by stacking 2 or a lot of MOS transistors serially.

From figure 2, MOS transistors (P1 and N2) square measure stacked in numerous ways that. The MOS semiconductors on top of the bottom MOS transistor can expertise a better threshold voltage because of the distinction within the voltage between the supply and body. Also, the Vdd of the upper MOS semiconductor is diminished, since the intermediate node incorporates a voltage on top of the bottom. This end in reduction of DIBL affects thus higher leak savings.

DRAM:

Random access memory may be a sort of memory that offer the direct access to any computer memory unit on the chip and computer memory unit addressing suggests that the contents of any computer memory unit may be browsed or written while not reference to the bytes before or once the browse and write speeds. RAM places a crucial role in several systems like laptop and communication systems and there are several applications code used for implementing the digital circuits of RAM. It takes not to jot down a computer memory unite than it will to browse one. RAM (also named as read-write memory) is taken into account store. Laptop and different sorts of system need the permanent or semi- permanent storage massive for giant for big amounts of binary Memory is that the portion of a system used for storing binary knowledge in large quantities. Memory unit may be a device to that binary data is transferred for storage and from that data is accessible once required for process. Binary data received from the data input device is keep in memory and data and

magnetic at intervals every class area unit a spread of memory varieties, usually the semiconductor reminiscences area unit used for smaller capability and quicker access applications. One bit DRAM cell is shown in below figure 3.

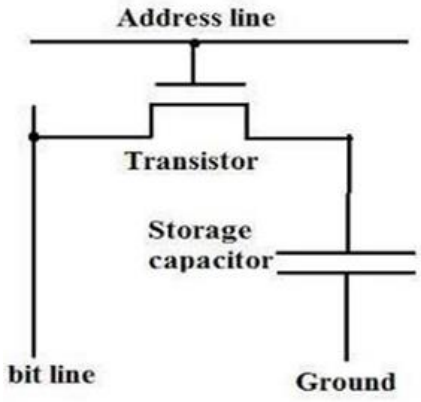


Fig 3 : One-bit DRAM cell PROPOSED METHOD SVL TECHNIQUE

Self- Controllable-Voltage level circuit (SVL) has been developed, that not solely reduces outpouring power however conjointly retains information throughout stand by amount. Self-Voltage Level (SVL) manageable switch could be a technique that permits full provide voltage to be applied in active mode, and reduced provide voltage in inactive mode. Conjointly this seems to be significantly promising for reducing gate / sub-threshold outpouring currents.SVL technique is shown in figure 4.

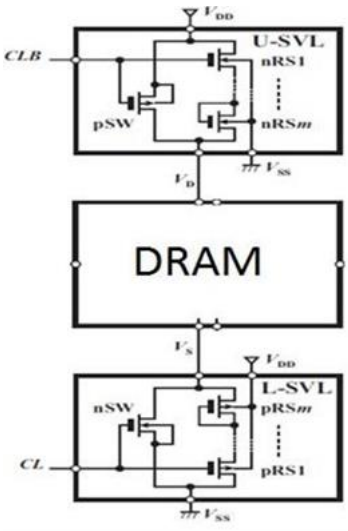


Fig 4: SVL CIRCUIT

Here self-controllable switch will be used either at the top side of the quality cell to cut back provide voltage (USVL scheme) or at the lower finish of the cell to boost the potential of the bottom node (LSVL scheme). From fig the higher SVL (U-SVL) circuit contains 2 or a lot of PMOS transistors connected nonparallel and one NMOS in parallel of those series PMOS transistors. Similarly, the L-SVL circuit contains 2 or a lot of NMOS transistors connected nonparallel and one PMOS in parallel of those series NMOS transistors. While the load circuit is active, the U-SVL and L-SVL circuits will provide a most provide voltage VDD and a minimum ground-level voltage VSS =0. Thus, the in operation speed of the load circuit will be maximized. When the load circuit is in stand-by, the U-SVL and 4L-SVL circuits severally generate a rather lower provide voltage sexually transmitted disease (VDD-Vna comparatively higher "ground-level" voltage VS (=Vp > 0V), wherever Vn and Vp area unit the entire voltage drops of all NMOS and every one PMOS severally. Thus, the back-gate biases.

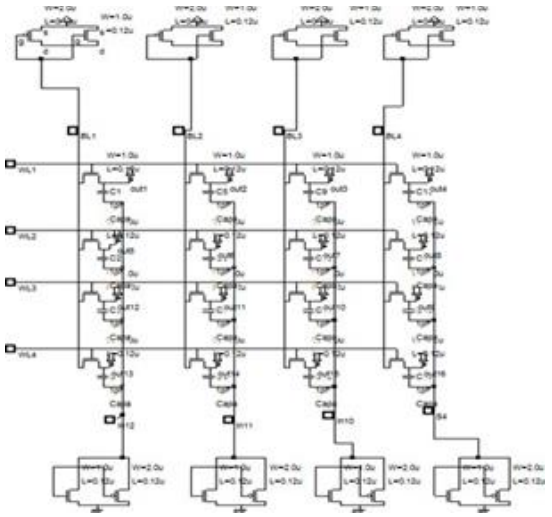


Fig 5 : Schematic diagram DRAM4x4 using SVL technique

From figure 5,VBGS (i.e., supply voltages (Vs)) of each the "cut-off" PMOSFETs and therefore the NMOSFETs within the stand-by load circuit square measure enlarged and square measure given by Vn

and VP severally. The rise in VBGS can increase the Vth of the "cut-off" MOSFETs. Therefore, the escape currents of the "cut-off" MOSFETs decrease.

The effective gate length of each the n-MOSFET and p- MOSFET was zero.13 μm, the edge voltage (Vthn) of the n-MOSFETs dsnwas zero.21 V, and therefore the threshold voltage (Vthp) of the p-MOSFETs was -0.25

V. whereas gate voltage (Vg) of the stand-by electrical converter shown Fig. 1(a) is unbroken at "0", the P-MOSFET (p- MOS) is turned on whereas the n-MOSFET (n-MOS) is turned off. Once management signal (CL) activates n-SW1 and turns off p-SW, VDD is provided to the electrical converter through m n-SWs. Thus, a drain-to-source voltage (Vdsn), that is, a drain voltage (Vd) of the "off n-MOS", may be expressed as Vdsn = VDD — mv, wherever v may be a drop of the one n-SW and Vdsn may be modified by varied m or v (or both). Decreasing V by increasing mv can increase the barrier height of the "off n-MOS"; that's, it'll decrease the drain induced barrier lowering (DIBL) and, consequently, increase Vthn. This ends up in a decrease within the sub threshold current of the n- MOS (Istn); that's, the escape current through the inverter decreases.

III. SOFTWARE TOOLS USED DSCH (DIGITAL SCHEMATIC)

The DSCH2 program could be a logic editor and a machine as shown in fig 6. DSCH2 is employed to validate the design of the logic circuit before the electronics style is started. DSCH2 provides a easy atmosphere for ranked logic style, and quick simulation with delay analysis, that permits the look and validation of advanced logic structures. Some techniques for low power style square measure represented within the manual. DSCH2 additionally options the symbols, models and assembly support for 8051 and 18f64. DSCH2 additionally includes associate interface to SPICE.

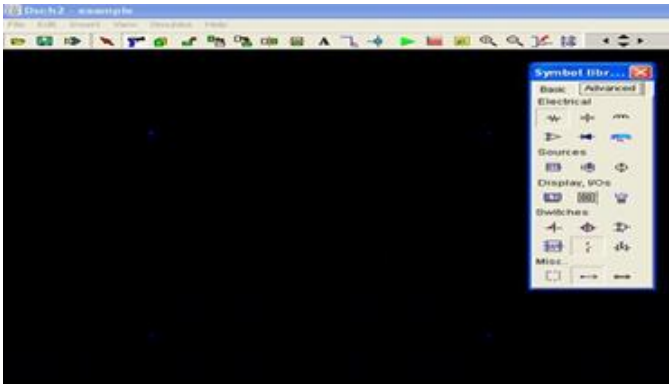
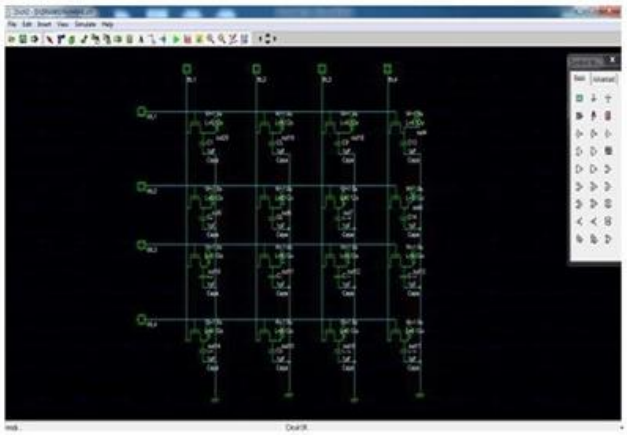


Fig 6 : DSCH at initial stage

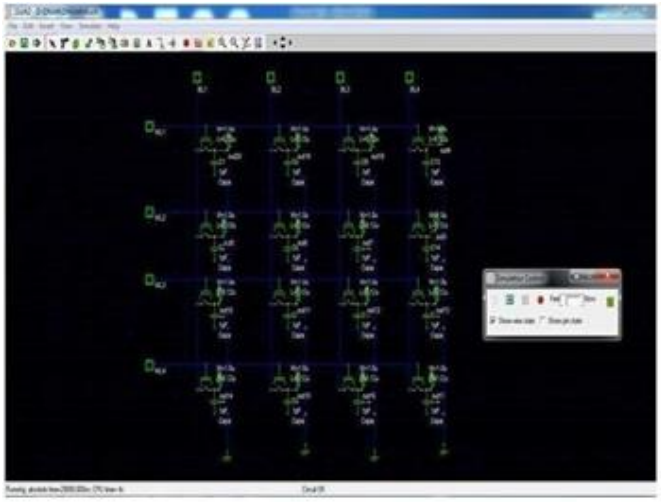
MICROWIND

OUTPUTS:

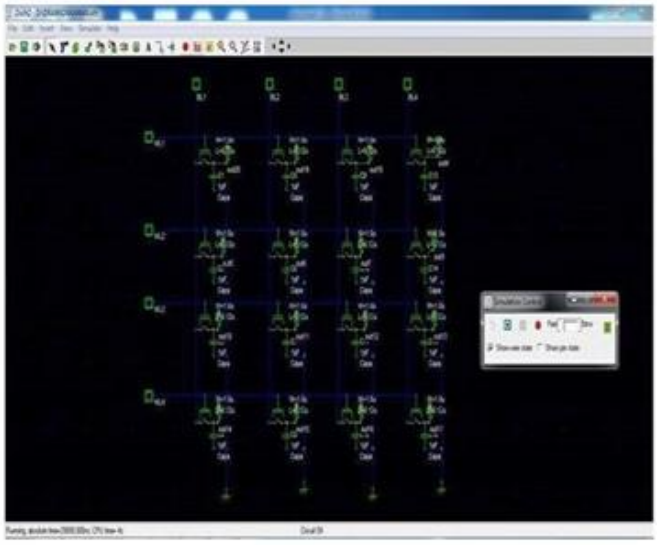
Schematic Diagram of DRAM 4x4 inDSCH:



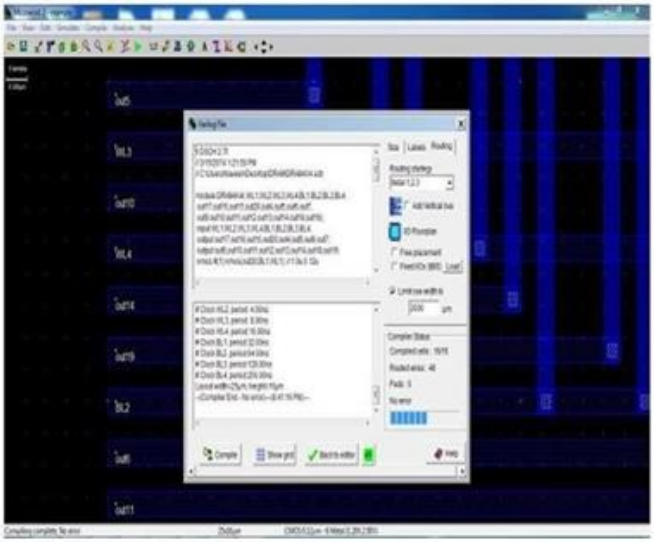
COMPILATION OF LAYOUT OF Dram 4x4:



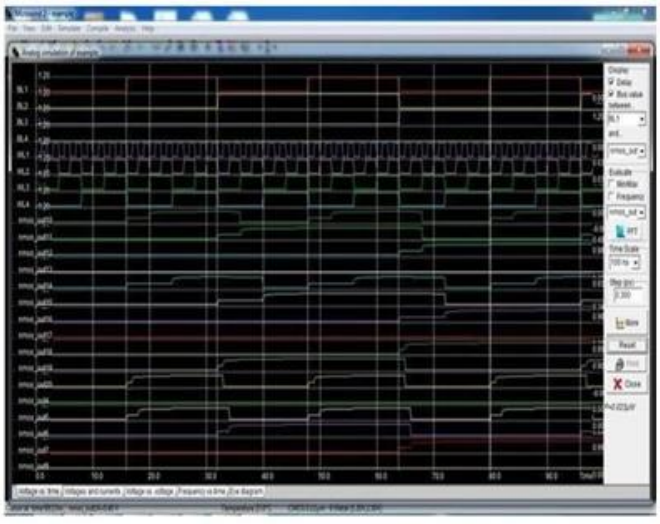
SIMULATION OF DRAM 4X4:



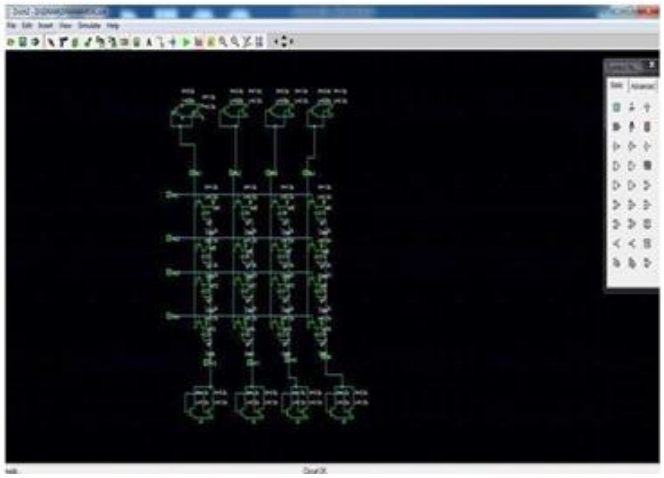
Compilation of DRAM 4x4:



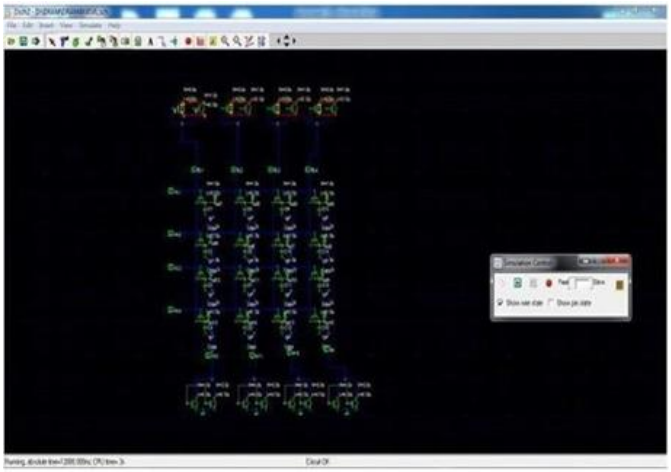
Power Dissipation waveform of DRAM 4x4:



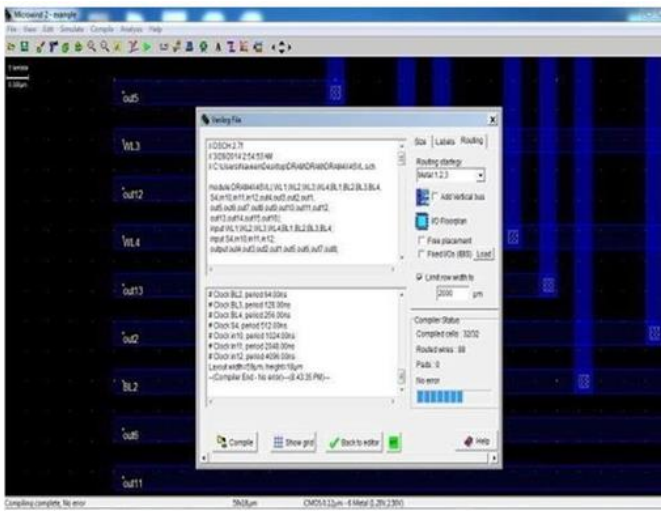
SCHEMATIC DIAGRAM OF DRAM 4x4 with SVL:



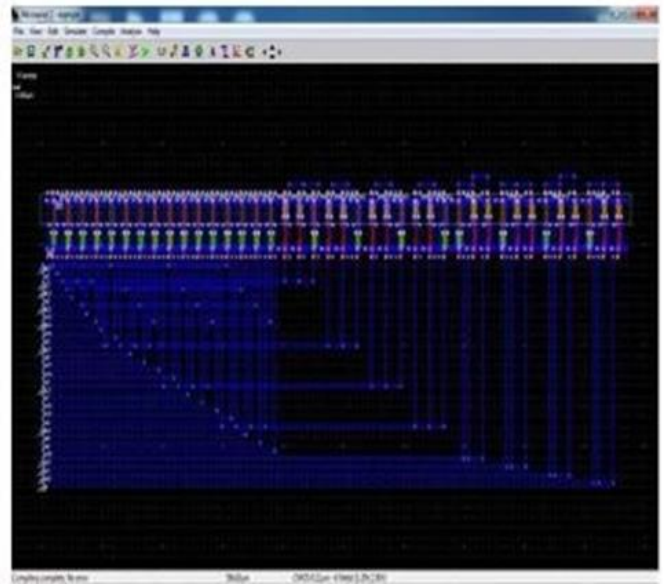
SIMULATION OF DRAM 4x4 USING SVL:



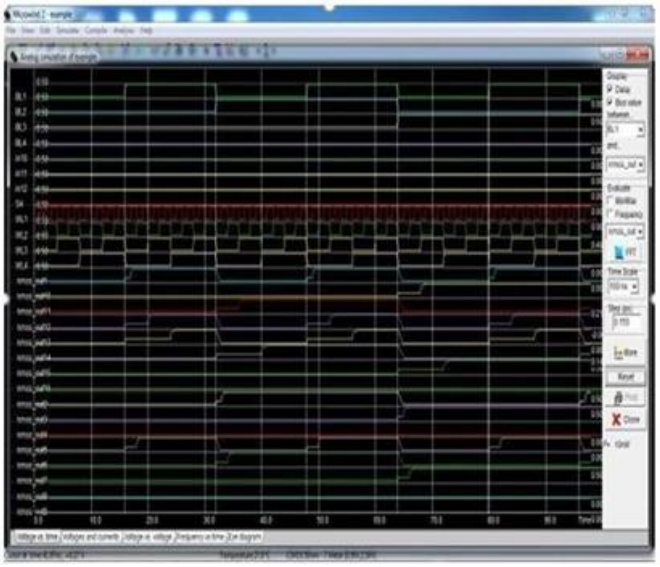
COMPILATION OF DRAM 4X4 USING SVL:



LAYOUT DIAGRAM OF DRAM 4X4 USING SVL:



OUTPUT WAVEFORMS OF DRAM 4X4 USING SVL:



IV. CONCLUSION

In this project, we represented DRAM 4X4 with self-controllable voltage level. The implementation of DRAM 4×4 with self-controllable voltage level. The implementation of DRAM 4×4 with self-controllable voltage level gives the advantageous of reduction of leakage current up to more than 50%. The layout of Simulation is done by using a DSCH2 and microwind2. VDD is used in this 1.2v. Here 50 nm technology is used. In this project we have shown that the previously introduced SVL technique can be employed to effectively combat the leakage current that will be rapidly increasing as CMOS circuits continue to scale down.

V. FUTURE SCOPE

DRAM 4x4 with self-controllable voltage level technique is to reduce the leakage currant in DRAM memory. In future by using 22nm technology we can reduce more leakage current and also the power consumption of the circuit. Beyond 45nm technology, it is not possible to control the leakage currents. So by using FINFET technology we can control more leakage currents without using additional circuitry.

VI. REFERENCES

[1]. Frangois Odiot, Hugues dry, “New check Structure for prime Resozution discharge Current And Capacitance Measurements In CMOS Imager Appncations,” Proc. 1EEE 2004 Int. Conference On electronics check Structures, Vol 15, March 2004.

[2]. Satoshi Kurihara, Yanuar Z. Arief, Takumi Tsurusaki, Shinya Ohtsuka, “Construction Of Remote watching System For Separative measure Of discharge Current Of Out door Insulators,” Proceedings Of The fifth Lntemarional Confere.

[3]. Sandeep K. Shukla, R. Iris Bahar (2004). Nano, Quantum and Molecular Computing. Springer, p. 10 and Fig. 1.4, p. 11

[4]. Ashish Srivastava, Dennis Sylvester, David Blaauw (2005).Statistical Analysis and improvement For VLSI: temporal order and Power. Springer, p. 135

[5]. Galup-Montoro & Schneider megacycle (2007).MOSFET modeling for circuit analysis and style. London/Singapore: World Scientific, p. 83

[6]. Norbert R leader (1995).Electronic circuits: analysis, simulation, and design. Englewood Cliffs, NJ : Prentice Hall, pp. 315-316

[7]. A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, “A 90nm high volume producing logic technology that includes novel 45nm gate length strained semiconducting material CMOS transistors,” IEDM Technical Digest, pp. 978-980, 2003.

[8]. K. Bowman, L. Wang, X. Tang, and J. Meindl, “A circuit-level perspective of the optimum gate chemical compound thickness,” IEEE Trans. lepton Devices, vol. 48, no. 8, pp. 1800–1810, Aug. 2001.

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