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Performance Optimization of Low Leakage and Low Power 8T SRAM Cell

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ABSTRACT

With CMOS technology scaling down to 65nm or below, Leakage current and leakage power and sub-threshold leakage current has been primary challenges for SRAM design and fabrication. In this paper, we introduce a low leakage and low power 8T SRAM cell. This cell is very essential for low power applications. The proposed 8T SRAM cell has been improve the dynamic current and reduces the leakage current and leakage power. To determine the performance of 8T SRAM cell under 45nm technology, we need to orCad pSpice A/D tool. This tool is very essential for transient analysis to calculate the yield accurately and efficiently. This paper presents the analysis and simulation of 8T SRAM cell with different parameters such as leakage current, leakage power and dynamic current.

Keywords: SRAM, Leakage Current, Dynamic Current, Leakage Power, Word Line, Bit Line

I. INTRODUCTION

With CMOS technology scaling down to 65nm or below, Leakage current and leakage power and sub-threshold leakage current has been primary challenges for SRAM design and fabrication. It is clear that the future of the technology of materials should show greater mobility, greater stability, and scalability against the process and reduces the effects of variations in short the channel effects. Because of the scale of the deep submicron processes in memory, the variations in temperature, supply voltage, and changes in the process put the most important challenges for the future of the design of the memory and the device to high performance [1-3]. As the lower supply voltage can result in more on saving energy, also has a negative effect on SRAM bits-cell performance. As a reduction of the supply voltage can reduce the noise margin and the performance of the device. In order to make faster SRAM, transistor threshold were lowered that also helps to reduce the leakage currents. These leakage currents can consume a lot of power and reduce the battery life considerably, a serious curse for multimedia applications portable [4-5].
As the density of SRAM cells on chips increase, the concerns toward excessive energy consumption continues to increase, in particular, the wireless sensors and mobile applications. However, the voltage and scaled to the fight against the increase in power and other problems, for example, the low level of noise margins of stability in conventional 6T SRAM cells [6-7]. A solution that involves additional transistors 8T has been designed to reduce the energy consumption and to reduce these negative effects on the performance of the cell. This paper presents information on how to check the leakage current, the loss of power and how to optimize the dynamic power in SRAM cell [8]. In Section 2 we shows that the problems of 6T and 7T SRAM cells. In Section 3 we described the proposed 8T SRAM cell. In Section 4 we described the simulation results. Final Section presents the conclusion of this paper.

II. METHODS AND MATERIAL

A. PROBLEMS 6T AND 7T SRAM CELLS

The problem associated with bulk MOSFET based 6T SRAM cell during read operation is, when the WL is turned ON, it raises the output voltage at node that stores “0”, which could turn ON the opposite inverter pull down transistor, when this happens the voltage at node which stores “1” will be reduced. This voltage may drop little, but it should not drop below the threshold voltage. If it drops below the threshold voltage of MOSFET, it

leads to read destructive operation. Due to this stability of the 6T SRAM cell will be degraded. The operation of writing is accomplished by forcing one bit line low while other bit line remains at about ,which could leads to enhancement in dynamic power consumption. With technology scaling, in the new coming manufacturing process the operating voltage and threshold voltage decrease and it demolishes the stability of the SRAM cell. Due to the direct paths between bit lines to the storage nodes, the data stored in conventional SRAM cell easily deteriorated by the external noise. Based on the above reasons bulk MOSFET based 6T SRAM cell is not suitable for real time video applications [9]. Hence we require a new design for high stability, low dynamic and leakage power.

SRAM stability is characterized by the data retention stability through a read operation. In 6T SRAM cell, the data storage nodes are accessed directly through the access transistors connected to the bit lines. The storage nodes are interrupted due to the voltage division between the cross-coupled inverters and the access transistors during a read operation. There are exact constraints on the sizing of transistors to be able to keep the data stability and functionality of a 6T and 7T SRAM cells. The stability of a 6T and 7T SRAM cells are characterized by the ratio (β) of the size of the pull-down transistors (M4 and M6) to the access transistors (M1 and M2). Higher β leads to enhanced data stability at the expense of increased leakage power and larger cell area. To overcome the problem of destruction of data storage during the read operation, we proposed 8T SRAM cell.

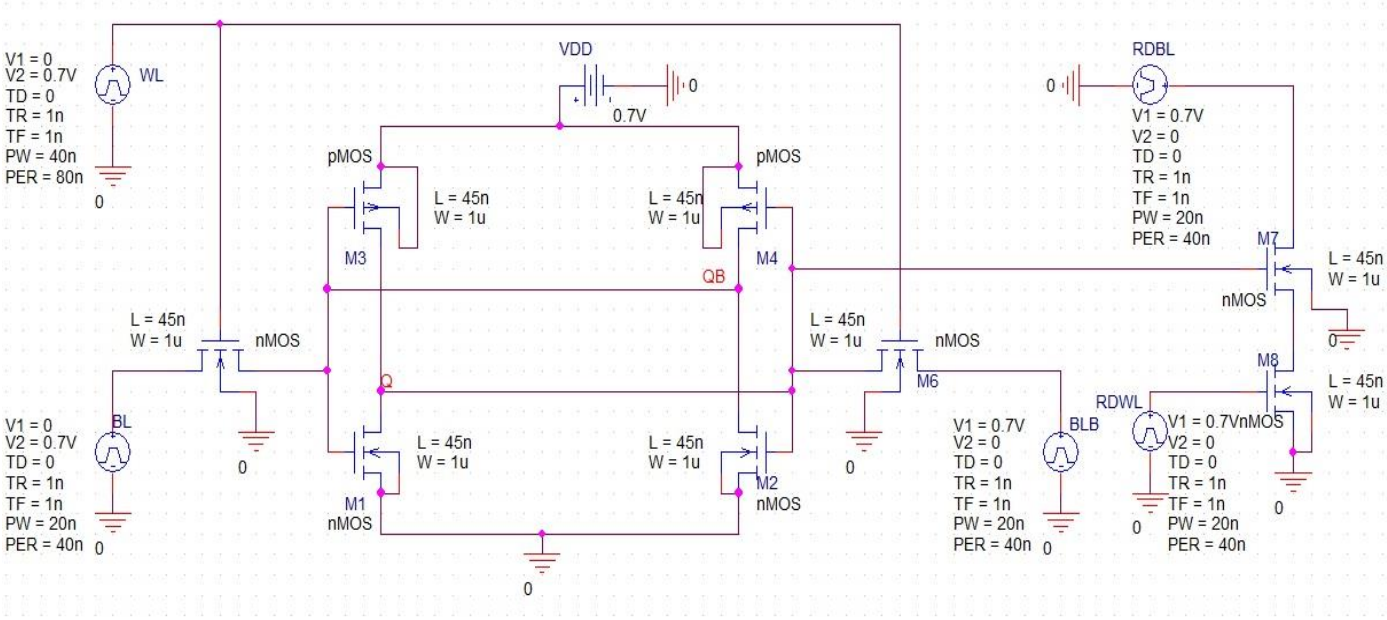

Figure 1: The Schematic of 8T SRAM Cell

B. PROPOSED 8T SRAM CELL

The SRAM cell consists of two cross coupled inverters and two n-channel access transistors shown in Fig.2; these cross coupled inverters are called as a latch. The latch has four transistors; each bit in a SRAM is stored on four transistors. The drain terminal of n-channel access transistors are connected to the latch inputs and source terminals are connected to the bit line and bit line bar. The additional n-channel transistor M7 is connected to the storage node Q and M8 transistor are connected to the Read word and read bit lines (RDWL and RDBL).

SRAM stability is characterized by the data retention stability through a read operation. In 6T SRAM cell design, the data storage nodes are accessed directly through the n-channel access transistors connected to the bit line and bit line bar. The storage nodes are cut off due to the voltage division between the latch and the n-channel access transistors during a read operation.

Separation of data retention component and data output component means there will be no relationship between I_{cell} and read SNM. To overcome the problem of destruction of data in 6T and 7T SRAM cells during the read operation [10], we implement the 8T cell, for which

separate word lines and read/write bits are used to separate the output data and the data retention element. In turn, the implementation provides a cell read disturb free operation. As shown in fig.2, 8T SRAM cell has 30% more area than a conventional 6T SRAM cell. The 30% area overhead is composed of not only the two added n-channel transistors but also of the contact area of the word-line for write (WWL) operations. While WL contact area is conventionally assigned to the boundary line between two SRAM cells, in this 8T SRAM cell the WWL contact area is assigned to within a cell.

III. RESULTS AND DISCUSSION

Simulation Results

The proposed 8T SRAM cell has been designed using orCad pSpice A/D tool; all the waveforms have been generated on pSpice A/D simulator. Clearly we see that the proposed 8T SRAM cells show good performance in terms of dynamic current, dynamic power and improve the leakage current, leakage power as compared with the 6T and 7T SRAM cells. Figure 2 shows the waveform for write operation in 8T SRAM cell. In the waveform BL and BLB refers to bit and bit line bar respectively. The voltage level on every source has been kept at 0.7V. In Figure 2, when write word line (WWL) is high the output states of Q and QB change according to the BL and BLB and when WWL goes low the SRAM retains the data.

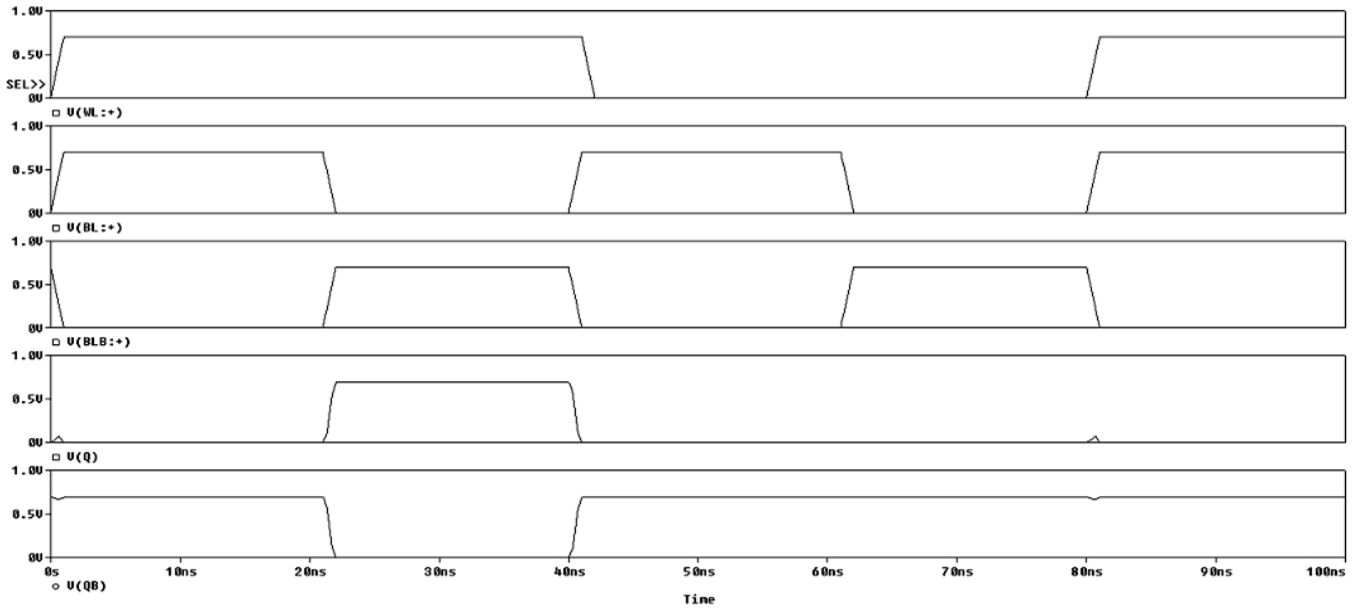

Figure 2: The waveform for write operation in 8T SRAM cell

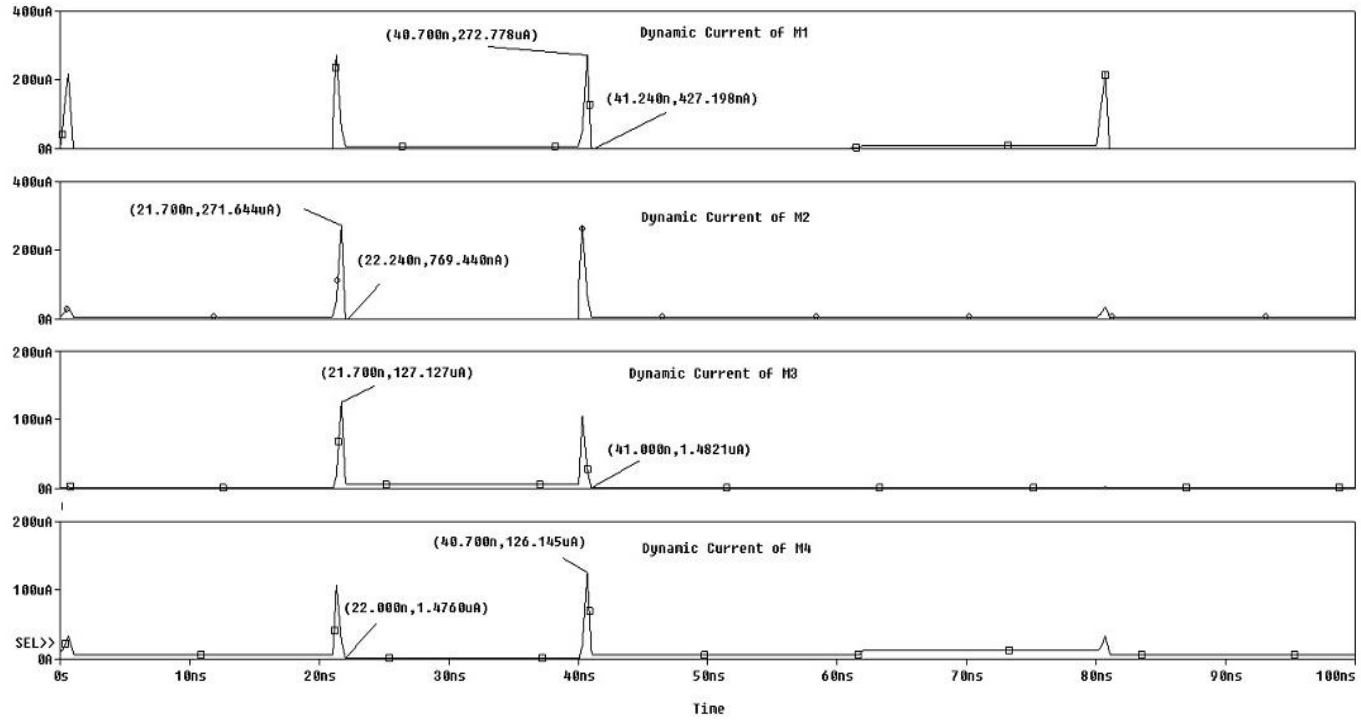

Figure 3: The waveform for dynamic current in 8T SRAM cell

Figure 3 shows that the waveform for dynamic current of latch transistors in 8T SRAM cell. This latch has two nMOS (M1 and M2) and two pMOS (M3 and M4) transistors. The dynamic current of M1, M2, M3 and M4 transistors are 272.778µA, 271.644µA, 127.127µA and 126.145µA respectively.

Figure 4 shows that the waveform for leakage current in 8T SRAM cell. The leakage current of M1, M2, M3 and M4 transistors are 45.604nA, 89.619nA, 555.915nA and 552.501nA respectively. Figure 5 shows that the waveform for leakage power in 8T SRAM cell. The leakage power of M1, M2, M3 and M4 transistors are 9.374nW, 8.082nW, 25.600nW and 29.262nW respectively.

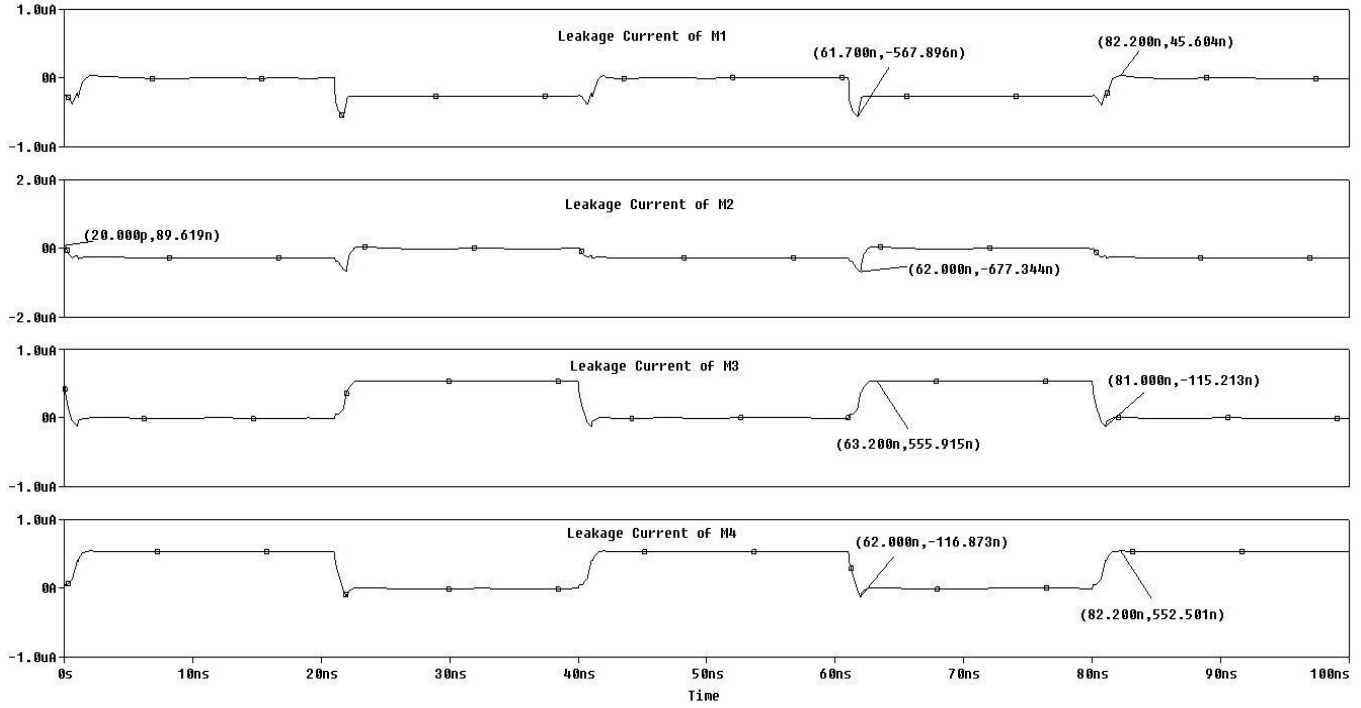

Figure 4: The waveform for leakage current in 8T SRAM cell

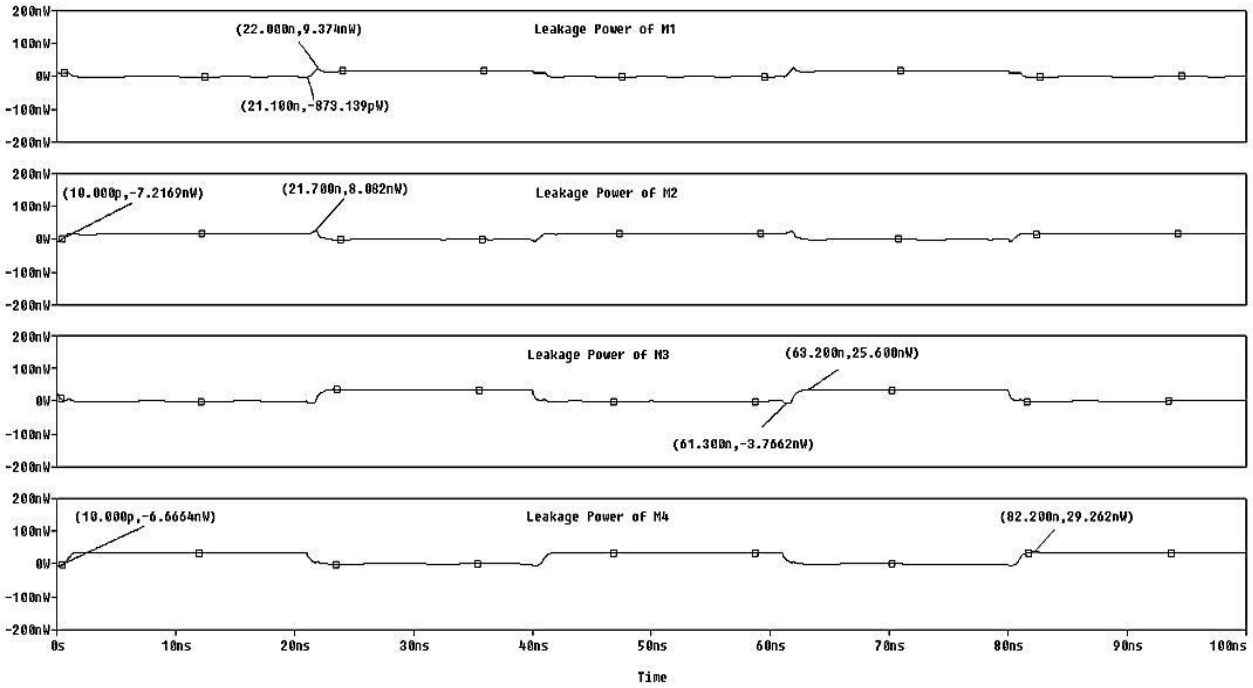

Figure 5 : The waveform for leakage power in 8T SRAM cell

IV. CONCLUSION

In this paper, we proposed 8T SRAM cell and analyze various parameters. These parameters are transient output, leakage current, dynamic current and leakage power and analysis of these parameters has been done on orCad pSpice A/D tool. The 8T SRAM shows better results for dynamic current and reduces the leakage current, leakage power as compare with 6T and 7T SRAM cells.

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