International Journal of Scientific Research in Science, Engineering and Technology
Print ISSN: 2395-1990 | Online ISSN : 2394-4099 (www.ijsrset.com)
doi : https://doi.org/10.32628/IJSRSET218461

A High-Speed Bidirectional Register with Parallel Loading using single electron Threshold Logic Technology

Anup Kumar Biswas
Department of Computer Science and Engineering, Kalyani Govt. Engineering College, Kalyani, Nadia, West Bengal, India

Article Info
Volume 8, Issue 4
Page Number: 394-408

Publication Issue :
July-August-2021

Article History
Accepted : 02 Aug 2021
Published: 08 Aug 2021

ABSTRACT

In this work we have concentrated our attention to a High Speed 4-bit Bidirectional Register with Parallel Loading counting on the principle of threshold logic gates (TLG). After determining the number of logic gates and other circuits needed to complete the desired circuit for our work, we implement some gates and circuits made up of tunnel junctions and capacitances. Some multi-inputs (greater than two) are designed or implemented with the assistance of modified version of the generic multi-input TLG. The types of gates suitable for the implementing the bidirectional Register are 3-input AND, 3-input NAND and 4-input OR gates, in addition an inverter and a more complex circuits like 4:1 Multiplexer are the part and parcel of the desired device. With the help of a 3-input AND gate and a 4-input OR gate, a 4:1 Multiplexer is built. By using the 3-input NAND gate a memory element – D Flip-flop is constructed. At last 4 number of 4:1 Multiplexers and another four number of D Flip-flops are combined in a parallel pattern to implement a 4-bit Bidirectional Register with Parallel Loading. Each component is made after analyzing their corresponding threshold linear equations. After constructing the threshold circuits, again they are formed by using the parameters as capacitors, tunnel junctions with their internal resistances. All the circuit, which are constructed, are verified by simulation with the help of SIMON and the result obtained are investigated and found that they are matched with the theoretical results. For comparing the fastness of our circuit with the CMOS-based or single electron transistor (SET) based circuit, the processing delays of all gates/ circuits are determined. How much power they consume are measured as well. Comparing the delays of CMOS-based and SET based circuit with the TLG based circuit we have decided that our 4-bit Bidirectional Register with Parallel Loading is speedier.

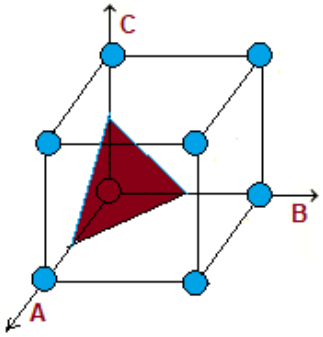
Keywords : High speed, Threshold-logic, tunneling, generic logic gate, bidirectional register

I. INTRODUCTION

Using single electron tunneling phenomena, we will be able to construct different logic gates, inverter, sequential and combinational circuits. Based on some of them, we must be able to implement a more complex circuit called 4-bit Bidirectional Register with Parallel Loading circuit which is made up of 4:1 Multiplexers and D Flip-flops. This circuit is capable of performing the operation of serial right shift, serial left shift and parallel loading under the control of control mode. This circuit consists of 4-stages with two control lines, it can also be extended to n stages with $\lceil log_2(n) \rceil$ control lines. The rule of threshold logic is strictly followed whenever a circuit is implemented. The thumb rule of threshold logic is: if the weighted sum of the multiple inputs of a linear logic circuit is greater than or equal to the threshold value θ of the circuit concerned, the output of the circuit will be $high$ otherwise low. A logical inverter circuit is also provided for the motive of inverting the logic value of a signal. In sections 2, 3, 4 5 and 6 some logic gates/circuits are made up of after analyzing their properties. In section 3, a LTG based D Flip-flop, in section 8, a 4:1 Multiplexer is discussed, in section 7 a multiple input threshold logic gate (TLG) with its functionality is described. In section 9, a "4-bit Shift Register (Bidirectional) with Parallel Load"-diagram based on different parameters like capacitances, resistances and signal voltages are provided. And in the remaining sections, regarding the processing delays, elements required, energy consumptions, speed-up of TLG circuits in comparison with the CMOS and single electron transistors (SETs) are enlightened.

II. 3-input NAND gate using linear threshold logic

The solution set (when value of F(ABC)=(ABC)' equals to 1) of this 3-input AND gate expression can be separated from the non-solution set (when value of F(ABC)=(ABC)' equals to 0) in three dimensional space by a plane. The diagram in support of this is shown in Fig. 1(a). Here blue color small circles indicates the value "1" for the logic expression F(ABC)=(ABC)' and blank small circle indicates the value "0" for the same expression. If these two set of values of the logic expression are separated by a plane then the Expression becomes linearly separable. In Fig. 1(a), the two sets of small circle in the eight corners of a cube is separated by a red plane, so the function representing this cube is linearly separable- i.e., the 3-input NAND gate is linearly separable. A linearly separable logic expression can be represented by a single node TLG.



Fig, 1(a) 3D solution set space diagram of 3-input NAND

Now, we write the threshold logic expression of 3-input NAND as in equation (1) below. The truth table of this expression is listed in Table-1.

$$F = sgn\{w_A \cdot A + w_B \cdot B + w_C \cdot C - \theta\} \quad \cdots\cdots\cdots\cdots (1)$$

Table-1

A	B	C	F(ABC) =(ABC)'	θ	inequality
0	0	0	1	$0 \geq \theta$	(1)
0	0	1	1	$w_C \geq \theta$	(2)
0	1	0	1	$w_B \geq \theta$	(3)
0	1	1	1	$w_B + w_C \geq \theta$	(4)
1	0	0	1	$w_A \geq \theta$	(5)
1	0	1	1	$w_A + w_C \geq \theta$	(6)
1	1	0	1	$w_A + w_B \geq \theta$	(7)
1	1	1	0	$w_A + w_B + w_C < \theta$	(8)

The inequality (1) in Table-1 tells that θ is a negative integer number as θ is considered to be an integer number (it can be taken as real number also). As the NAND gate is a negative logic, so all the 3- weights w_A, w_B and w_C will be of negative numbers. If the value of θ *equals to* -2 and the values of w_A, w_B, w_C are equal to -1 each then all the eight conditional equations given in Table-1 are satisfied. Hence, a solution set of $\{w_A, w_B, w_C: \theta\}$ will be $\{-1,-1,-1:-2\}$. Taking them as satisfactory values, the 3-input threshold logic NAND logic gate expression will be as equation (2) and its respective threshold linear logic gate is depicted in Fig. 1(b)

$F = sgn\{-A - B - C - (-2)\}$ ..... (2)

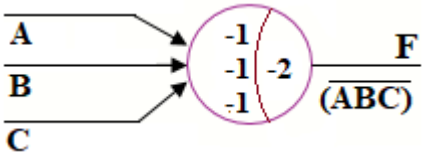


Fig. 1(b) A 3-input NAND TLG

III. Edge triggered D flip-flop with set and reset

Counting on the 3-input NAND gate, a positive edge triggered D flip-flop with set and reset can be implemented. To draw the D Flip-flop, 6(six) number of 3-input NAND gates are essential. The D flip-flop is special regular pattern of 3-input NAND gates and it is placed in Fig. 2 and the corresponding Truth table is given in Table-2 as well. A parameter based D-Flip-flop is depicted in Fig.2(b).

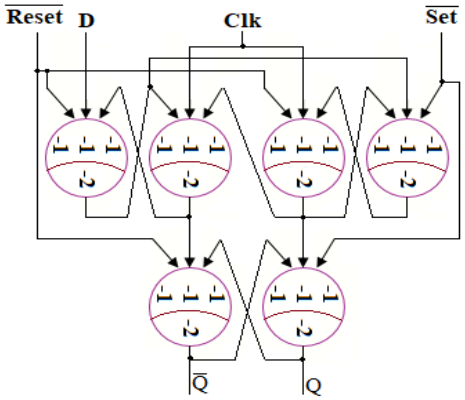


Fig. 2(a) A D-Flip-flop w.r.to TLG

Table 2 : D Flip-flop Truth-Table

$\overline{SET}$	$\overline{RESET}$	D	Clk	Q	$\overline{Q}$
0	1	x	x	1	0
1	0	x	x	0	1
0	0	x	x	1	1
1	1	1	↑	1	0
1	1	0	↓	0	1

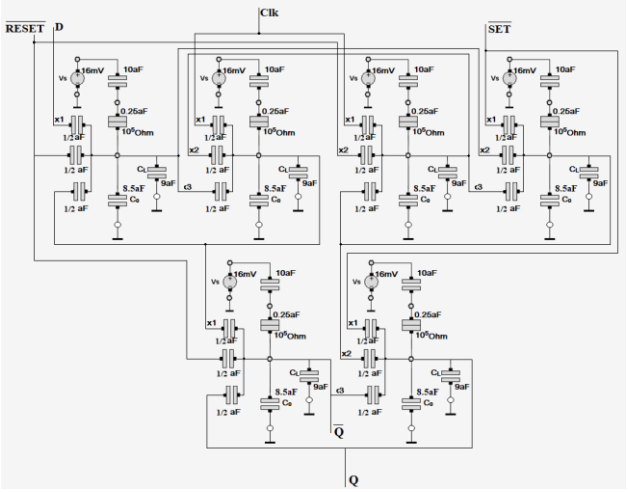


Fig. 2(b) A TLG based D-Flip-flop with parameters

IV. 3-input AND gate

Logical expression of 3-**input AND is** $Y(X_1, X_2 X_3) = X_1 X_2 X_3$.

Threshold logic equation of a 3-input AND gate of three variables X_1, X_2 and X_3 can be written as

$F(X_1X_2X_3) = sgn(w_1 X_1 + w_2 X_2 + w_3 X_3 - \theta)$ ..... (3)

Where, w_1, w_2 and w_3 are the weightage value of X_1, X_2 and X_3 and θ is the threshold value. For finding the exact threshold logic equation of 3-input AND gate, the logic variables (X_1, X_2 and X_3) for positive logic will be set as 1 each. The equation (3) will be as

$F = sgn(w_1 + w_2 + w_3 - \theta)$ .....(4)

To obtain the values of w_1, w_2, w_3 and θ, we first draw the truth table Table-3 of a 3-input AND gate

and compare the weighted sum of weights w_1 , w_2, and w_3 of three variables X_1 and X_2 and X_3 respectively with the threshold value θ [1,2,3, 7, 9].

Table-3

X_1	X_2	X_3	F= $X_1X_2X_3$	θ	Eqn. No.
0	0	0	0	$0<\theta$	(1)
0	0	1	0	$w_3 < \theta$	(2)
0	1	0	0	$w_2 < \theta$	(3)
0	1	1	0	$w_2 + w_3 < \theta$	(4)
1	0	0	0	$w_1 < \theta$	(5)
1	0	1	0	$w_1 + w_3 < \theta$	(6)
1	1	0	0	$w_1 + w_2 < \theta$	(7)
1	1	1	1	$w_1 + w_2 + w_3 \geq \theta$	(8)

For positive logic, we assume weights of X_1, X_2 and X_3 are positive 1 each i.e. w_1=1, w_2=1 and w_3=1. For the case of threshold "θ", if we take the value θ =3, then all the eight inequalities in right-most column in Table-3 are satisfied. Hence, we get a solution set for {w_1 , w_2 , w_3: θ} = {1, 1, 1:3}. So the Threshold logic equation for 3-input AND gate given in equation (3) can be written as equation (5). The corresponding threshold logic gate is drawn in Fig. 3.

$$F(X_1X_2X_3) = sgn(X_1 + X_2 + X_3 - 3) \quad \text{.....(5)}$$

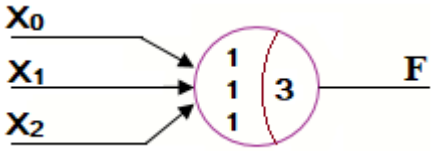


Fig. 3 TLG of F = $X_1X_2X_3$

V. 4-input OR Gate

We are interested in constructing a 4-input OR gate by representing a single node with 4-inputs. Consider the 4-input threshold OR gate as

$$Y(X_1X_2X_3X_4) = sgn\,(w_1X_1 + w_2X_2 + w_3X_3 + w_4X_4 - \theta) \quad \text{.....(6)}$$

While finding the threshold logic equation of 4-input OR gate, the logic variables (X_1, X_2 , X_3 and X_4) for a positive logic will be considered as 1 each. Then the equation (6) will be as

$$Y = sgn(w_1 + w_2 + w_3 + w_4 - \theta) \quad \text{.....(7)}$$

To solve the equation (7) i.e., the values of w_1 , w_2 , w_3 , $w_4$and θ, we draw the truth table Table-4 for the 4-input OR gate and compare the weighted sum of weights w_1 , w_2, and w_3 of four variables X_1 and X_2 , X_3 and X_4 respectively with the threshold value θ [1,2,3, 8, 9].

Table-4

X_1	X_2	X_3	X_4	F=$X_1X_2X_3$	θ	inequality No.
0	0	0	0	0	$0<\theta$	(1)
0	0	0	1	1	$w_4 \geq \theta$	(2)
0	0	1	0	1	$w_3 \geq \theta$	(3)
0	0	1	1	1	$w_3 + w_4 \geq \theta$	(4)
0	1	0	0	1	$w_2 \geq \theta$	(5)
0	1	0	1	1	$w_2 + w_4 \geq \theta$	(6)
0	1	1	0	1	$w_2 + w_3 \geq \theta$	(7)
0	1	1	1	1	$w_2 + w_3 + w_4 \geq \theta$	(8)
1	0	0	0	1	$w_1 \geq \theta$	(9)
1	0	0	1	1	$w_1 + w_4 \geq \theta$	(10)
1	0	1	0	1	$w_1 + w_3 \geq \theta$	(11)
1	0	1	1	1	$w_1 + w_3 + w_4 \geq \theta$	(12)
1	1	0	0	1	$w_1 + w_2 \geq \theta$	(13)
1	1	0	1	1	$w_1 + w_2 + w_4 \geq \theta$	(14)
1	1	1	0	1	$w_1 + w_2 + w_3 \geq \theta$	(15)
1	1	1	1	1	$w_1 + w_2 + w_3 + w_4 \geq \theta$	(16)

From the inequality (1) in the 7th column of Table-4, we have θ is a positive number and from inequalities (2), (3), (5) and (9), our conclusion is that w_1 , w_2 , w_3 , w_4 are all positive as $\theta > 0$. If we take w_1 =1, w_2 =1 , $w_3 = 1$, w_4 =1 and $\theta = 1$, then all the 16 (sixteen) inequalities in right-most column in Table-4 are satisfied. Hence a solution set for {w_1 , w_2 , w_3, w_4: θ} = {1, 1,1,1:1}. So the Threshold logic equation

can be written as equation (8) below. And the corresponding threshold logic gate is depicted in Fig. 4.

$$Y(X_1X_2X_3X_4) = sgn\ (X_1 + X_2 + X_3 + X_4 - 1) \quad \text{..... (8)}$$

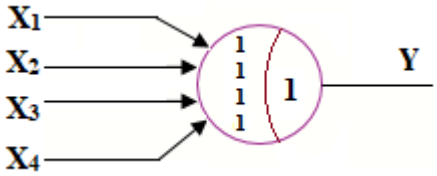


Fig. 4 TLG of $Y = X_1 + X_2 + X_3 + X_4 - 1$

VI. INVERTER

An inverter that complements the input of a variable is shown in Fig. 5(a) [1-4, 8-10]. It is made up of 9 elements as: 5 true capacitors, 4 Tunnel junctions; one input terminal, one output terminal and one bias or supply voltage V_s. This inverter is considered to be constructed with two single electron transistors (SETs) connected in series. Upper two Tunnel junctions (J_1, J_2) and two true capacitors (C_g, C_b) belong to SET1. Similarly, the lower two Tunnel junctions (J_3, J_4) and two true capacitors (C_g, C_b) belong to SET2. Two input terminals connected to the same values V_{in} are straight coupled to the islands (small circles) of the SET1 and SET2 [1, 2, 8-10] through the two capacitors C_g and C_g respectively. The island sizes of each SET are approximately 10 nm diameter of gold and their corresponding capacitance values will be less than 10aF. The output terminal V_0 is straight connected to the common channel between the SET1 and SET2. We ground the output terminal through a load capacitor C_L to suppress charging effects.

While using an inverter, the parameter values are chosen as: V_{g1}=0, V_{g2}=0.1$\times\frac{q_e}{C}$, $C_L = 9C$, $C_j = \frac{1}{10}C$, $5C_j = \frac{1}{2}C$, $C_g = \frac{1}{2}C$, $C_b = \frac{17}{4}C$, R_j 50KΩ. We take the value of C =1aF whenever necessary in this work.

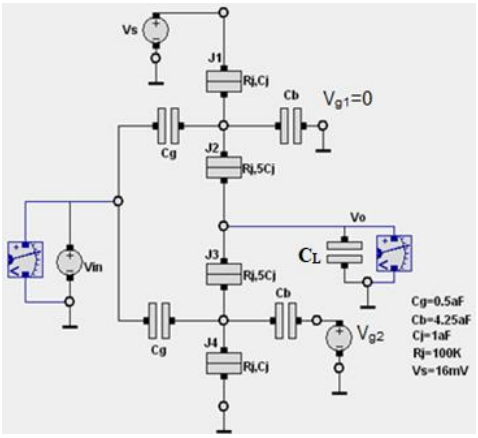


Fig. 5(a) Simulation set of an Inverter

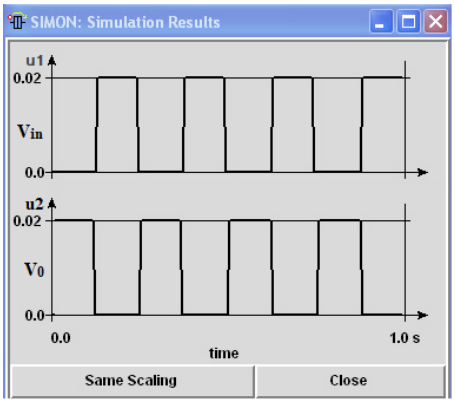


Fig.5 (b) input and output result after simulation of inverter

We maintain the voltages $V_{g1} = 0\ and\ V_{g2}$ =16mV. The operation of the inverter is as follows: - the output V_0 value will be logic high if the input voltage V_{in} is low and that will be 0 logic low (0) if the input voltage V_{in} applied to is high. SET1 (upper part) remains in conduction mode and the SET2 in Coulomb blockade [2-4, 11] whenever the input signal V_{in} being applied to is low. This makes the output voltage V_0 connect to V_b and therefore the output voltage becomes high. If the high input voltage is applied, the charges induced on each of the islands are shifted by a fraction of an electron charge. As a consequence, SET1 transfers to in Coulomb blockade mode and the SET_2 in conducting condition. And we say that the output V_0 changes from high to low logic condition (logic 0).

In this work, we take the inputs "0" =0 Volts and logic "1"=0.1× $\frac{q_e}{C}$.

Whenever simulated, we take C=1aF and Logic "1"= $0.1 \times \frac{1.602\times10^{-19}}{1\times10^{-18}} = 0.1 \times 1.602 \times 10^{-2} = 16.02 \times 10^{-3}$ =16.02 ≅ 16 mV.

VII. General Purpose Multiple input threshold logic gate

A generic multi-inputs threshold logic gate [1-10] depicted in Fig. 6 comprises a tunnel junction bearing internal capacitance C_j and resistance R_j, two multi-input-signals (i) V_k^P s and (ii) V_l^n s which are connected to two points 'q' and 'p' respectively. Each input voltage V_k^P (upper side) is joined at the point "q" through the capacitance C_k^P ; and each input voltage V_l^n (lower side), is joined at the point "p" through the capacitance C_l^n as well. The bias voltage V_b , for the helping of the tunneling, is joined at the point "q" through the capacitor C_b. Tunnel Junction element with its internal capacitance C_j is straight connected between "p" and "q". Point "p" is grounded through C_0. C_j and C_0 play the important role in the circuit. A tunnel event occurs whenever an electron passes through tunnel junction from point "p" to "q". For a LTG, the operation can be expressed by means of a function called signun function . The *signun function* of a function h(x) can be described by two equations (9a) and (9b).

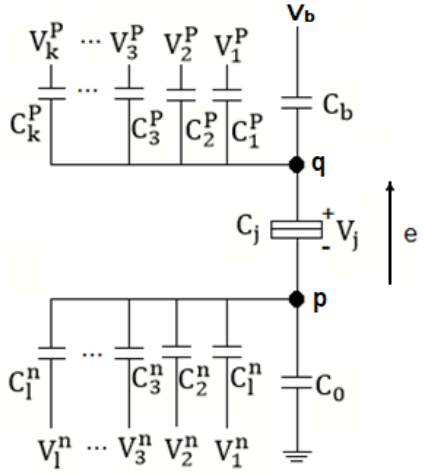


Fig. 6 Threshold logic gate with multi-input

$$g(x) = \mathrm{sgn}\{h(x)\} = \begin{cases} 0, & if\ h(x) < 0 \\ 1, & if\ h(x) \geq 0 \end{cases} \quad \text{..... (9a)}$$

$$h(x) = \sum_{k=1}^{n}(w_k \times x_k) - \theta \quad \text{..... (9b)}$$

where x_k represents n-Boolean inputs, and w_k are their corresponding integer weights.

The LTG compares the weighted sum of the inputs $\sum_{k=1}^{n}(w_k \times x_k)$ with the threshold value θ. When $\sum_{k=1}^{n}(w_k \times x_k)$ is greater than or equal to the threshold value θ of the circuit, output of the LTG becomes high (logical "1"), otherwise it is low (logical "0").

VIII. Threshold logic gate based 4:1 Multiplexer

Multiplexer has four inputs, one output and two control lines. In the previous sections we have enlightened about the 3-input AND gate, 4-input OR gate and an inverter. Following the functional diagram of Fig.7 (b), a threshold logic gate based 4-to-1 line Multiplexer is depicted in Fig. 7(a). Counting upon the control mode of C_1 C_0 we can select one of the four inputs A, B, C and D input for each mode.

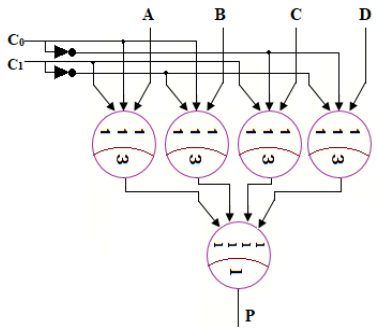


Fig. 7(a) TLG based 4:1 Multiplexer

C_1	C_0	P
0	0	D
0	1	C
1	0	B
1	1	A

Fig. 7(b) Functional Diagram

After manipulating the measuring of parameters of 3-input AND gate (TLG based), we have got the capacitor values shown in Table-6 in section 9 and with the help of them, a simulation set of a 4:1 Multiplexer is drawn in Fig. 8 below.

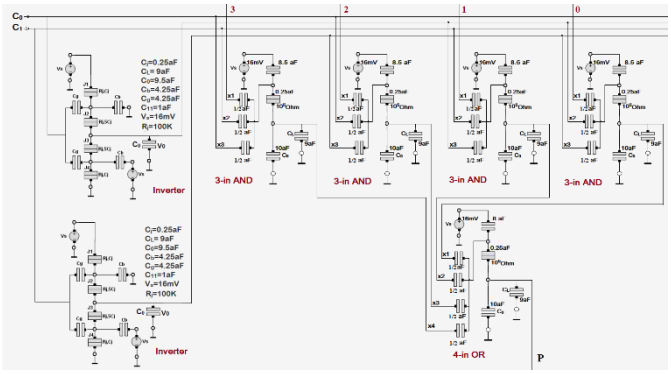


Fig.8 Simulation set of a 4:1 Multiplexer

IX. Shift Register (Bidirectional) with Parallel Load

A Shift registers can convert the serial data to parallel data, and reversely convert serial data to parallel. Shift registers can be used as: data enter into serially but they are taken out in parallel from the outputs of D Flip-flops used here. If there is an advantage of adding a parallel-load capability, then data are being penetrated or entered in parallel can be found out serially by shifting the stored data in the desired register.

A shift register can have the essential input and output ports for transferring data parallely. It can have facilities both of right-shifting and left-shifting of data through the flip-flops of the register concerned. Other registers can have some of the functions not all but with 1(one) shift operation. The general purpose shift register have the following capabilities.

a) For synchronizing all operations a **clock-pulse** *input* for providing clock pulses.
b) A set or *clear* control to set or clear the register to 1 or 0.
c) A *shift-right* control can enable to do shift-right operation and make the *serial input* and *output* lines related to the shift right enable.
d) A *shift-left* control, in the same manner as discussed in (c), can enable the shift-left operation and that create the *serial input* and *output* lines relating to the shift-left enable.
e) *There will be* ***n*** parallel output lines.
f) A control state which is providing the information in the register remains unaltered even if clock pulses are provided continuously.

A register can be a bidirectional shift register in this case it can shift data either right or left. If a register can only shift data in one direction then it is treated as a unidirectional shift register. If the register has capabilities of both directional shift and parallel load, then this register is identified as a shift register with parallel load.

Here, a linear threshold logic gate based shift register having all the capabilities cited above is given in Fig. 9. It comprises four *D* flip-flops and four 4:1 Multiplexers connected to control lines C_1 and C_0. Under the different control mode of lines C_1 and C_0, the operation of the register will be as:

When C_1 C_0=0 0, there would be no change of the output terminals ($B_4B_3B_2B_1$) of the register in Fig.9. In this situation a path is formed from each of four outputs of the four flip-flops into their corresponding flip-flops. The next clock-pulse, when applied, transfers the binary values previously stored into each flip-flop. As a result the change of the state occurs.

When C1 C_0=0 1 and a clock pulse is applied, one right shift happens

When C1 C_0=1 0 and a clock pulse is provided, one left shift happens

When C1 C_0=1 1 and a clock pulse is given, all the data ($A_4A_3A_2A_1$) connected to the terminals 3 for each MUX will be selected and transferred to corresponding D Flip-flops, i.e., loaded parallely. The selection modes and related operations are listed in tabular form in Table-5.

Table-5

Mode		Operation of register
C_1	C_0	
0	0	Unaltered
0	1	Right shift
1	0	Left shift
1	1	Load parallely

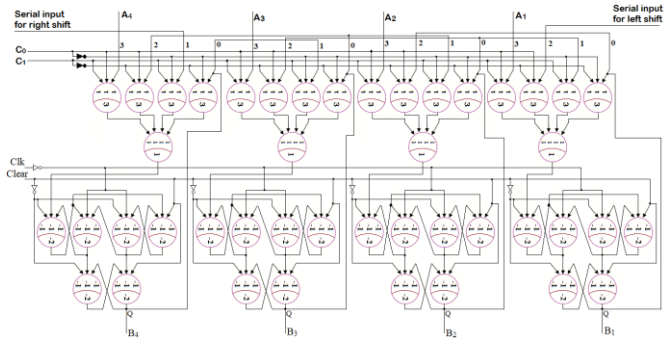


Fig.9 A 4- bit bilateral shift register with parallel load

A bidirectional shift register with parallel load depicted in Fig.9 and Fig.10 are the generic register being capable of performing three types of operations: left-shifting, right-shifting and parallel-loading.

A. Simulation set and result of 4-bit bilateral shift register with parallel load

An interested person may be interested in simulating the input –output results for the 4- bit bilateral shift register with parallel load. Before establishing the simulation set, what types of essential components are to be taken into consideration?

Two types of electronic components (i) 4:1 Multiplexers and (ii) Flip-flops which are made up of either 3-input AND gate or 3-input NAND or 4-input OR gate. These three kinds of gates are discussed in previous sections. Their linear threshold logic expressions and the corresponding logic gates are provided in due places. But the elements required to construct them are not cited. After analyzing each of their logic expressions we have measured numerical values of elements like capacitances, resistances and the supplied voltages to activate the execution of operations. The list of the parameter values relevant to the different logic gates with which we can build a 4--bit bilateral shift register with parallel load is given in Table-6. For inverting a signal, an inverter will be needed.

Table-6

Sl. No.	Expressions used	Name of Expression	Parameters required for setting
1	$F(X_1X_2X_3) = sgn(X_1 + X_2 + X_3 - 3)$	3-input AND gate	logic input "0"=0V, logic "1" = 16mV,C=1aF, $C_1^p = C_2^p = C_3^p = \frac{1}{2}C$ =0.5aF, $C_b = 8.5aF$, $C_j = 0.25aF$, $C_L = 9aF$, $C_0 10aF$, R_j = $10^5\ \Omega$, . $V_b = V_b$ =V_s=16mV
2	$Y(X_1X_2X_3) = sgn(-A - B - C + 2)$	3-input NAND gate	"0"=0V, logic "1" = 16mV, C=1aF, $C_1^n = C_2^n = C_3^n = \frac{1}{2}C$ =0.5aF, $C_b = 10aF$, $C_j = 0.25aF$, $C_L = 9aF$, $C_0 = 8.5aF$, R_j = $10^5\ \Omega$, . $V_b = 15.81mV$, V_s=16mV
3	$Y(X_1X_2X_3X_4) = sgn(X_1 + X_2 + X_3 + X_4 - 1)$	4-input OR gate	"0"=0V, logic "1" = 16mV, C=1aF, $C_1^p = C_2^p = C_3^p = C_4^p = \frac{1}{2}C$ =0.5aF, $C_b = 8aF$, $C_j = 0.25aF$, $C_L = 9aF$, $C_0 = 10aF$, R_j=$10^5\ \Omega$, . $V_b = 15.81mV$ V_b =V_s=16mV
4	$Y \leftarrow \overline{Y}$	Inverter	For the inverter, the parameter values chosen are: V_{g1} =0, V_{g2} =0.1 × $\frac{q_e}{C}$, $C_L = 9C$, $C_j = \frac{1}{10}C$, $5C_j = \frac{1}{2}C$, $C_g = \frac{1}{2}C$, $C_b = \frac{17}{4}C$, R_j =50K Ω . For the case of simulation, the value of C =1aF is taken.

The operation of a bidirectional shift register with parallel load is discussed in the previous section 8. For space limitation, only a 4-bit bilateral shift register with parallel load is taken into consideration. The parameter based 4- bit bidirectional shift register with parallel load is depicted in Fig.10 {Fig. 10(a) + Fig. 10(b)}. As the picture of 4- bit bilateral shift register

with parallel load is large in size, the picture is sectioned into two parts Fig. 10(a) and Fig. 10(b). After combining these two parts one after another, you will get full picture of the 4-bit bidirectional shift register with parallel load.

If we concentrate our attention on the control lines C_1 C_0, and we give the control signals C_1 C_0 = 0 0. With next clock pulse when applied, the binary value stored in each flip-flop previously is transferred into all the D Flip-flops. As a result there is no change of state happens. If control signals C_1 C_0 = 0 1, with next clock pulse, the 1-terminal of the four Multiplexers get the communication path to the inputs of the D Flip-flops. This makes a right shift operation and a "*serial input value from the leftmost Serial input*" for right shift in Fig 10(a) is transferred into terminal number 1 of the leftmost multiplexer. If the control signals C_1 C_0 = 1 0 is applied with a next clock pulse, a left operation happens, with the results that a "serial input from the rightmost side" in Fig. 10(b) enters into flip-flop rightmost Flip-flop. And lastly, if the control signals C_1 C_0 = 1 1, the binary information available at $A_4A_3A_2A_1$ are passed to the register simultaneously at the time of next clock pulse applied. The simulation results regarding the circuit drawn in Fig. (10(a) +10(b)) is given in Fig. 10(c).

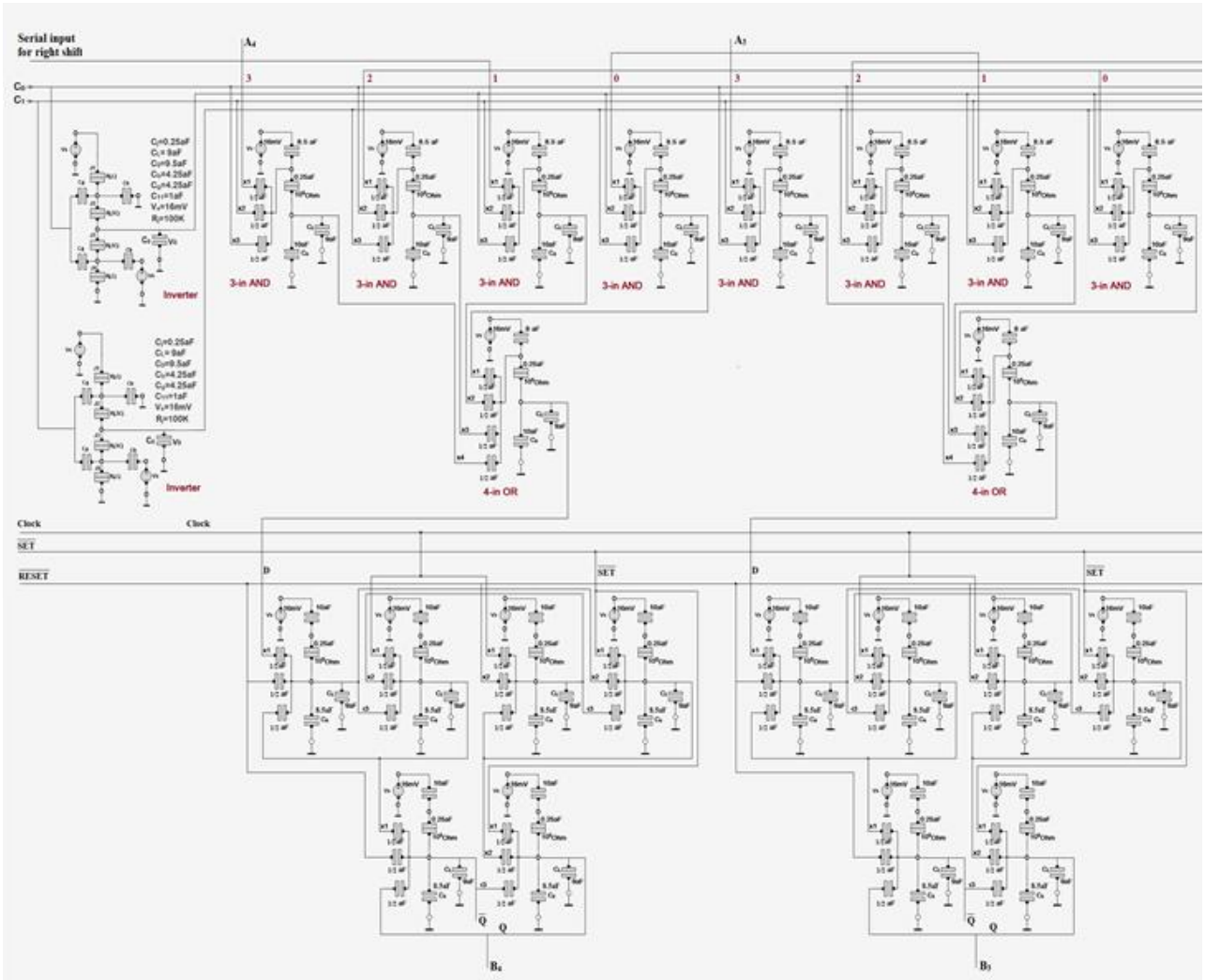


Fig. 10(a) 4- bit bilateral shift register with parallel load based on parameters (Left Part)

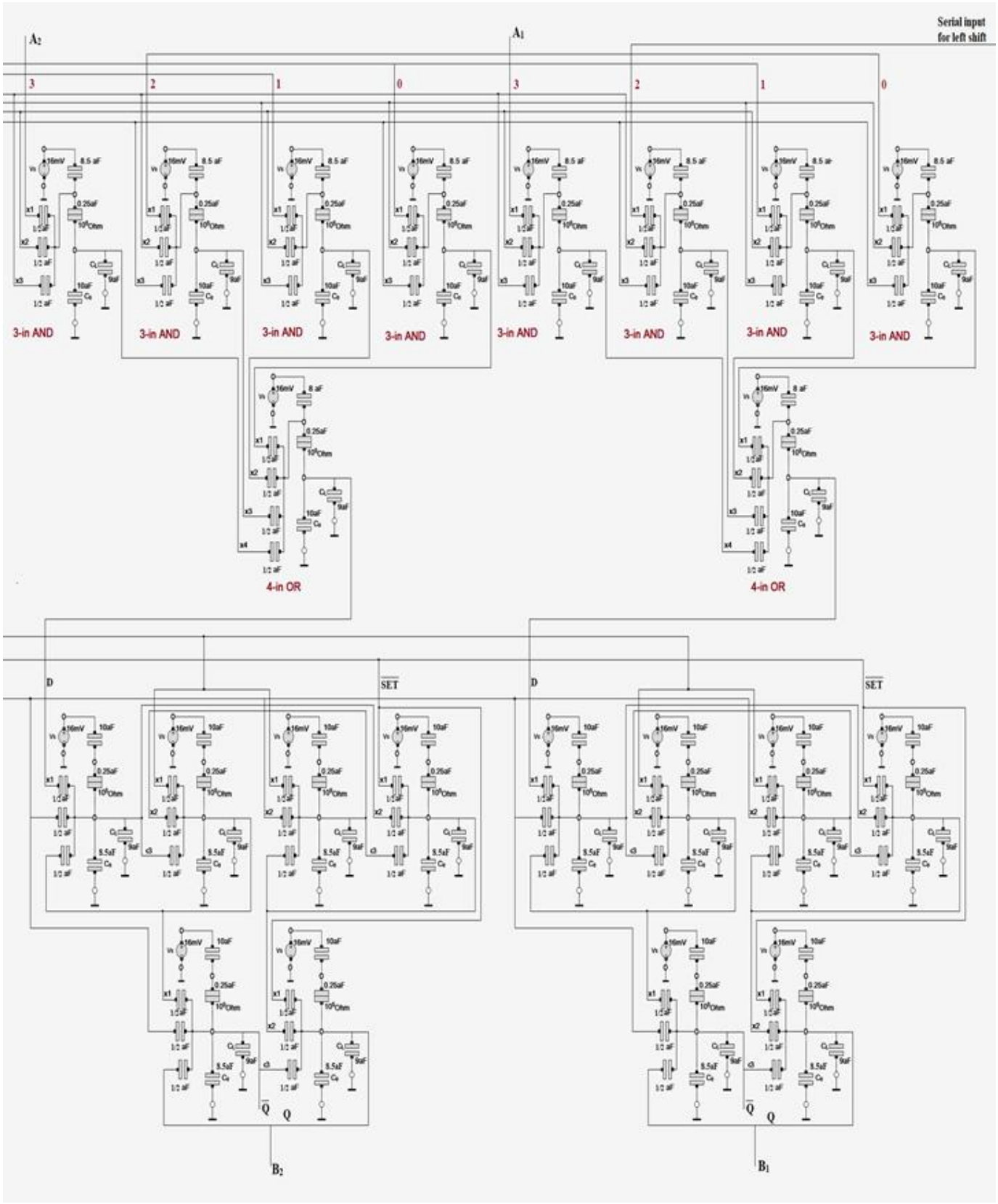


Fig. 10(b) 4- bit bilateral shift register with parallel load based on parameters (Right Part)

Given that $A_4A_3A_2A_1$ =1 0 1 1
Serial input for right shift =1
Serial input for left shift=1

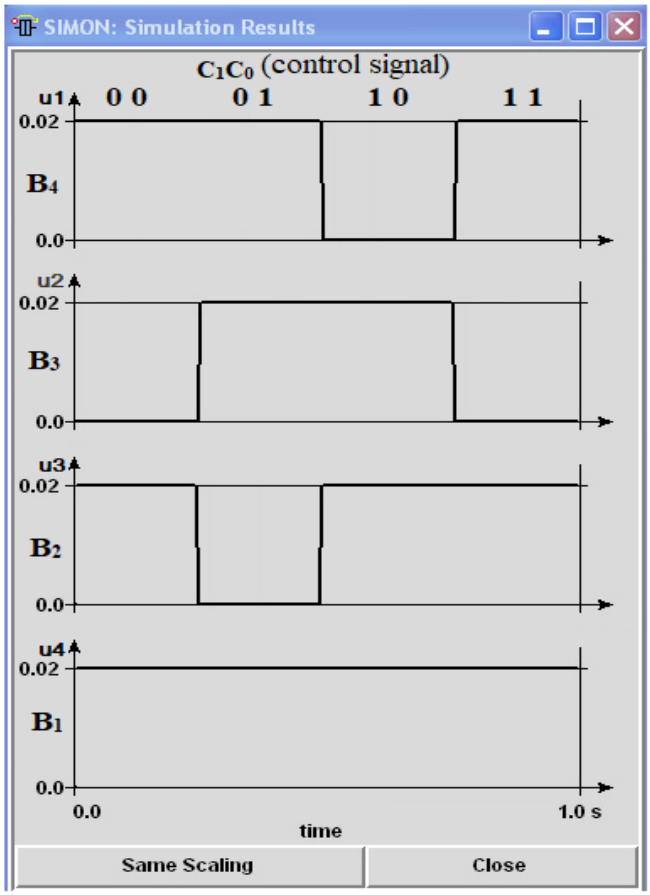


Fig. 10(c) Simulation result of Fig. 10(a) +Fig. 10(b)

Initially, it is cocsidered that the inputs of A_4 A_3 A_2 A_1=1 0 1 1 in Fig.10, serial input (for Right shift) =1 and serial input (for left shift) =1. For the "*set*" of all D Flip-flops, we can use $\overline{SET}$ =1 and $\overline{RESET}$ =0 without clock pulse or $\overline{SET}$ =1 and $\overline{RESET}$ =1 and with a stored value of all D flip-flops 0 and with a clock pulse.

Now, we apply the control signal C_1C_0 =00 with a clock pulse, the output at the output terminals $B_4B_3B_2B_1$ will be same as will be the same as before, i.e., if the initial binary values stored in the D Flip-flops $B_4B_3B_2B_1$=1010, then after the next clock pulse the output at terminals $B_4B_3B_2B_1$ will be1011 as shown in Fig. 10(c).

Next, when we put the next pulse and C_1C_0 is changed to 01, then one right shift happens and the output becomes $B_4B_3B_2B_1$=1101, next when C_1C_0 is changed to 10 and a clock pulse is applied, one left shift of $B_4B_3B_2B_1$ occurs and the result changes to $B_4B_3B_2B_1$=0111, and at last if we put C_1C_0 = 11, all the four Multiplexers input are selected and the output lines get the connection path from A_i to B_i, [i =1,2,3 and 4], so the result becomes $B_4B_3B_2B_1$ = $A_4A_3A_2A_1$. AS we have chosen $A_4A_3A_2A_1$=1011, so the output value of $B_4B_3B_2B_1$ = 1 0 1 1. All these simulation results which are executed by the simulator are shown in Fig. 10(c). The results are also listed in Table-7 as well.

Table 7

Set the D Flip-flop						
$\overline{SET}$	$\overline{RESET}$	D	Clk	Q	$\overline{Q}$	Result
1	0	×	×	0	1	Set the Flip-flop
1	1	0	↓	0	1	Set the Flip-flop
Input at terminals A_4 A_3 A_2 A_1						
Right input	Left input	A_4	A_3	A_2	A_1	Result
0	1	1	0	1	1	Input values given
Control mode		**Output of all Flip-flop**				
C_1	C_0	B_4	B_3	B_2	B_1	Result
0	0	1	0	1	1	No change
0	1	1	1	0	1	Right shift A into B
1	0	0	1	1	1	Left shift A into B
1	1	1	0	1	1	A_4 A_3 A_2 A_1

X. Discussion concerning Delay, Switching energy and Fastness

When implemented a circuit of a device, some indispensable components are collected, and joined them to make it. Similarly, for the case of **bilateral shift register with parallel load**, 3-input AND gate, 3-input NAND gate, 4-input OR gate, 4:1 Multiplexer, D Flip-flop and inverter are essential. A **4-bit bilateral shift register with parallel load** is implemented by using the components cited above. Efficiency of a device relies upon several factors like execution time, component numbers, costs of materials, fan-outs, speed, power consumption, controlling charge etc. First we calculate the processing delays of all the

components used in our work. For calculating the processing/switching delays, we are to involve the critical voltage V_c as well as the tunnel junction capacitance C_j of the linear TLG concerned. This delays with respects to logic gate/circuit may be measured by the approaches [1-3, 8, 9] given below.

$$\text{Delay} = -(e|\ln(P_{error})|R_t) / (|V_j| - V_c) \cdots\cdots (10)$$

Here, V_j is the tunnel junction voltage and V_c is the critical voltage and R_t is being the internal junction resistance. Execution of the circuit occurs only when a tunneling event occurs. The tunneling event occurs only when the tunnel junction voltage V_j is higher than or equal to the internal critical voltage V_c, i.e., when $|V_j| \geq V_c$. Whenever this conditional expression is gratified by a 3-input AND gate, junction voltage of the 3-input AND gate becomes V_j =11.8mV, the internal critical voltage V_c of the tunnel junction is found to be 11.58mV. The parameter values of tunnel resistance $R_t = 10^5\Omega$ and the probability of error $P_{error} = 10^{-12}$ are given. Putting these values into equation (10) we measure the gate delay =0.072|ln ($\boldsymbol{P_{error}}$) ||ns = 1.98 ns. In this same way we can find out the delays of different gates/ circuits and they are listed in Table-6 and 7.

While tunneling, an electron passes through the junction barrier, then the total energy in the circuit is altered. The energy levels, before and after the tunneling event are measured by using the equation (11).

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel} = -e(V_c - |V_j|) \cdots\cdots (11)$$

This switching/tunneling energy $-e(V_c - |V_j|)$ is consumed for a tunnel event in the tunneling circuit. We have listed the energy consumptions with respect to different TLG circuits in Table-6.

Table-8

Gate/Device	n elements	Delay (ns)	Switching Energy meV
inverter	9	0.022|ln($\boldsymbol{P_{error}}$) |	10.40
2-in NOR	6	0.060|ln($\boldsymbol{P_{error}}$)|	10.70
2-in OR	6	0.062|ln($\boldsymbol{P_{error}}$)|	10.80
2-in NAND	6	0.062|ln($\boldsymbol{P_{error}}$) |	10.80
2-in AND	6	0.062|ln($\boldsymbol{P_{error}}$) |	10.80
3-in AND	7	0.072|ln($\boldsymbol{P_{error}}$) |	11.58
3-in NAND	7	0.072|ln($\boldsymbol{P_{error}}$) |	11.58
2-in XOR	13	0.080|ln($\boldsymbol{P_{error}}$)|	21.20
3-in OR	7	0.073|ln($\boldsymbol{P_{error}}$) |	11.58
3-in NOR	7	0.072|ln($\boldsymbol{P_{error}}$) |	11.57
4-in OR	8	0.078|ln($\boldsymbol{P_{error}}$) |	14.22
4:1 MUX	54	0.172|ln($\boldsymbol{P_{error}}$) |	103.4
D Flip-flop	42	0.144|ln($\boldsymbol{P_{error}}$) |	60.58
4-bit Bidirectional Register	330	0.288|ln($\boldsymbol{P_{error}}$) |	676.72

Two curves have been drawn in respect of the switching delay vs. switching error probability in Fig. 11(a) as well as the switching delay vs. the unit capacitance C (=1aF) in Fig. 11(b) below.

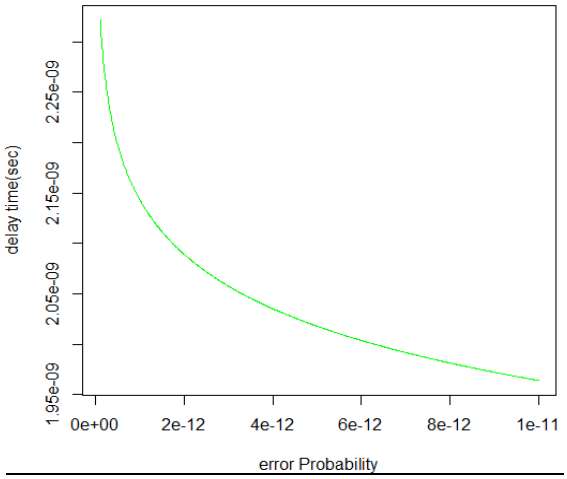


Fig. 11(a) Delay vs. Error Probability

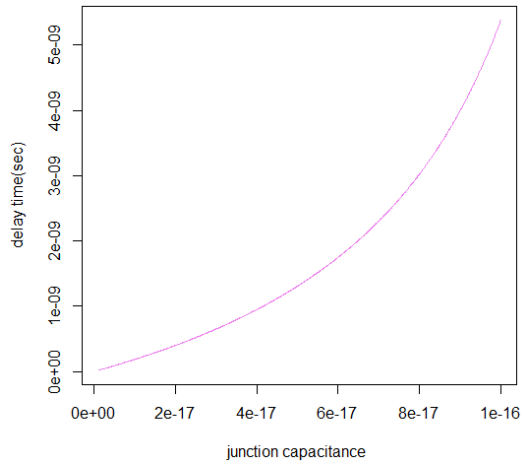


Fig. 11(b) Delay Vs. capacitance

The total number of small elements required to construct a gate or circuit is counted. We keep track of the data got from this work in relation to small element numbers, delays or late, and switching energy and all of them are given in Table-6.

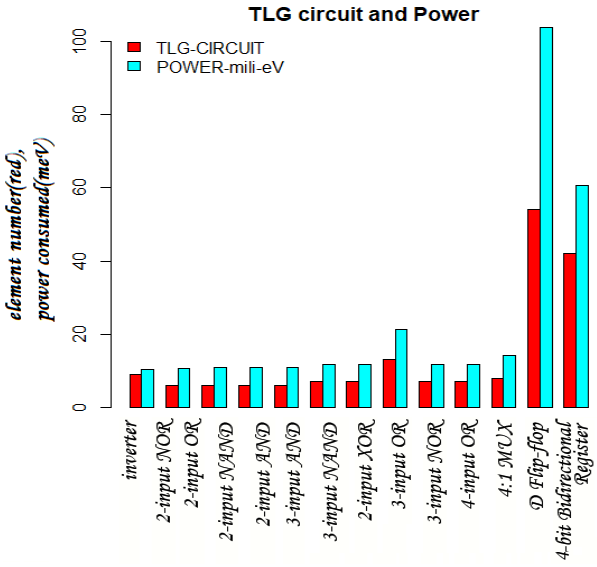


Fig. 12 comparison of small Elements and switching energy

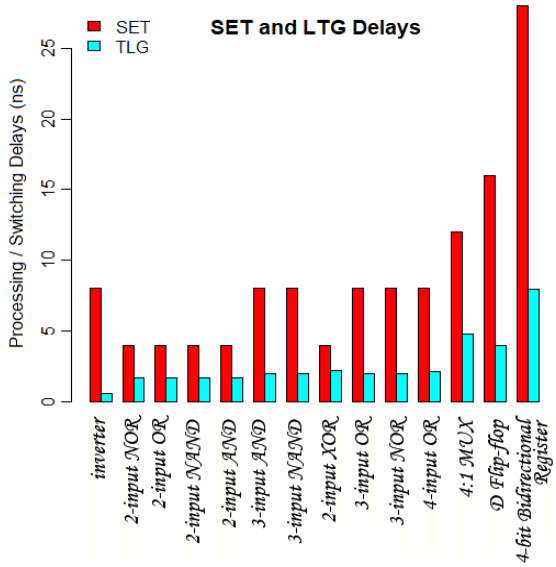


Fig. 13 Delays of SET/TLG Vs. gates

The execution delays for distinct threshold logic circuits must be distinct. For instance, for the 3-input OR gate, the processing delay is 2.01 ns, for 2-input XOR gate it becomes 2.21 ns, and in the 4- bit bilateral shift register with parallel load – delay is $0.288|\ln(P_{error})|$ns.

Given the value of $P_{error} = 10^{-12}$, so the time after which the first output of the 4- bit bilateral shift register with parallel load circuit will fan out is $0.288|\ln(P_{error})|$ns =7.95 ns. Hence, we surely maintain the control signal time i.e., after every 7.95 ns or more we are to apply the control signals (C_1C_0). In this condition, the speed or frequency of the 4- bit bidirectional shift register with parallel load circuit will be $1/7.95\ ns$ = 125.78 MHz.

We are interested in finding out the circuit delays as to CMOS, SET-based and LTG-based. The have obtained the processing delays in case of a CMOS logic gate for AND, NAND, NOR, XOR is 12ns [1-4, 8, 9]. The tunneling time through a single electron transistor (SET) [9, 10] is approximately 4ns [4-6, 12, and 13].

Table-9

Gate/Device	SET-based delay ns	LTG-based delay ns	Speed-up times
inverter	8	0.60	13.33
2-input NOR	4	1.65	2.42
2-input OR	4	1.71	2.33
2-input NAND	4	1.71	2.33
2-input AND	4	1.71	2.33
3-input AND	8	1.98	4.04
3-input NAND	8	1.98	4.04
2-input XOR	4	2.21	1.81
3-input OR	8	2.01	3.98
3-input NOR	8	1.99	4.02
4-input OR	8	2.15	3.72
4:1 MUX	12	4.75	2.52
D Flip-flop	16	3.96	4.04
4-bit Bidirectional Register	28	7.95	3.21

A. Switching delays of SET and LTG

Assuming that the error probability is 10^{-12}, the processing late /delays for different gates/circuits we have measured are given in Table-7. From the Table-7, we find that the LTG based circuit is at least 2 times faster than the SET based circuit. And in connection with CMOS, the LTG based circuit is at least 8 times faster than it.

XI. CONCLUSION

In this work, a 4-bit bidirectional resister capable of right-shifting and left-shifting of data is implemented. This circuit can also load a 4-bit data parallely. This device is made up of 4:1 Multiplexers and D Flip-flops which are also implemented with the help of 3-input AND gate, 3-input NAND gate and 4-input OR gate based on the principle of threshold logic. For the verification of our circuit "4-bit bidirectional resister", it is simulated by using the simulator-SIMON and the result we got is correct and errorless. The switching delays, power consumptions and the number of elements required for all the circuits, we have implemented, are measured. As the TLG based circuits' operation relies upon the tunneling of an electron, the power consumed for moving an electron will be very small. For instance, in a 4-bit bidirectional resister, the power consumption, when an electron passes through the circuit, is 676.72meV= $676.72 \times 10^{-3} \times 1.602 \times 10^{-19}$ Joule $=1.084 \times 10^{-25}$ Joule which is very small amount. When comparing to the switching delays of CMOS based circuits and SET based circuit with respect to the TLG-based circuit, we obtain that TLG-based circuit is at least 8-times and 2-times faster than them respectively. The drawback of single electron based threshold logic technology is that the temperature during the execution must be maintained at $0K$. To maintain this low temperature is, no doubt, difficult. In the work, control line signals must be changed after 7.95ns or more otherwise proper result will not be obtained.

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BIOGRAPHY

ANUP KUMAR BISWAS, born in 1971. He defended his Ph.D.[Engg.] thesis in 2005 in the stream of Electronics and Telecommunication Endineering at Jadavpur University. He was a Senior Research Fellow(SRF) in Faculty of Engineering and Technology (*FET*) from 2002 to 2005 at the Department of Electronics &TC. Dr. Biswas has published 27 papers in national, international journals and conferences. The area of his scientific interests are computer arithmetic, parallel architectures, nanotechnology, and computer-aided design. He is engaged in research activities and teaching last 18 years.

Cite This Article :

Anup Kumar Biswas, " A High-Speed Bidirectional Register with Parallel Loading using single electron Threshold Logic Technology, International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 8, Issue 4, pp.394-408, July-August-2021. Available at doi : https://doi.org/10.32628/IJSRSET218461
Journal URL : https://ijsrset.com/IJSRSET218461