

Integrated-Circuit Random Access Memory based on an Emerging Technology - Electron Tunneling Through Tunnel Junction

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ABSTRACT

Depending upon the Principle of linear threshold logic, we will be able to construct more complex circuits with low power, electronic speed, and high concentration density. In this work, a more complex circuit called Integrated-Circuit Random Access Memory has been developed. To develop this Random Access Memory we will have to implement some small components like 3-input AND gate, a 4-input OR gate, inverter, RS Flip-flop, 2×4 decoder. After verifying their theoretical characteristics with the simulated result done by the simulator, we have constructed the desired IC RAM using them. All the small elements we have provided in due places are analyzed, found out their threshold logic equations, drawn their threshold logic gates, listed their truth tables, given the corresponding circuits with exact values of parameters and above all drawn their input-output simulated graphs. Based on 3-input AND gate and Inverter, a memory cell (MC) is implemented. Arranging the memory cells in a regular pattern with the assistance of the decoder, a random access memory (RAM) of 4 words having 3-bits each is built. Whether the circuits drawn is faster or not are checked with the same type of CMOS circuits and Single electron transistor (SET) based circuits. We have observed that our threshold logic based circuits are mere faster than the other two types. The power required for execution or for performing the tunneling event is measured and seen that it is in the range of up to 900meV which is really very low. All the circuit presented in this work are made up of generic multiple input threshold logic gate(s) which is also described.

Keywords : Electron-tunneling, Threshold logic, Memory cell, RAM, high-speed, low-power

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I. INTRODUCTION

The access mode for a memory system is fixed by the different components used in the system. For the case of a RAM, the different word locations can be

considered to be separated in space with every word capturing a particular location. Two types of operating mode for Integrated-circuit RAM units are available and which are being static and dynamic. The static RAM is made up of internal flip-flops which

really store the binary information in the form of 0 and 1. The stored information becomes valid till the power supply is available in the unit. We are not interesting in discussing about the dynamic mode. The static RAM is easy to use and it has shorter read and write cycles. When the power is shut down and at that time if the Memory units losses all the information, the memory units are termed as volatile. IC RAMs, either static or dynamic, are volatile since the binary memory cells require continuous power supply to maintain the information stored in the cells.

On the basis of single electron tunneling phenomena utilizing General Purpose Multiple input threshold logic gate which is discussed later, we will be able to construct some logic gates, inverter, 2×4 Decoder, RS Flip-flop and binary Memory Cell (MC). With the help of them, we will be able to implement a more complex circuit called “Logical construction of an IC for a 4×3 RAM” which is made up of one 2×4 Decoder, twelve MC and three 4-input OR Threshold Logic Gate. This 4×3 RAM circuit is capable of performing the operation of storing binary information in the form of 3-bit word; and these 3-bit word of four words can be retrieved/stored easily by using the address lines of the Decoder and read/write signal line. Though this RAM circuit is confined to 4×3 RAM because of space limitations, it can be extended up to $2^n \times m$ RAM, where n= number of decoder address lines and m= word length. The threshold logic rule is strictly maintained whenever a TLG circuit is implemented. The thumb rule for a threshold logic is as follows: in case the weighted sum of the multiple inputs of a linear threshold logic circuit is more than or equal to the threshold value θ of the related circuit, then the output signal of the circuit must be *high* otherwise *low*. A logical inverter circuit that inverts the value of its own is being provided for the purpose of inverting the logic value of a signal. In sections 2, 3, 6 and 7 some logic gates/circuits are made up of after analyzing their properties. In section 2, a LTG based 3-input AND; in

section 3, a 4-input OR TLG; in section 4, an inverter; in section 5, a multi-input threshold logic gate; in section 6, a RS Flip-flop; in section 7 a 2×4 Decoder and in section 8, an IC Random Access Memory are discussed. In Table-7, distinct circuit parameters like capacitances, resistances and signal voltages are provided for different circuits. Regarding the processing delays, number of elements needed, energy consumptions, speed-up times of TLG circuits in connection with the CMOS and single electron transistors (SETs) are focused in the remaining sections.

II. METHODS AND MATERIAL

1. 3-input AND gate

For the purpose of constructing a 3-input AND gate based on TLG, we first think of Threshold logic equation (1) of a 3-input AND gate of three variables X_1 , X_2 and X_3 .

$$F(X_1X_2X_3) = \text{sgn}(w_1X_1 + w_2X_2 + w_3X_3 - \theta) \dots\dots\dots (1)$$

For finding the linear threshold logic equation relating to 3-input AND, the logic variables (X_1 , X_2 and X_3) for the positive logic should be taken as 1 each and the equation (1) will be written as

$$F = \text{sgn}(w_1 + w_2 + w_3 - \theta) \dots\dots\dots(2)$$

To unearth the values of w_1 , w_2 , w_3 and θ , we first trace the truth table Table-1 of a 3-input AND gate and compare the weighted sum value of weights w_1 , w_2 , and w_3 of three variables X_1 and X_2 and X_3 respectively with the value θ [1-4, 8-10].

Table-1

X ₁	X ₂	X ₃	F= X ₁ X ₂ X ₃	θ	Eqn. No.
0	0	0	0	$0 < \theta$	(1)
0	0	1	0	$w_3 < \theta$	(2)
0	1	0	0	$w_2 < \theta$	(3)
0	1	1	0	$w_2 + w_3 < \theta$	(4)
1	0	0	0	$w_1 < \theta$	(5)
1	0	1	0	$w_1 + w_3 < \theta$	(6)
1	1	0	0	$w_1 + w_2 < \theta$	(7)
1	1	1	1	$w_1 + w_2 + w_3 \geq \theta$	(8)

For positive logic, we choose the weights of X₁, X₂ and X₃ as 1 each i.e. w₁=1, w₂=1 and w₃=1. For the case of threshold “θ”, if we take the value θ =3, then all the eight inequalities in 6th column in Table-1 are satisfied. Hence, we have a solution set for {w₁ , w₂ , w₃: θ} = {1,1,1:3}. So the Threshold logic equation for 3-input AND gate is given below in equation (3) and the corresponding threshold logic gate is drawn in Fig. 1(a). The capacitor based circuit of the Fig. 1(a) is drawn in Fig. 1(b) and the simulated result of it is depicted in Fig. 1(c) as well.

$$F(X_1X_2X_3) = \text{sgn}(X_1 + X_2 + X_3 - 3) \dots\dots\dots(3)$$

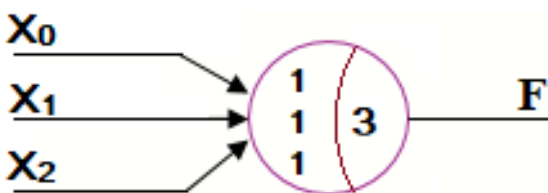


Fig. 1(a) TLG of F = X₁X₂X₃

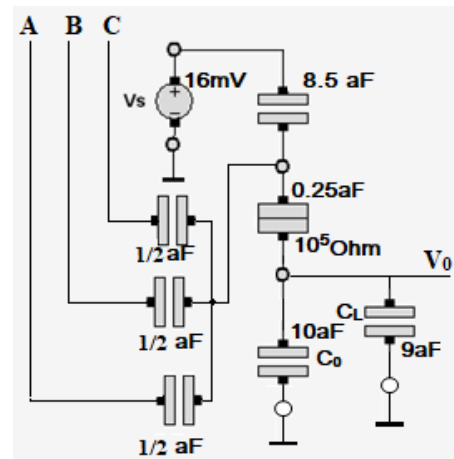


Fig. 1(b) Simulation set of 3-in AND

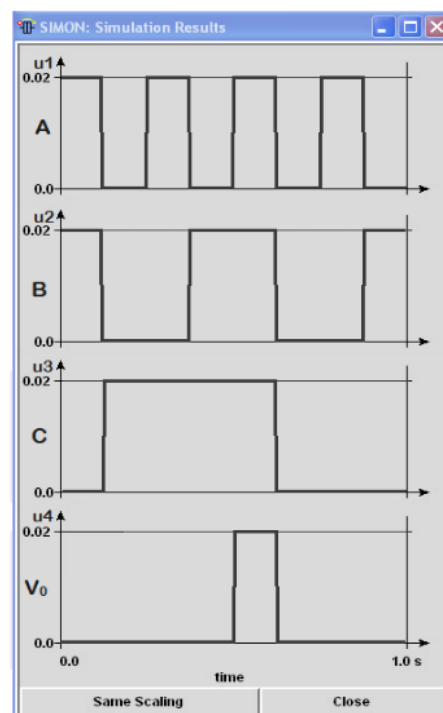


Fig.1(c) simulated result Fig. 1(b)

2. 4-input OR Gate

Now 4-input OR gate based relation will be derived. Let the threshold logic equation of a 4-input OR TLG of four variables X₁, X₂, X₃ and X₄ be

$$Y(X_1X_2X_3X_4) = \text{sgn}(w_1X_1 + w_2X_2 + w_3X_3 + w_4X_4 - \theta) \dots\dots\dots(4)$$

For finding the linear threshold logic equation relating to 4-input OR, the logic variables (X₁, X₂ and

X_3) for the positive logic should be taken as 1 each and the equation (4) will be written as

$$Y = \text{sgn}(w_1 + w_2 + w_3 + w_4 - \theta) \dots\dots\dots (5)$$

To have the values of w_1, w_2, w_3, w_4 and θ , we first trace the truth Table-2 of a 4-input OR gate and compare the weighted sum of weights w_1, w_2, w_3 and w_4 of four variables X_1 and X_2, X_3 and X_4 respectively with the threshold value θ [1 – 4, 9 – 10].

Table-2

X ₁	X ₂	X ₃	X ₄	4-in OR	θ	inequality No.
0	0	0	0	0	$0 < \theta$	(1)
0	0	0	1	1	$w_4 \geq \theta$	(2)
0	0	1	0	1	$w_3 \geq \theta$	(3)
0	0	1	1	1	$w_3 + w_4 \geq \theta$	(4)
0	1	0	0	1	$w_2 \geq \theta$	(5)
0	1	0	1	1	$w_2 + w_4 \geq \theta$	(6)
0	1	1	0	1	$w_2 + w_3 \geq \theta$	(7)
0	1	1	1	1	$w_2 + w_3 + w_4 \geq \theta$	(8)
1	0	0	0	1	$w_1 \geq \theta$	(9)
1	0	0	1	1	$w_1 + w_4 \geq \theta$	(10)
1	0	1	0	1	$w_1 + w_3 \geq \theta$	(11)
1	0	1	1	1	$w_1 + w_3 + w_4 \geq \theta$	(12)
1	1	0	0	1	$w_1 + w_2 \geq \theta$	(13)
1	1	0	1	1	$w_1 + w_2 + w_4 \geq \theta$	(14)
1	1	1	0	1	$w_1 + w_2 + w_3 \geq \theta$	(15)
1	1	1	1	1	$w_1 + w_2 + w_3 + w_4 \geq \theta$	(16)

From the inequality (1) of the 7th column in Table-2, we have θ is a positive number and from inequalities (2), (3), (5) and (9) we decide that w_1, w_2, w_3, w_4 are all positive as $\theta > 0$. If we assume that $w_1=1, w_2=1, w_3 = 1, w_4=1$ and $\theta = 1$, then all the sixteen inequalities in the 7th column in Table-2 are satisfied. So a solution set for $\{w_1, w_2, w_3, w_4 : \theta\} = \{1,$

$1,1,1,1\}$ is obtained. As a result, the Threshold logic equation for 4-input OR gate given in equation (4) can be written as equation (6) below. The respective threshold logic gate is drawn in Fig. 2(a). The corresponding simulation set and the simulation result are shown in Fig. 2(b) and 2(c) respectively.

$$Y(X_1X_2X_3X_4) = \text{sgn}(X_1 + X_2 + X_3 + X_4 - 1) \dots\dots\dots (6)$$

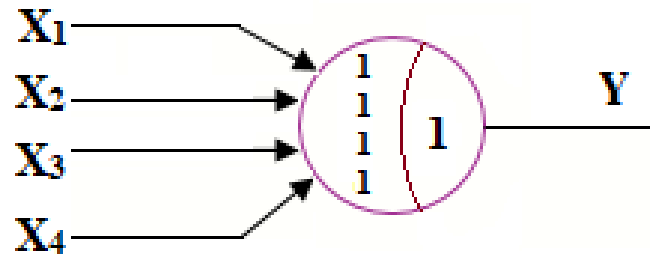


Fig. 2(a) TLG of $Y = X_1 + X_2 + X_3 + X_4 - 1$

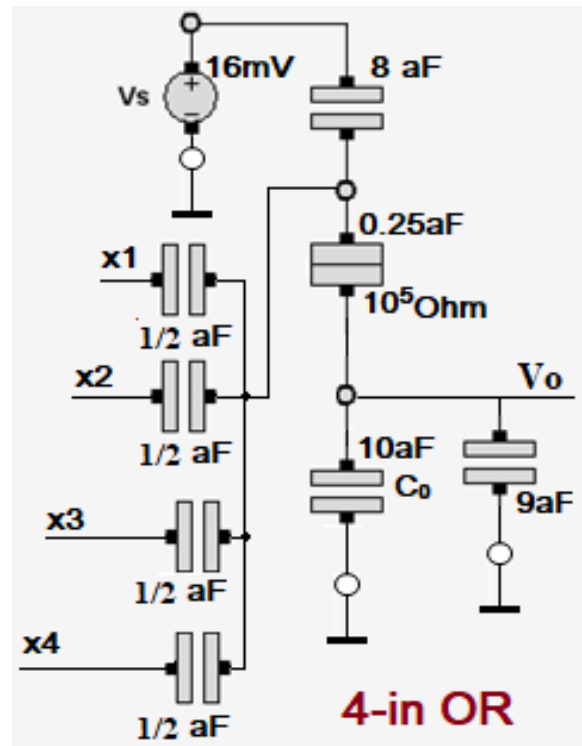


Fig. 2(b) Simulation set of 4-in OR gate

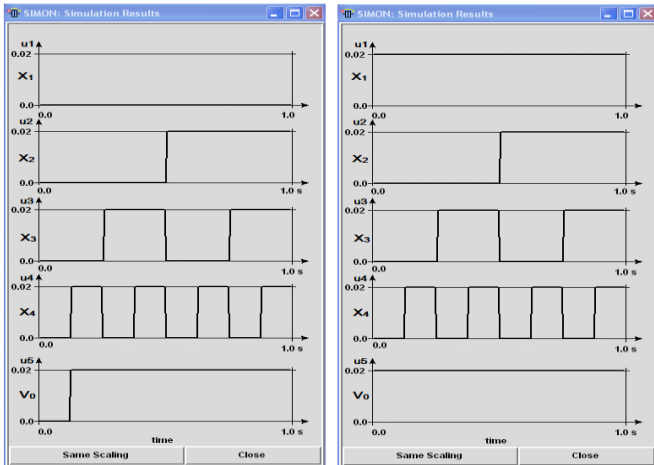


Fig.2(c) Simulation result of Fig. 2(b)

3. Inverter

An inverter that is capable of inverting its own input is shown in Fig. 3(a) [1-4, 8-10]. It is made up of 9 elements: 4 Tunnel junctions, 5 true capacitors; one supply voltage $V_s=16mV$, one input terminal and one output terminal. The inverter is constructed with two single electron transistors (SETs) which are connected in series. Upper two Tunnel junctions (J_1, J_2) and two true capacitors (C_g, C_b) belong to SET1. Similarly, The lower two Tunnel junctions (J_3, J_4) and two true capacitors (C_g, C_b) belong to SET2. Two inputs terminals (both V_{in}) are directly coupled to the small islands (small circles) of the SET1 as well as SET2 [1, 2, 8-10] through their respective capacitances C_g and C_g respectively. The island sizes of each SET are of size close to 10 nm diameter of gold and their respective capacitor values will be less than 10aF. The output terminal V_0 is directly connected to the common channel in between SET1 and SET2. The output terminal must be grounded through a load capacitance C_L to suppress charging effects.

When an inverter is used we should choose the parameter values as: $V_{g1}=0, V_{g2}=0.1 \times \frac{q_e}{C}, C_L = 9C, C_j = \frac{1}{10}C, 5C_j = \frac{1}{2}C, C_g = \frac{1}{2}C, C_b = \frac{17}{4}C, R_j=50K \Omega$. For the case of simulation, we take the value of $C = 1aF$. The simulation set and its simulation result are provided in Fig. 3(a) and 3(b) respectively.

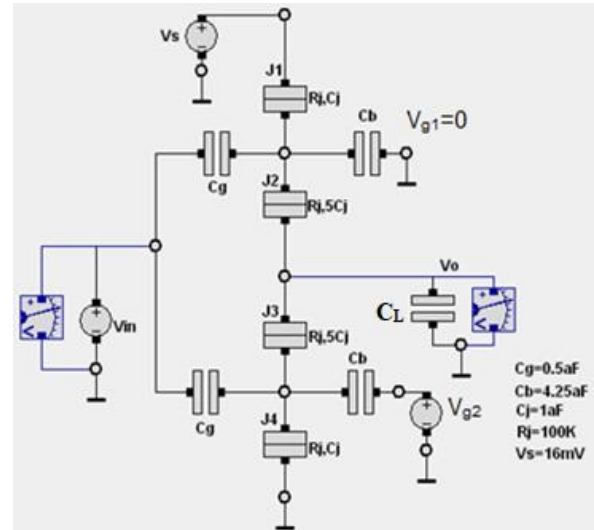


Fig. 3(a) Inverter based on parameters

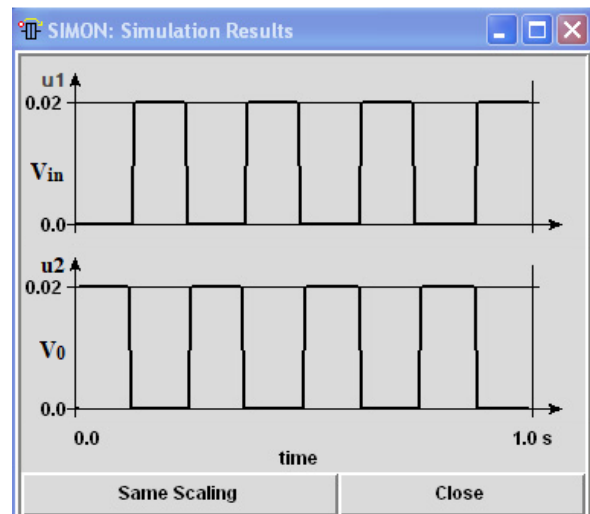


Fig.3 (b) Result after simulation of the inverter

We maintain the voltages $V_{g1} = 0$ and $V_{g2} = 16mV$ all time. The operation of the inverter can be marked as: - the output V_0 value will be 1 (logic high) provided that the input voltage V_{in} is low and that will be 0 (logic low) whenever the input voltage V_{in} is high. SET1 (upper part in fig. 3(a)) will be in conduction mode and the SET2 is in Coulomb blockade [1-5, 12] if the input signal V_{in} is connected to low (0). This causes the output voltage V_0 to connect to V_b , as a result the output voltage becomes high. When the input signal is high (logic 1), then the charges which is accumulated on each of the islands (for two SETs) are transferred by a fraction of an electron charge. By turns, SET1 turns up in Coulomb blockade mode and the SET2 turns up in conducting

mode. In these circumstances, we call that the output V_0 changes the condition from high to low (logic 0).

For high and low inputs, we use the logic inputs “0” =0 Volts and logic “1”= $0.1 \times \frac{q_e}{c}$.

For simulation purpose, we assume that $C=1aF$ and Logic “1”= $0.1 \times \frac{1.602 \times 10^{-19}}{1 \times 10^{-18}} = 0.1 \times 1.602 \times 10^{-2} = 16.02 \times 10^{-3} = 16.02 \cong 16$ mV.

4. Generic Multiple input threshold logic gate

A multiple threshold logic gate [1-10] which may also be called a generic Multiple input threshold logic gate is shown in Fig. 4.

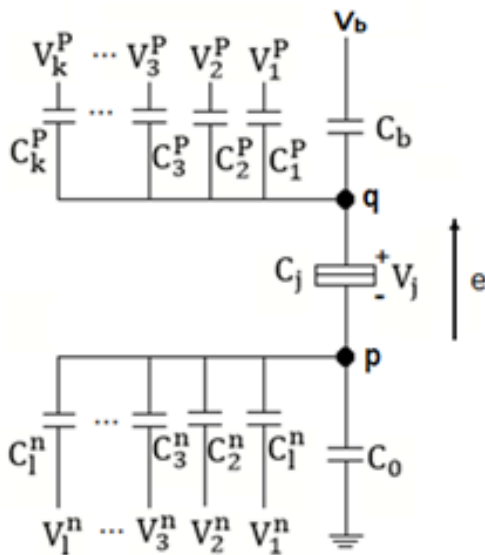


Fig.4 TLG with multi-input

It consists of a tunnel junction having internal capacitance C_j and resistance R_j , two multi-input-signals (i) V_k^p s and (ii) V_l^n s connected at two points ‘q’ and ‘p’ respectively. Each input voltage V_k^p (upper side) is connected to the point “q” through the capacitance C_k^p ; and each input voltage V_l^n (lower side), is joined at the point “p” through the capacitance C_l^n . The bias voltage V_b , for the assistance of the tunneling, is connected to the point “q” through the true capacitor C_b . Tunnel Junction capacitor C_j is linked between “p” and “q”. Point “p” is grounded through C_0 . C_j and C_0 play the important

role in the circuit. For a LTG, the operation of it can be expressed by a function called *signun function*. The *signun function* of $h(x)$ expressed by two equations (7a) and (7b).

$$g(x) = \text{sgn}\{h(x)\} = \begin{cases} 0, & \text{if } h(x) < 0 \\ 1, & \text{if } h(x) \geq 0 \end{cases} \dots\dots\dots (7a)$$

$$h(x) = \sum_{k=1}^n (w_k \times x_k) - \theta \dots\dots\dots (7b)$$

where x_k represents n-Boolean inputs, and w_k are their corresponding integer weights.

The LTG compares the threshold value θ with the weighted sum of the inputs $\sum_{k=1}^n (w_k \times x_k)$. When $\sum_{k=1}^n (w_k \times x_k)$ is more than or equal to the threshold value θ of the circuit, then output of the LTG shows high (logical “1”), otherwise low (logical “0”).

5. Characteristic equation of RS Flip:

For the sake of implementing a memory cell, a sequential circuit /a flip-flop is indispensable. In this section, an RS Flip-flop will be discussed. For tracing the characteristic equations of an RS Flip-flop, we draw the truth table of it, and with the help of the Karnaugh map, the characteristic equations of Q^{t+1} and \bar{Q}^{t+1} are written in the equations (8) and (9) respectively. The truth table is depicted in Table-3.

$$Q^{t+1} = \bar{R}Q^t + \bar{R}S \dots\dots\dots (8)$$

$$\bar{Q}^{t+1} = \bar{S}\bar{Q}^t + R\bar{S} \dots\dots\dots (9)$$

Table-3. Truth table for RS Flip-flop

R	S	Previous		New	
		Q ^t	\bar{Q}^t	Q ^{t+1}	\bar{Q}^{t+1}
0	0	1	0	1	0
0	1	1	0	1	0
1	0	1	0	0	1
1	1	1	0	invalid	
0	0	0	1	0	1
0	1	0	1	1	0
1	0	0	1	0	1
1	1	0	1	invalid	

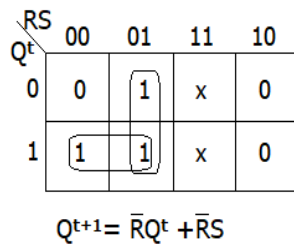


Table-4

R	S	Previous		New	
		Q ^t	\bar{Q}^t	Q ^{t+1}	\bar{Q}^{t+1}
0	0	1	0	1	0
0	1	1	0	1	0
1	0	1	0	0	1
1	1	1	0	1	0
0	0	0	1	0	1
0	1	0	1	1	0
1	0	0	1	0	1
1	1	0	1	0	1

It is translucent that Boolean gate based RS Flip-flop retains the unstable behavior when both of the inputs R and S are high i.e., R=S=1. This instability would occur only for the reason of the cross-connection of the two NOR gates. If we are able to construct an RS Flip-flop in the absence of cross-coupling gates, we will settle a solution to this instability problem. In this ambiances, when we are interested in designing the RS Flip-flop, it will cost more number of gates. Whereas when we are going to make the same thing with the help of TLG design, the gates required will be lesser.

A TLG based design of an RS Flip-flop can be constructed by means of a single threshold gate only. After a small modification [7, 8] of the equations (8) and (9) we obtain the Threshold gate equations (10) and (11) respectively, where there will not be any events of uncertainty.

$$Q^{t+1} = \bar{R}Q^t + \bar{R}S + SQ^t \dots\dots\dots (10)$$

$$\bar{Q}^{t+1} = R\bar{Q}^t + R\bar{S} + \bar{S}\bar{Q}^t \dots\dots\dots (11)$$

For the verification of equations (10) and (11), we draw a truth table in absence of giving the input condition R=1 and S=1 in Table-4.

Now for the implementation of an RS Flip-flop, we must substantiate that the functions (10) and (11) are satisfying the function of RS Flip-flop (in Table-4). If we select R=0 and S= 0, we obtain Q^{t+1}=Q^t (Hold). If we set R=0 and S= 1, we have Q^{t+1}= 1 (Set). If we set R=1 and S= 0, we get Q^{t+1}= 0 (Reset). If we set R=1 and S= 1, we have Q^{t+1}=Q^t (Hold). And for all cases, the output \bar{Q}^{t+1} becomes the complement of output Q^{t+1}. So we conclude that equation (10) and (11) meet the expectations of the characteristics of the RS Flip-flop without any forbidden input combinations R=1, S=1 or R=0, S=0 and both of these two combinations corresponding to Hold function.

If we are intended to implement the Boolean gate based logic circuit of the equation (10) we need three 2-input AND gates and one 3-input OR gate. On the other hand if somebody wants to implement it by means of TLG based circuit, a 3-input threshold gate becomes adequate to implement the same Boolean equation (10).

For the purpose of constructing a 3-input RS Flip-flop based on TLG, we first think of Threshold logic equation (12) of a 3-input RS Flip-flop gate of three variables \bar{R} , S and Q^t. We draw the Truth table-5 of the equation (10). For the threshold logic equation of equation (10), we can write as

$$F(\bar{R}, S, Q^t) = \text{sgn}(w_1\bar{R} + w_2S + w_3Q^t - \theta) \dots\dots\dots (12)$$

For getting the threshold logic equation of 3-input RS Flip-flop ($Q^{t+1} = \bar{R}Q^t + \bar{R}S + SQ^t$), the logic variables (\bar{R} , S and Q^t) for the positive logic will be taken as 1 each and the equation (12) will be as

$$F(\bar{R}, S, Q^t) = \text{sgn}(w_1 + w_2 + w_3 - \theta) \dots\dots\dots(13)$$

Table-5

\bar{R}	S	Q^t	output Q^{t+1}	θ	Eqn. no.
1	0	1	1	$w_1 + w_3 \geq \theta$	(1)
1	1	1	1	$w_1 + w_2 + w_3 \geq \theta$	(2)
0	0	1	0	$w_3 < \theta$	(3)
0	1	1	1	$w_2 + w_3 \geq \theta$	(4)
1	0	0	0	$w_1 < \theta$	(5)
1	1	0	1	$w_1 + w_2 \geq \theta$	(6)
0	0	0	0	$0 < \theta$	(7)
0	1	0	0	$w_2 < \theta$	(8)

We assume the positive logic, for this reason, we will take all the coefficients of \bar{R} , S, Q^t i.e., w_1 , w_2 , w_3 and θ are positive. If we take, $w_1=1$, $w_2=1$, $w_3=1$ and $\theta=2$, then all the 8 conditions in the 6th column in Table-5 are satisfied. So, one solution set is $\{w_1, w_2, w_3: \theta\} = \{1, 1, 1: 2\}$. The threshold logic equation of equation (13) is given in equation (14).

$$Q^{t+1} = \text{sgn}\{\bar{R} + S + Q^t - 2\} \dots\dots\dots(14)$$

We know that $R + \bar{R} = 1$ or $R = -\bar{R} + 1$ or $\bar{R} = -R + 1$, so the above equation becomes

$$Q^{t+1} = \{-R + S + Q^t - 1\} \dots\dots\dots(15)$$

According to the threshold logic equation (15), the threshold logic gate is drawn in Fig. 5. For the verification of the correctness of equation (15) and a truth Table-6 is provided.

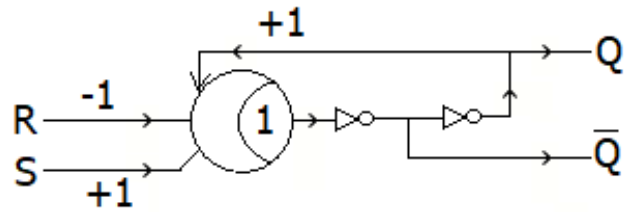


Fig.5 TLG based RS Flip-flop for eqn. (15)

Table-6. Verification of the correctness of equation (15)

R	S	Q^t	Q^{t+1}	function
0	0	0	0	Previous value
0	0	1	1	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	0	Previous value
1	1	1	1	

The RS Flip-flop which we have proposed has been theoretically proven and justified by using the simulator. The simulation set and the simulation results are shown in the Fig. 6(a) and Fig. 6(b) respectively. We have obtained the Simulation results by using the circuit parameters stated below: for the threshold logic gate logic input “0”=0V, logic “1” = 16mV,

$$C_1^p(w_1 = 1) = C_2^p(w_2 = 1) = 0.5aF, C_1^n(w_3 = -1) = 0.4aF, C_3 = 12.7aF, C_L = 9aF, C_0 = 8.6aF, R_j = 10^5 \Omega, V_s = V_b = 16mV. \text{ For the buffer, the parameters taken are, } C_{g1} = C_{g2} = 0.5aF, C_1 = C_4 = 0.5a, C_2 = C_3 = 0.1aF, C_{b1} = C_{b2} = 4.25aF, C_L = 9aF, R_j = 50K\Omega, C_j = 0.1aF.$$

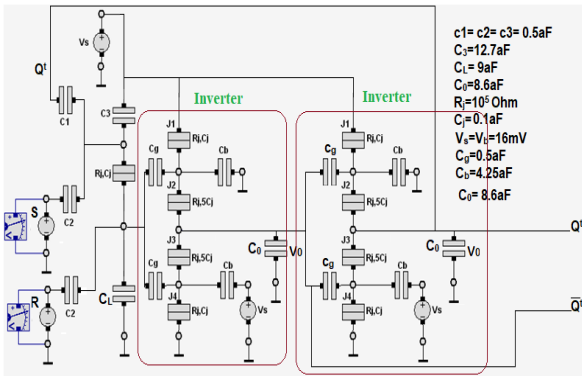


Fig. 6(a). LTG based RS Flip-flop

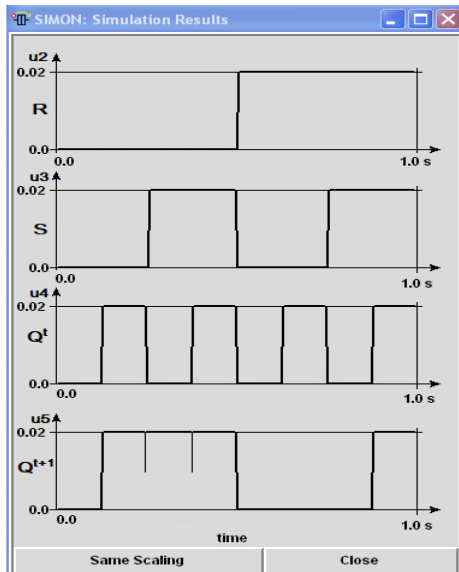


Fig. 6(b) R & S-input, Previous Q^t , Q^{t+1} =New Q^t

6. Memory Decoding

In the IC Random Access Memory, there would be the main component -- Memory unit and another component called decoder which is required to select the memory words to be written to or read from the memory unit using its Address lines and enable line. In this section, we present the internal construction of a 2×4 Decoder (in Fig. 7) which is made up of four 3-input AND TLGs and two inverters. There are two Address lines, one enable line and four output lines from D_0 to D_3 . When we are able to include decoder and the memory in one diagram in a special pattern, then the operation of storing words in the memory unit and taking out the binary data in a word will be easy. The memory unit presented in Fig. 8(a), bears a small capacity of 12 bits arranged in 4 words of 3 bits

each. In addition to the internal decoder shown in Fig. 7, a memory unit may require external decoders. The reason of it is that when integrated-circuit RAM chips are connected in a multichip memory configuration, the external decoders will act for selecting the different RAM chips.

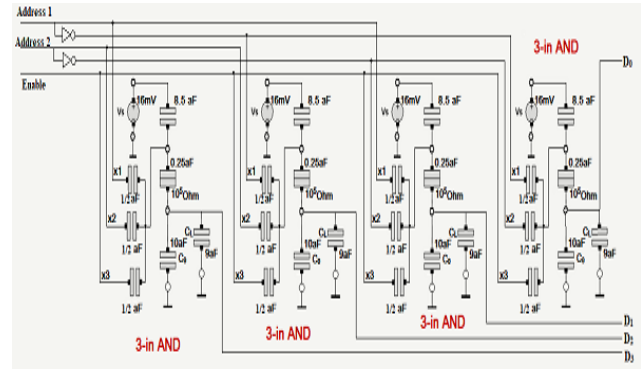


Fig.7 A 2×4 Decoder

7. RANDOM ACCESS MEMORY

A random access memory (RAM) with its internal construction is enlightened in this section. This RAM is constructed with the help of sequential circuit called Flip-flops, and logic gates based on TLGs. To be able to involve complete memory unit in a diagram, a restricted capacity (in size) will be used. This is why the memory unit depicted herein has a small size of $3 \times 4 = 12$ bits of pattern in four words having three bits each. Commercial RAM can have potency of thousands of words and every one word may range somewhere in the range between 8 and 128 bits. For a large capacity memory unit, its logical construction will be a straight extension of the configuration given here.

8. (A) Internal Construction of a Memory for an Integrated-circuit

A RAM of $m \times n$ binary storage cells has m words with n bits per word and an associated decoding circuit in support of selecting individual words. The building block of a memory unit is the binary storage cell.

The equiponderant logic of a binary memory cell storing a single bit of information is given in Fig. 8(a) and the symbol of this binary memory cell (MC) is shown in Fig. 8(b).

A binary memory cell should be small enough so that the manufacturer will be able to pack as many cells as possible in the region available for the IC chip. The binary memory cell can store one bit information in its flip-flop/latch. The memory cell contains one data-input, one selection-input, on read/ write input and one output.

The memory-enable input in Fig. 9 enables the memory cell to write or read and the read /write input enables the memory cell operation whenever this is selected. A high signal in the read / write input makes the read operation by creating a path from the flip-flops to the output terminals. Similarly, a low signal (0) in the read /write input makes the write operation by creating a bus from the input terminals to the flip-flops. The flip-flop, here, operates in the absence of a clock and is equivalent to an SR latch as in Fig. 8(a) and Fig. 9.

The logical configuration of an IC RAM of 12 bits is shown in Fig. 9. It is having 4 words of 3 bits each and a total number of 12 binary cells. Each block marked by MC (memory cell) is the representative of the binary memory cell along with its three inputs and one output, as shown in in Fig. 8(b). A memory of four words requires two address lines. The two address input lines pass through a 2×4 decoder in order to select one of the four words Word(0), Word(1), Word(2) and Word(3). The 2×4 decoder is enabled with the help of the memory-enable input. When the memory-enable = 0, all outputs of this decoder will be 0 and the memory words are not selected. When the memory-enable signal= 1, one of the four words will be selected under the direction of two address line values of Address1 and Address 0. When a word is selected, the read /write input signal fixes the operation. During the time of read operation, the all three bits of the selected word pass through 4-input OR gates to the output terminals Data (2), Data (1) and Data (0) in Fig. 9. At the time of write operation, the data present at the input lines are passed into the three binary memory cells (MCs) of the selected word. The non-selected binary cells are disabled and their respective previous binary values remain unaltered. When the memory-enable input in the decoder = 0, none of the words are identified and the contents of all cells remain unaltered irrespective of the value of the read /write input.

The different parameters utilized in different logic circuits are listed in Table-7 above.

Table-7

Sl. No.	Expressions used & Name of Expression	parameters
1	$Q^{t+1} = \{-R+S+Q\} \cdot 1$ RS Flip-Flop	logic input "0"=0V, logic "1" = 16mV, $C_1^p(w_1 = 1) = C_2^p(1) = 0.5aF, C_1^r(w_2 = -1) = 0.4aF, C_2^r = 12.7aF, C_1 = 9aF, C_0 = 8.6aF, R_j = 10^5 \Omega, V_s = V_b = 16mV$. For the buffer, the parameters taken are, $C_{g1} = C_{g2} = 0.5aF, C_1 = C_4 = 0.5a, C_2 = C_3 = 0.1aF, C_{g1} = C_{g2} = 4.25aFv, C_L = 9aF, R_j = 50K\Omega, C_c = 0.1aF$.
2	$F(X_1, X_2, X_3) = \text{sgn}(X_1 + X_2 + X_3 - 3)$ 3-input AND gate	logic input "0"=0V, logic "1" = 16mV, $C = 1aF, C_1^p = C_2^p = C_3^p = \frac{1}{2}C = 0.5aF, C_b = 8.5aF, C_j = 0.25aF, C_L = 9aF, C_0 = 10aF, R_j = 10^5 \Omega, V_b = V_s = 16mV$
3	$Y(X_1, X_2, X_3, X_4) = \text{sgn}(X_1 + X_2 + X_3 + X_4 - 1)$ 4-input OR gate	"0"=0V, logic "1" = 16mV, $C = 1aF, C_1^p = C_2^p = C_3^p = C_4^p = \frac{1}{4}C = 0.25aF, C_b = 8aF, C_j = 0.25aF, C_L = 9aF, C_0 = 10aF, R_j = 10^5 \Omega, V_b = 15.81mV, V_s = 16mV$
4	$Y \leftarrow \bar{Y}$ Inverter	For the inverter, the parameter values chosen are: $V_{g1} = 0, V_{g2} = 0.1 \times \frac{V_s}{C}, C_L = 9C, C_j = \frac{1}{10}C, 5C_j = \frac{1}{2}C, C_g = \frac{1}{2}C, C_b = \frac{17}{4}C, R_j = 50K\Omega$. For the sake of simulating, the value of $C = 1aF$ is fixed.

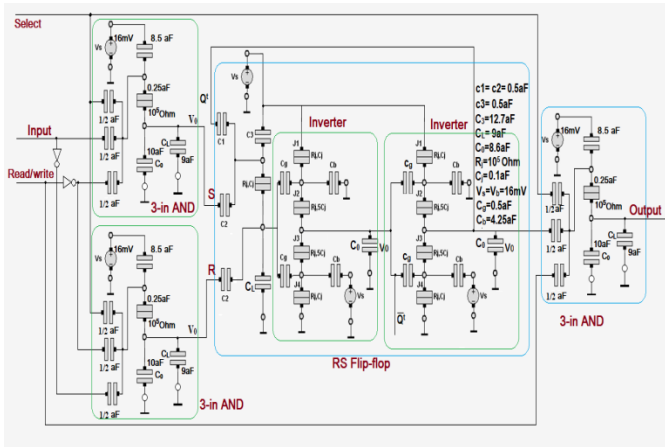


Fig. 8(a) A Memory cell

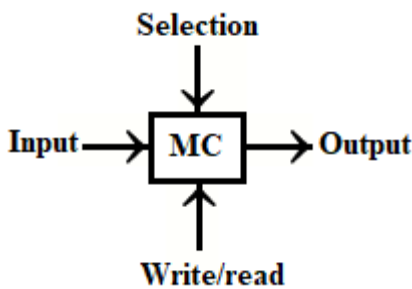


Fig. 8(b) MC (memory cell)

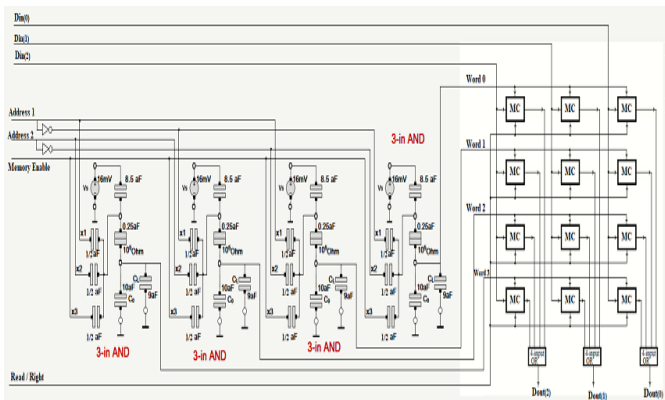


Fig. 9 Logical construction of an IC for a 4x3 RAM
The operational input –output data of the circuit IC RAM of Fig. 9 are listed in the Table-8

Table-8

Read/ write operation

Initially data stored in memory as					
Word 0 = 1 0 1					
Word 1 = 1 1 0					
Word 2 = 1 1 1					
Word 3 = 0 0 1					
Memory -enable	Read/write	Addr 1	Addr 0	Input D ₍₂₎ D ₍₁₎ D ₍₀₎	Operation
1	1	0	0	Any value	1 0 1
	1	0	1		1 1 0
	1	1	0		1 1 1
	1	1	1		0 0 1
Memory -enable	Read/write	Addr 1	Addr 0	Input D ₍₂₎ D ₍₁₎ D ₍₀₎	Operation
1	0	0	0	Any value	1 0 0
	0	0	1		1 1 0
	0	1	0		0 1 1
	0	1	1		0 0 1
0	x	x	x	Any value	No operation

8 (B) Simulation result of IC RAM

READ OPERATION: Assuming that the data stored in the memory words as: - Word 0 = 1 0 1; Word 1 = 1 1 0; Word 2 = 1 1 1 and Word 3 = 0 0 1 as depicted in Fig. 9(a). As the data are available in the memory cells (MCs) we will be able to read/retrieve data from the memory. For doing so, we set Memory-enable =1 and Read/write=1, irrespective of the data input values, when we apply the Address1 input and address2 input as 00, 01, 10 and 11, we obtain the outputs given in Fig. 9(b).

WRITE OPERATION: Now we wish to write data in the memory. Which data we have read from the memory are also retain intact if the Read/Write input value is not 0. We set Memory-enable =1 and Read/write=0, now we will be able to write data in the memory though the previous stored data are still available. That is new data will replace the previous data according to the Address lines input values. If we apply the Address1 input and address 2 input values as 00, 01, 10 and 11, the corresponding input data given in Fig.9(c) will be stored in the corresponding

word bit positions. The data stored in the memory cells are given in Fig. 9(d).

NO OPERATION: If we put Memory-enable = 0, memory will not be selected and **Read** and **Write** operation will not be performed but the data previously stored in the memory will remain unchanged.

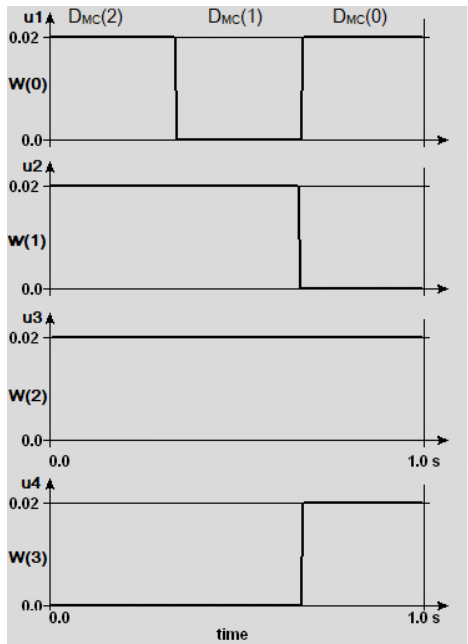


Fig. 9(a) initial stored data

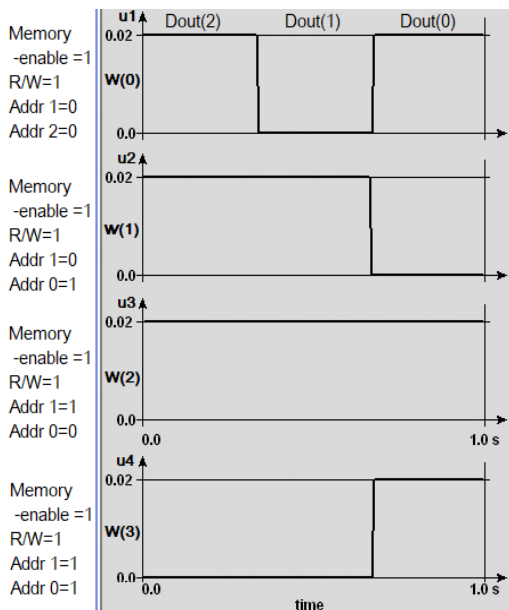


Fig. 9(b) Read Data from memory

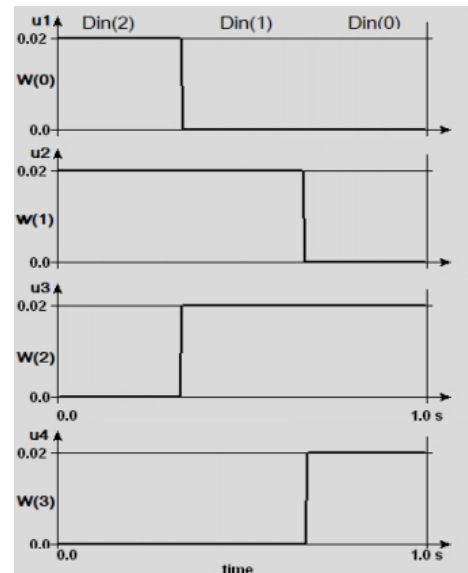


Fig.9(c) input Data for Words (0-2)

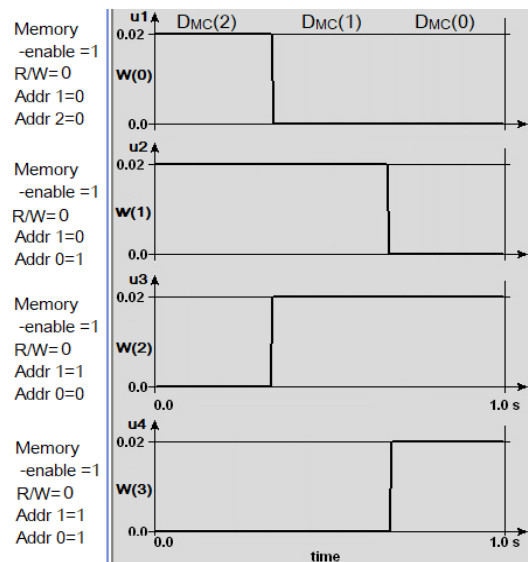


Fig. 9(d) Write Data in Memory

Discussion relating to Delay, Switching energy and Fastness

When implemented a circuit regarding a device, some inevitable components are gathered, and joined them properly to make it. Similarly, for the case of Integrated-Circuit Random Access Memory (IC RAM), 3-input AND gate, 4-input OR gate, 2 × 4 Decoder, RS Flip-flop and inverter are absolutely necessary. An Integrated-Circuit RAM is implemented by using the components as cited above. Efficiency of a device counts upon various factors like time for execution, number of components considered

essential, costs of materials, fan-outs, speed, power consumption, controlling charge, atmospheric temperature etc. First we measure the processing delays cum latency of all the components used in our work. For calculating the processing/switching delays, we are to entangle the critical voltage V_c along with the tunnel junction capacitance C_j of the linear TLG. This delays with respects to logic gate/circuit may be calculated by the approaches [1-3, 9, 10] given below.

$$\text{Delay} = -(e|\ln(P_{error})|R_t) / (|V_j| - V_c) \dots\dots (16)$$

Here, R_t is being the internal junction resistance, V_j is the tunnel junction voltage and V_c is the critical voltage. Execution of the circuit occurs only when a tunneling event occurs i.e., an electron passing through the tunnel junction. The tunneling event occurs only when the tunnel junction voltage V_j applied is more than or equal to the internal critical voltage V_c , i.e., when $|V_j| \geq V_c$. As soon as this conditional expression is fulfilled by a 4-input OR gate, junction voltage of the 4-input OR gate becomes $V_j = 11.8\text{mV}$, the internal critical voltage V_c of the tunnel junction is found to be 11.58mV . The parameter values of tunnel resistance $R_t = 10^5\Omega$ and the probability of error $P_{error} = 10^{-12}$ are given. Putting these values into equation (16) we measure the gate delay $=0.078|\ln(P_{error})|\text{ns} = 2.15\text{ns}$. In this same way we can find out the delays of different gates/ circuits and they are listed in Table-7 and 8.

While tunneling, an electron goes through the junction barrier, then the total energy in the circuit is varied. The energy levels, before and after a tunneling event are measured by using the equation (17).

$$\begin{aligned} \Delta E &= E_{\text{before tunnel}} - E_{\text{after tunnel}} \\ &= -e(V_c - |V_j|) \dots\dots\dots (17) \end{aligned}$$

This switching/tunneling energy $-e(V_c - |V_j|)$ is consumed for a tunnel event in the tunneling circuit. We have listed the energy consumptions as regards different TLG circuits in Table-9.

Table-9

Gate/Device	n-elements	Delay (ns)	Switching Energy meV
inverter	9	$0.022 \ln(P_{error}) $	10.40
2-in NOR	6	$0.060 \ln(P_{error}) $	10.70
2-in OR	6	$0.062 \ln(P_{error}) $	10.80
2-in NAND	6	$0.062 \ln(P_{error}) $	10.80
2-in AND	6	$0.062 \ln(P_{error}) $	10.80
3-in AND	7	$0.072 \ln(P_{error}) $	11.58
3-in NAND	7	$0.072 \ln(P_{error}) $	11.58
2-in XOR	13	$0.080 \ln(P_{error}) $	21.20
3-in OR	7	$0.073 \ln(P_{error}) $	11.58
3-in NOR	7	$0.072 \ln(P_{error}) $	11.57
4-in OR	8	$0.078 \ln(P_{error}) $	14.22
RS Flip-flop	24	$0.136 \ln(P_{error}) $	32.42
2 x4 Decoder	28	$0.216 \ln(P_{error}) $	34.74
MC	42	$0.210 \ln(P_{error}) $	76.34
IC RAM	572	$0.360 \ln(P_{error}) $	676.72

Two curves have been traced apropos of the switching delay vs. switching error probability in Fig. 10(a) and the switching delay against the unit capacitance $C (=1\text{aF})$ in Fig. 10(b) below.

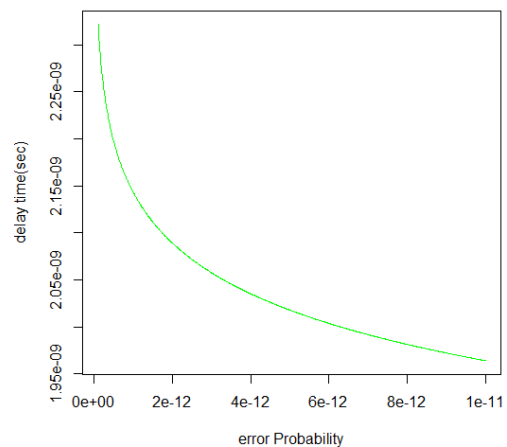


Fig. 10(a) Delay vs. Error Probability

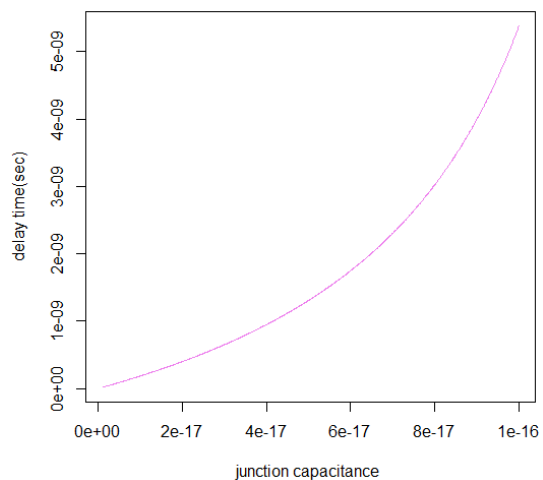


Fig. 10(b) Delay Vs. capacitance

The total number of small elements like capacitors, resistors to construct a gate or circuit is counted. We keep track of the data obtained from this work in connection to small element numbers, delays or late, and switching power and all of them are given in Table-9. Power consumption (meV) versus elements is shown in Fig. 11 below. The delays of SET and TLG based circuits with respect to the distinct elements are projected using the bar diagram in Fig. 12.

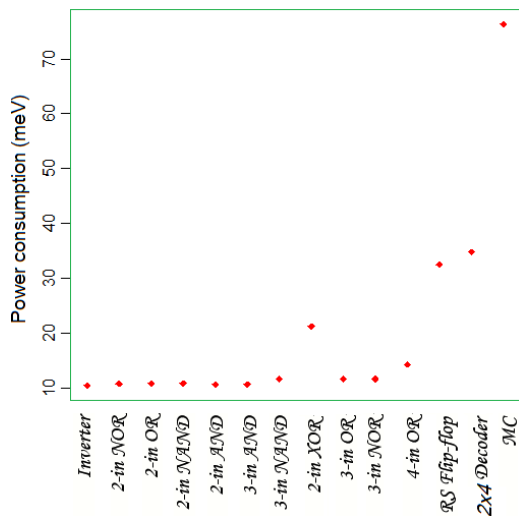


Fig.11 Comparison of small Elements and switching energy

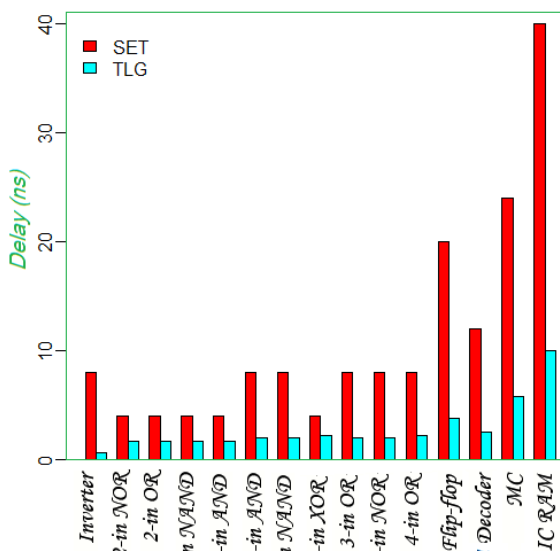


Fig. 12 Delays of SET/TLG Vs. gates

The execution delays for various TLG based circuits must be distinct. For instance, for 2-input XOR gate the latency becomes 2.21 ns, for the 3-input OR gate the processing delay is 2.01 ns, and in IC RAM delay is 9.94 ns.

It is considered that the value of $P_{error} = 10^{-12}$, so the time after which the first output of the Integrated-Circuit Random Access Memory will fan out is $0.360|\ln(P_{error})| = 9.94ns$. Hence, we surely maintain the Address signals time i.e., after every 9.94ns ns or more we should apply the Address(1) and Address(2) signals of the 2x4 Decoder connected in IC-RAM circuit. In this condition, frequency of fan out of the Integrated-Circuit Random Access Memory circuit will be $1/9.94 ns = 100.6 MHz$.

We are intended to find out the circuit delays with regard to CMOS, SET-based and LTG-based. We have obtained the processing delays in case of a CMOS logic gate for AND, NAND, NOR, XOR is 12ns [1-5, 9, 10]. The tunneling time delay through a single electron transistor (SET) [10, 11] is approximately 4ns [4-7, 13-14]. The speed-up times of LTG-based delays with respect to the corresponding delays of SET-based delays are listed in Table-10 and the three graphs of (i) SET-based delay, (ii) LTG-based delay and (iii) Speed-up times with respect to the distinct logic gates / circuits are provided in Fig.13.

Table-10

Gate/Device	SET-based delay ns	LTG-based delay ns	Speed-up times
inverter	8	0.60	13.33
2-input NOR	4	1.65	2.42
2-input OR	4	1.71	2.33
2-input NAND	4	1.71	2.33
2-input AND	4	1.71	2.33
3-input AND	8	1.98	4.04
3-input NAND	8	1.98	4.04
2-input XOR	4	2.21	1.81
3-input OR	8	2.01	3.98
3-input NOR	8	1.99	4.02
4-input OR	8	2.15	3.72
RS Flip-flop	20	3.75	5.33
2 x4 Decoder	12	2.54	2.52
MC	24	5.80	4.1
IC RAM	40	9.94	4.02

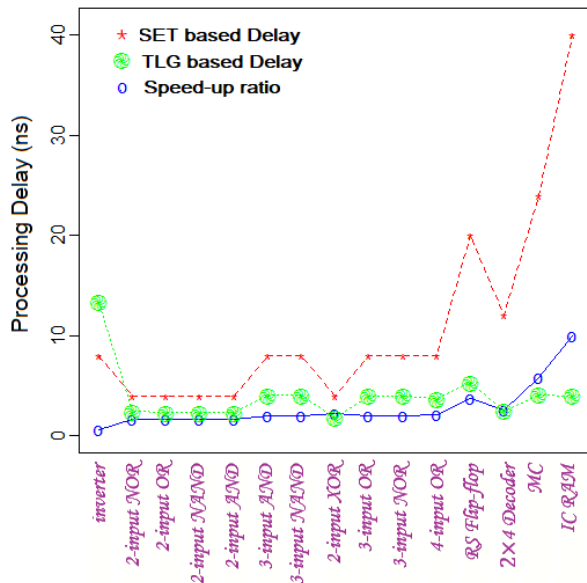


Fig. 13 Delays of SET- and TLG- based and their ratio

Switching delays of SET and LTG

Assume that the probability of error is 10^{-12} , the processing late /delays for different gates/circuits we have measured are given in Table-10. From the Table-10, we can easily get that the LTG based circuit is at least 2 times faster than the SET based circuit. And pertaining to CMOS, the LTG based circuit is at least 8 times faster than that.

III. CONCLUSION

An IC RAM is implemented which is volatile i.e. data will be present in this Memory unit till the power supply exists. With proper power supply, we can store data in the memory and the stored data can be retrieved with the help of memory-enable and address lines of the decoder connected to the memory unit. As the tunnel junction is very small in size (nm), the concentration density of the TLG based nodes in a chip must be high. The power required for processing a single bit in this ram is $676.72\text{mev} = 676.72 \times 10^{-3} \times 1.602 \times 10^{-19} = 1.084 \times 10^{-25}$ Joule which is, no doubt, very low. From the comparison result of the processing delay, it is found that the TLG-based circuit is at least 2-times faster than the SET based

circuit and 8-times faster than CMOS based circuits. In our investigation, it is observed that after every 9.94ns one output bit is fanned out from the output terminal. Hence, the fan-out is 100.6MHz. Almost all the circuits are verified by the simulator-SIMON and found that the simulated results are matched with the theoretical observations. The prime drawback of single electron tunneling based linear threshold logic technology is that the temperature of the environment will be kept close to 0K and it is a big challenge.

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