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Parallel Comparator based voltmeter using Single Electron Tunneling Transistor

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ABSTRACT

By manipulating an electron that tunnels the tunnel junction of a single electron transistor, one will be able to reach a standard output logic "1" or logic "0". The operation of the Single Electron Transistor (SET) is depending upon the bias voltage as well as the input signal(s). By varying the input voltage levels of a SET, the output voltage levels can significantly be changed on the basis of tunneling of an electron whether tunneling happened or not. As our concentration is the measuring of an unknown voltage, we are to implement a voltmeter system to provide a digital output of 3 bits whenever an unknown input voltage is kept in touching in the input terminal. A reference/standard voltage (say 8mV) will be connected in series with eight resistances (8 Rs) for the purpose of making a seven threshold voltages, for 7 comparators, in an ascending order of values from ground to reference voltage for seven comparators which are used in this present work. The voltmeter implemented consists of (i) a voltage divider, (ii) a set of seven comparators, (iii) seven Exclusive-OR gates and (iv) three 4-input OR gates. The concepts of implementing "Parallel Comparator based voltmeter" is discussed in two ways (i) by classical block diagram and (ii) using Single electron transistor based circuit. The measuring of an input analog voltage will not be the same as the digital output value. A 3-bit output indicates that the input analog voltage must lie on within a particular small range of voltage. The encoder circuit which is connected to the outputs of the comparators is hard to construct whenever the three terminals output are expressed with the output variables (Wi) of the comparators. For simple and user-friendly circuit, the outputs (Wi) of the comparators are modified to Di variables so as to get the same 3-bit encoder/voltmeter output. For this purpose, 7 extra component called 2-input XORs based on SET are used. Seven such XORs are set, and the output of them are passed to three 4-input OR gates according to the required logic expressions. It is found that all the output data of the voltmeter are coherently matched with the theoretical aspects. Processing delays are found out for all circuits. Power consumptions

of all of them are shown in tabular and graphical forms. All the circuit we are intending to make are provided in due places with their logic circuit or simulation set and the simulation results are provided as well. Different truth tables are given for keeping track of whether input-output relationships matches with the theoretical results. We have thought of whether the present work circuits are faster or slower than the circuits of CMOS based-circuits. The power consumed at the time of tunneling event for a circuit is measured and sensed that it exists in the range between 1×10^{-18} Joules to 22×10^{-18}Joules which is very small amount. All the combinational circuits presented in this work are of SET-based.

Keywords: Electron-tunneling, SET, Comparator, Voltmeter, high-speed

I. INTRODUCTION

Persons involved in manufacturing the digital logic circuits wants to decrease the manufacturing cost, to reduce the concentration density, to increase fan-out rate and to light the weight. In lieu of classical CMOS circuit, the SET-based circuit can perform the above cited qualities. This is why we are interested in making a SET-based combinational circuit called parallel comparator based voltmeter. Another single electron tunneling based Technology termed as linear Threshold Logic Gate (TLG) can be used to do the same work done in this work. Linear threshold logic gate (TLG) is taken into account only at the time of comparisons with CMOS and SET circuits. Some SET based circuits are made and they are simulated and the digital outputs are provided. Step by step we have discussed about single electron transistor, Tunnel junction, an inverter, Simulation set of inverter, comparator, analog to digital converter and voltmeter.

II. METHODS AND MATERIAL

1. Single electron transistor & Coulomb blockade

A tunnel junction consists of a thin insulating barrier that is sliced in between the two conducting electrodes. The tunnel junction is given in Fig.1 (a). The electrodes for a tunnel junction may be semiconducting or superconducting; if they are superconducting, electrons with one elementary charge (1.602×10^{-19} Coulomb) can carry the current. In classical electrodynamics, current can't flow through an insulating barrier. But in the case of quantum mechanics, there must be a non-disappearing (i.e., more than zero) probability for an electron residing one side of the barrier to reach the other side of it. If proper bias voltage is applied, there will be a current flow. Neglecting additional effects, in accordance with first-order–approximation-tunneling, current is proportional to the applied bias voltage. Regarding electrical terms, a tunnel junction shows the nature of a resistor bearing a constant value relying upon the barrier thickness. Whenever two metals or conductors are connected with an insulating slice between them, there will be not only a resistance but a capacitance as well. In this context the tunnel junction acts as a capacitor and the insulator as dielectric. For the discrete nature of electric charge, current which follows through a tunnel junction is a series of events in which merely one electron can pass or tunnel through the tunnel junction. As soon as an electron tunnels through the junction, the tunnel capacitance gets charged with an

elementary charge (1.602×10^{-19} Coulomb) building up a voltage V = $\frac{e}{C}$, C = junction capacitance. When the capacitance of the tunnel junction gets drastically small, the voltage developed in the tunnel junction may be enough to obstruct another electron to pass. No current will flow as the bias voltage is smaller than the voltage developed in the tunnel junction and the resistance of the device will no longer keep constant. The raise of the differential resistance relating to the tunnel junction around (0) zero bias is called the Coulomb blockade [2-7, 19].

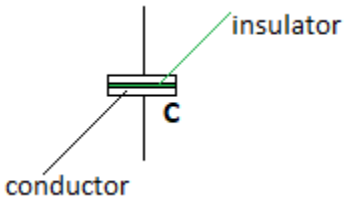

Fig.1 (a) Tunnel Junction

The principle of single-electronics [1, 8-13] is developed on the basis of the Coulomb blockade and single electron tunneling. SET circuits seems to be a promising candidate for future VLSI circuits for its ultra-small size, very small power consumption, reducing number of node capability and rich functionality.

A single electron Transistor (SET) [1-5, 14-15] with two tunnel junctions is shown in Fig. 1(b). The SET consisting of two tunnel junctions of internal values (C1, R1) and (C2, R2) respectively, shares only a common inland having a low capacitance.

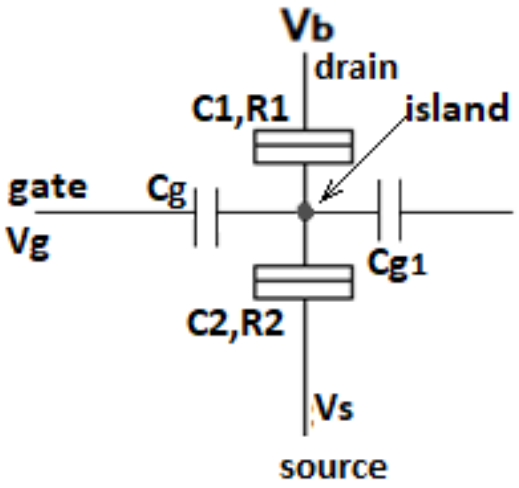

Fig.1 (b) Single Electron Transistor (SET)

The electric potential of the island can be tuned (i.e, increased or decreased) by a third electrode, defined as gate, which is coupled through capacitance Cg to the island. For the purpose of adjusting the gate (input) voltage, an extra capacitance C_{g1} may be connected intentionally to the island. The source, drain, and gate voltages are indicated by V_s, V_b and V_g respectively. For undisturbed operations of a SET, both of the resistances R1 and R2 of two junctions, must be greater than $R_q = h/e^2 \approx 25.8$ KΩ and charging energy $E_C = e^2/2C$ [where C = C1+C2+Cg+Cg1] has to be greater than thermal fluctuations kT, i.e, $E_C = \frac{e^2}{2C} > kT$, the product of the Boltzmann constant, k, and the temperature, T. The Boltzmann constant (k) value is 1.380649×10^{-23} Joule / Kelvin (J/K), or 1.380649×10^{-16}Erg / Kelvin.

2. Inverter based on SET

An inverter [1-10, 18] based on SET is shown in Fig. 2(a) consists of two SETs which are connected in series. Two input voltages of same values V_{in} are directly coupled to the two islands (SET1 and SET2) through two capacitors C_1 and C_2 respectively. The islands of the two SETs are made up of small size of gold of diameter ~10nm having total capacitance of C_{tot}=1pF. The two extra gates V_{g1} and V_{g2} may be used, if necessary, to the islands of SET1 and SET2 through two capacitors C_{g1} and C_{g2} respectively for

the purpose of tuning the induced charges on the islands of SET1 and SET2. The output terminal V_0 is joined to the middle of the common path of the two SETs and to the ground through a capacitor C_L to put down charging effects. The symbol of the inverter is given in Fig. 2(b).

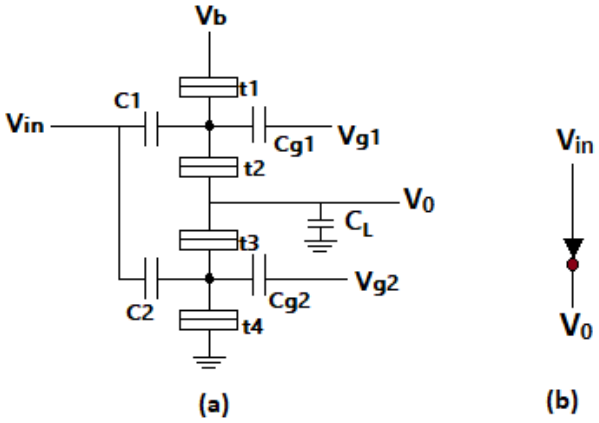

Fig.2 (a) An Inverter 2**(b)** its symbol

The inverter having the parameter-values are as follows: V_{g2}=0, V_{g2}=0.1$\times\frac{q_e}{C}$, $C_L = 9C$, $t_4 = \frac{1}{10}C$, $t_3 = \frac{1}{2}C$, $t_2 = \frac{1}{2}C$, $t_1 = \frac{1}{10}C$, $C_1 = \frac{1}{2}C$, $C_2 = \frac{1}{2}C$, $C_{g1} = \frac{17}{4}C$ and $C_{g2} = \frac{17}{4}C$, R1 =R2=100KΩ. For the simulation purpose, the value of C is chosen as =1aF.

The tunneling operation of the inverter will be like this: V_0 value will be low when the input voltage is high and the output V_0 value will be high when the input voltage V_{in} is low. While achieving this target, the voltages $V_{g1} = 0, and\ V_{g2}$ =16mV are set, the tuning input gate voltage V_{in} for SET1 and SET2 are provided. The SET1 will be in conduction mode, at the same time the SET2 is in Coulomb blockade provided that V_{in} is low.

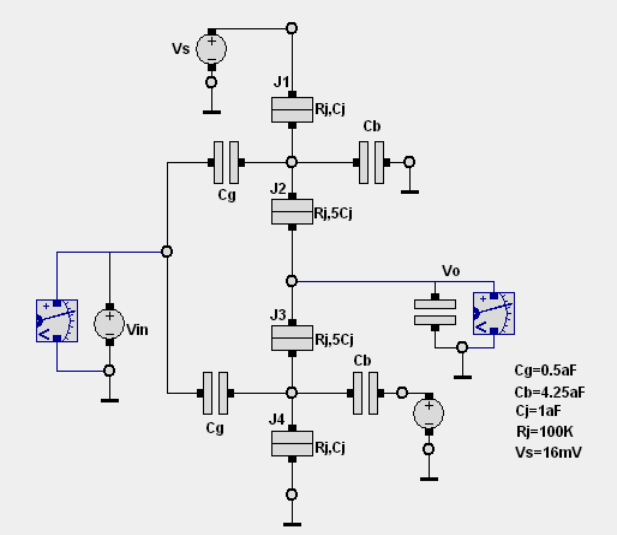

Fig. 2(c) Simulation set of Inverter

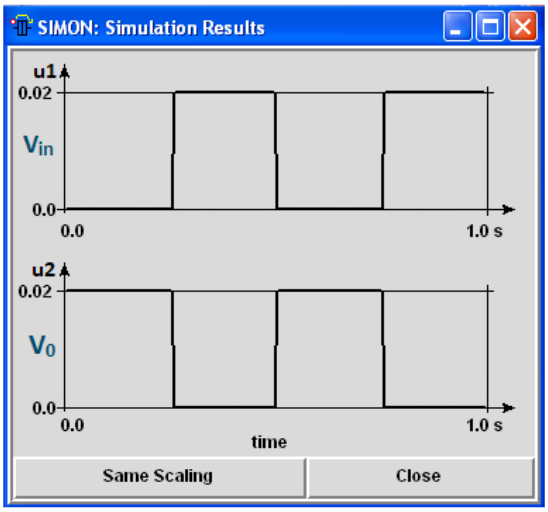

Fig.2 (d) Simulation result of Inverter

In this case, the output terminal gets virtually connected to V_b, as a result the output gets logic high, i.e, this effectively connects the output terminal to the supply voltage and makes the output level high. Coulomb blockade disturbs the steady flow of current provided the logic "1" is applied to the input V_{in}, it causes to move a fraction of an electron charge induced on the islands of these SETs and forces the SET1 to keep in Coulomb blockade and the SET2 in conducting mode. Since the lower transistor is in conduction mode when $V_{in}\ is\ logic$ "1", the output is virtually connected to the ground and the output shifts from high to low.

In the present work, we assume that the Boolean logic inputs corresponding to the voltages like: logic "0" =0 Volts and logic "1"= $0.1\times\frac{q_e}{C}$ Volts. We have accepted for simulation purpose, Logic "1"= $0.1\times\frac{1.602\times10^{-19}}{1\times10^{-18}} = 0.1\times1.602\times10^{-2} = 16.02\times10^{-3}$ =16.02 ≅ 16 mV provided C=1aF.

3. Analog Comparator:

An analog comparator or simply called a comparator, contains two input voltage signals V_1 and V_2 and one output voltage signal V_0. One of the input voltage like V_2 is taken as the constant reference voltage θ, sometimes considered as the threshold voltage, and the other one is taken to be time-varying signal (V_a). An comparator having the voltage transfer characteristics is shown in Fig. 3(b), has one constant output voltage W =0 if V_a<θ, and a distinct constant voltage W=1 if $V_a \geq \theta$. Clearly, by using the comparator, the time varying input voltage is compared with the reference voltage and the output is digitized or quantized into one of the two states: a '0' level for voltage low and '1' level for high.

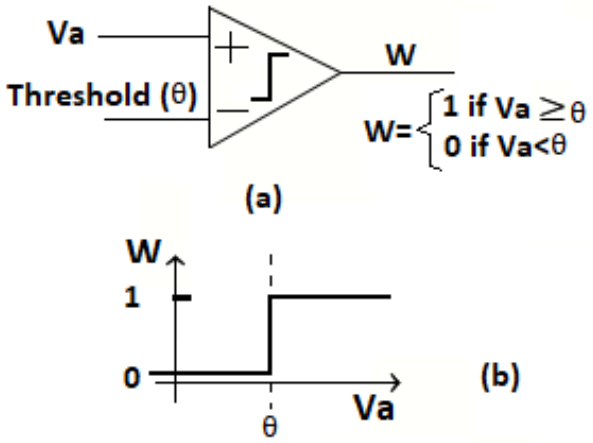

Fig. 3(a) A comparator (b) input-output relation

4. Operation of Parallel comparator Analog to Digital Converter

The operation of the Analog to Digital Converter is easily understood when the reference is made for the 3-bit Analog to Digital Converter as shown in Fig. 4(a). In the figure, there are two inputs (i) reference voltage V_{Ref} and (ii) analog input voltage V_a. As per the combination of a bank of the comparators, when an analog voltage applied at analog input terminal—this is basically applied to the bank of comparators simultaneously. The comparators are being the equally spaced thresholds, here the thresholds (or reference voltages) are $V_{Ref1}=\frac{V}{8}$, $V_{Ref2}=\frac{2V}{8}$, $V_{Ref3}=\frac{3V}{8}$, $V_{Ref4}=\frac{4V}{8}$, $V_{Ref5}=\frac{5V}{8}$, $V_{Ref6}=\frac{6V}{8}$, and $V_{Ref7}=\frac{7V}{8}$. Such type of processing is termed as "bin conversion" [21] as the input analog voltage is sorted in a given voltage range being determined using the thresholds to two adjoining comparators. The comparator outputs W_i ; $i = 1,2,\ldots,7$ undertake distinct pattern: output of the comparators will be low (level 0) when the thresholds are above the input voltage and that of the comparators will be high (level 1) when the thresholds are below or equal to the input voltage. For instance, if $\frac{3V}{8}<v_a \leq \frac{4V}{8}$ we have $W_1 = 1, W_2 = 1, W_3 = 1$ and W_4 =1, and all other W_i , $i = 5,6\ and\ 7$, output values will be 0. Under this condition, the output of this converter ought to be Y_2=1, Y_1=0, Y_0=0, and it is interpreted to give meaning that the input voltage lies in the range between $\frac{3V}{8} < v_a \leq \frac{4V}{8}$. Regarding this discussion, we can present the diagram and graph for clear understanding in Fig. 4(a) and 4(b).

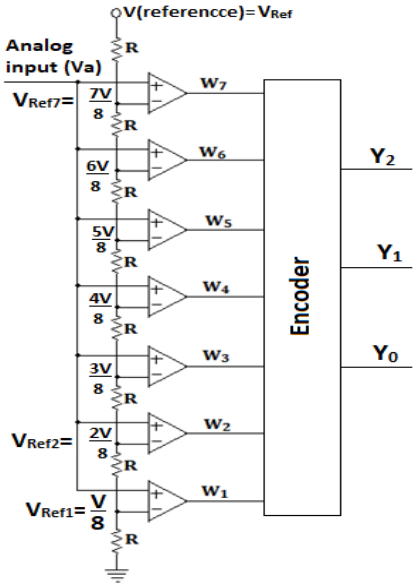

Fig. 4(a) 3-bit (output) Analog to Digital Converter

The operation of the Fig. 4(a) is interpreted with the help of Fig. 4(b), where the Y-axis shows the 3-bit output in quantum fashion and X-axis informs about the analog input V_a. When any input value V_a lies in an interval between two contiguous marking points in X-axis, the output of the encoder of the Analog to Digital Converter (ADC) will be a discrete 3-bit value. For example, if the unknown analog input voltage stays in the interval $\frac{3V}{8} < V_a \leq \frac{4V}{8}$, the ADC gives the result $Y_2Y_1Y_0$= 011, similarly, if the input V_a exists in $\frac{4V}{8} < V_a \leq \frac{5V}{8}$, the output will be $Y_2Y_1Y_0$= 100, and so forth.

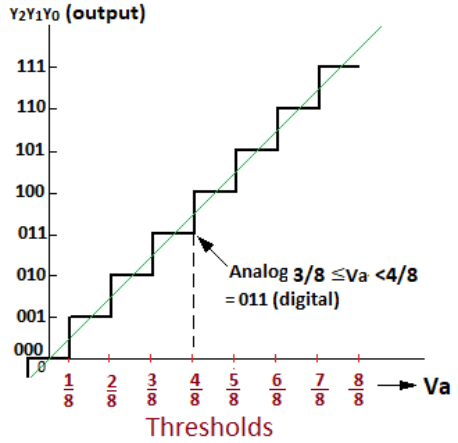

Fig. 4(b) digital output vs. analog input

As the outputs ($Y_2Y_1Y_0$) have the relations with(W_1,W_2, W_3,W_4, W_5, W_6, W_7), and it is shown in the Table-1.

Table-1
Relationships of inputs and outputs of comparators

input	output						
V_a	W_7	W_6	W_5	W_4	W_3	W_2	W_1
$V_a < 0$	0	0	0	0	0	0	0
$0 \leq V_a < \frac{1V}{8}$	0	0	0	0	0	0	**1**
$\frac{1V}{8} \leq V_a < \frac{2V}{8}$	0	0	0	0	0	**1**	1
$\frac{2V}{8} \leq V_a < \frac{3V}{8}$	0	0	0	0	**1**	1	1
$\frac{3V}{8} \leq V_a < \frac{4V}{8}$	0	0	0	**1**	1	1	1
$\frac{4V}{8} \leq V_a < \frac{5V}{8}$	0	0	**1**	1	1	1	1
$\frac{5V}{8} \leq V_a < \frac{6V}{8}$	0	**1**	1	1	1	1	1
$\frac{6V}{8} \leq V_a < \frac{7V}{8}$	**1**	1	1	1	1	1	1

We are going to focus on the digital part of the ADC exclusive of comparators, i.e. on the inputs Wi; i=1,2,…,7 , outputs $Y_2Y_1Y_0$ and the Encoder circuit. The corresponding related data concerning W_i and Y_j of the Encoder are listed in Table-2.

Table-2

inputs							outputs		
W_7	W_6	W_5	W_4	W_3	W_2	W_1	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	**1**	0	0	1
0	0	0	0	0	**1**	1	0	1	0
0	0	0	0	**1**	1	1	0	1	1
0	0	0	**1**	1	1	1	1	0	0
0	0	**1**	1	1	1	1	1	0	1
0	**1**	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

For the purpose of measuring the unknown voltage (Analog signal) given at the input terminal the relationship between $W_i, i = 1,2,\ldots,7$ and Y_j, $j = 0,1,2$ should be as in Table-2, but the implementation of the related circuit would be more complex as the logic expressions for ($Y_2Y_1Y_0$) with respect to(W_1,W_2, W_3,W_4, W_5, W_6, W_7) will be complex. To do more simple and user-friendly circuit, we are to convert the input values of Table-2 into the input values of Table-3. These conversions are done with the assistance of the following relations. Here we are interested in involving the Exclusive-OR gate. In the following relations, the symbol "⊕" indicates the Exclusive-OR operator.

D7=w7⊕ 0, D6=w6⊕ $w7$, D5=w5⊕$w6$, D4=w4⊕$w5$, D3=w3⊕$w4$, D2=w2⊕$w3$ and D1=w1⊕$w2$

Applying these relations, a new set of data is created and is listed them in Table-3.

Table-3

inputs							outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	0	1	0	1
0	1	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	1	1	1

From the Table-3, one can write the logic expressions of $Y_i, i = 0,1 and\ 2$ with respect to D_1, D_2, D_3, D_4, D_5, D_6 and D_7 as below.

$Y_2 = D_4+D_5+D_6+D_7$ ..... (1)

$Y_1 = D_2+D_3+D_6+D_7$ ..... (2)

$Y_0 = D_1+D_3+D_5+D_7$ ..... (3)

Where "+"indicates the OR operator in the equations (1), (2) and (3).

All the three equations are of OR operations. So the above three equations related circuit can be implemented with the 4-input OR gates only.

From the above discussion, we have found it good to implement two types of gates (i) 2-input XOR gates and (ii) 4-input OR gate. So, using the XOR and OR the modified circuit is drawn Fig. 4(c).

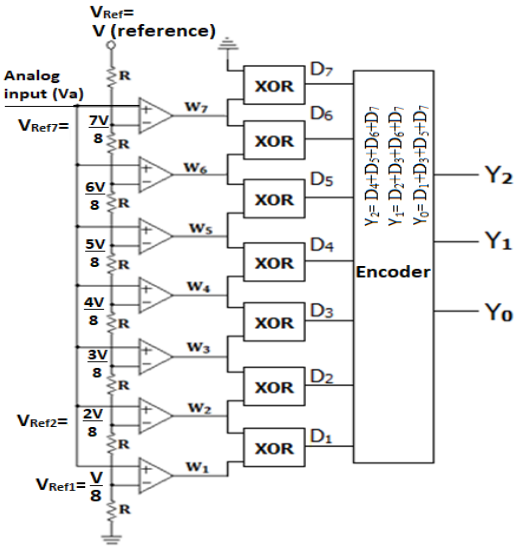

Fig. 4(c) Modified Analog to Digital Converter

As we are interested in making a device performing the Analog to Digital(A/D) conversion operation or simply a voltmeter based on single electron tunneling phenomena, we must concentrate our attention to SET based XOR gate and OR gate and then we have to arrange the connection pattern so as to obtain the desired circuit.

5. The single-electron XOR gate

The single-electron XOR gate is shown in Fig. 5(a)[20]. The circuit consists of four islands N_1, N_1, N_1 and N_4 , and five tunnel junctions $J_1 - J_5$. Tunnel junctions $J_2 - J_5$ are identical. The resistance of each is 10^5 ohm and the capacitance is 1aF. It is less transparent for the junction J_1 to prevent an electron transport from the ground (V_{SS}) to the first island N_1 and vice versa. Its resistance and capacitance are 10MΩ and 1aF, respectively. The voltage V_{dd} is constant and its value is 100mV.

V_1 and V_2 are the two input voltages of XOR gate. V_1 and V_2 can take only two values, 0.0 V, which corresponds to the logic "1", and -100mV, which corresponds to the logic "0". The input voltages are applied to nodes N2 and N3, respectively, through the capacitors $C2$ and $C1$ which are identical, and their capacitance is 10^{-18} F. The gate output is at the island N_1. When a positive charge presents on N1, it corresponds the logic "1", whereas if a negative charge is present on N1 , the output corresponds to the logic "0".

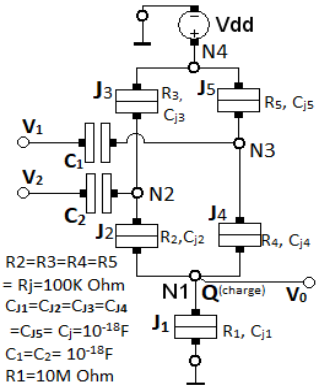

Fig. 5(a) SET based XOR gate

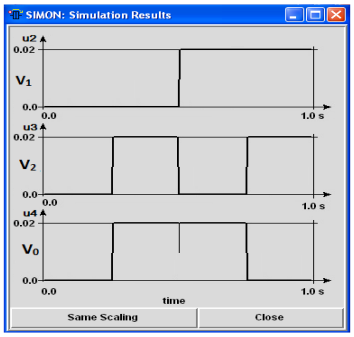

Fig 5(b) Simulated result of XOR

6. Single Electron Transistor based 4-input NOR gate

We think it appropriate to make a 4-input OR gate by using 2×4 single electron transistors as shown in Fig. 6(a). These SETs are arranged in horizontal and orthogonal pattern. The orthogonal 4 p-channel SETs are linked in series and horizontal 4 SETs which are n-channel SETs are connected in parallel. The SET based circuits can be configured as CMOS circuits, the pull down transistor (lower four transistors connected in parallel) defined as n-channel transistors (N-SET) tied to the ground and the pull up transistor (upper four series connected transistors) called p-channel (P-SET) is tied to V_{dd}.

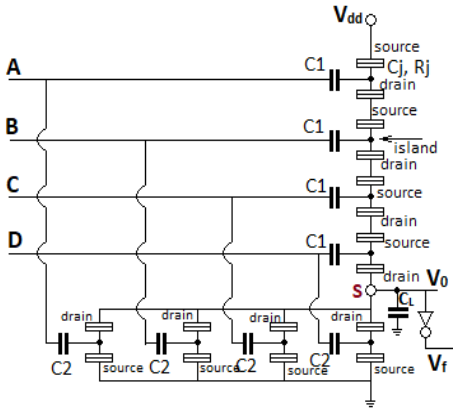

Fig.6 (a) 4-input NOR/OR Gate

The circuit constructed in Fig. 6(a) is called a 4-input OR gate, the operation of which is as:-when all the inputs values of A, B, C and D are set as low, there will be created p-channel for each of the upper SETs. As a result, the electron(s) available at point S easily tunnel/s towards V_{dd} and the point S is thought to be connected to V_{dd} as a consequence the output value becomes high(1).

Table-4

A	B	C	D	V_0	V_f
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	1

On the other hand, as the horizontally connected n-channel transistors are in cut-off mode when the all input signals are in low. So, no tunnelling phemomena will happen through the lower n-channel SETs. Now if we set any one or any two or any three or all 4 SET(s) as logic "1", then the lower parallel connected SETs get n-channel and the point S is considered to be connected to ground and it results $V_0 = 0$. The input-output relationships are given in Table-4.

A small modification of Fig. 6(a) is done with a capacitor having capacitance 0.5aF conneced to the node for each of the transistors and a voltage source is also connected in series with the capacitor (for upper four) in Fig. 6(b) for the purpose of balancing/tuning the electron tunneling [3-8,17]. In Fig. 6(c) the simulated result of Fig. 6(b) is depicted.

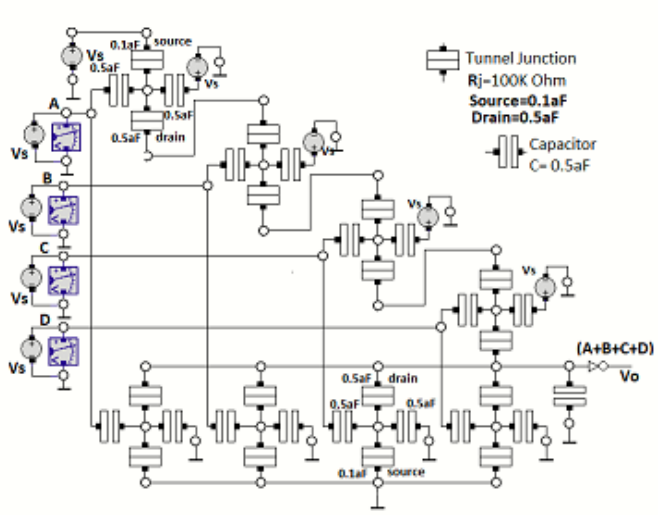

Fig. 6(b) SET based 4-input OR gate V_0 = (A+B+C+D)

For the simulation purpose, the parameters used for the 4-input NOR gate are: Drain capacitance=0.5aF, Source capacitance=0.1aF, and for inverter: $C_1 = C_2 = 0.5aF$, $C_{g1} = C_{g2} = \frac{17}{4}C = 4.25aF$, $C_L = 9aF$, R1 = R2 =100KΩ, high logic voltage=16mV and low logic= 0 Voltage.

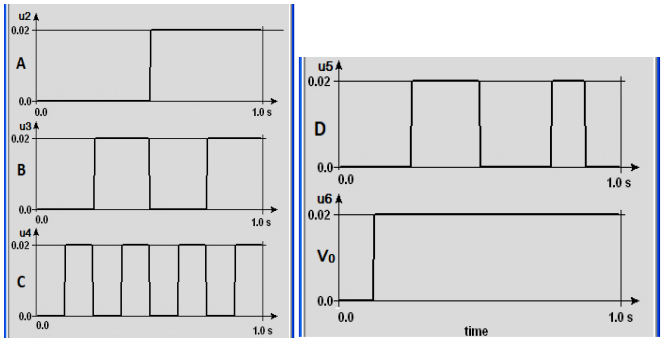

Fig. 6(c) Simulated result of 4-input OR gate

7. Operation of the voltmeter based circuit:

A simple digital voltmeter circuit drawn in Fig. 7(a) [placed in the last page due to its big size] consists of (i) 8 registers, each having values R=1MΩ, (ii) 7 comparators, (iii) 7 Exclusive-OR gates and three 4-input OR gates and an indicator showing the outputs. The reference voltage is on the top of the 8 resistors connected in series, so it is a voltage divider circuit. The analog voltage V_a is applied directly and simultaneously to the bank of comparators with equally spaced thresholds where the reference voltages for the –ve terminals of the comparators comp1, comp2, etc. would be $V_{R1}=\frac{V}{8}$, $V_{R2}=\frac{2V}{8}$, and so on.

Note that a switch circuit is placed in between the comparator output and XOR input. The switching circuit converts logic "1" to 0.0 Volt and logic "0" to -100mV. As the XOR used here can take only two values for inputs: 0.0 V, which corresponds to the logic "1", and -100mV, which corresponds to the logic "0".

It can draw our attention that the comparator output $W_{i,\ i=1,2,\ldots,7}$ take on very distinct pattern as: when the thresholds for all the comparators are above the input voltages, the outputs for them are low ("0"), and for each comparator when its threshold is equal to or less than the analog input then the output is high ("1"). For instance, if v_a lies between $V_{R2}=\frac{2V}{8}$ and $V_{R3}=\frac{3V}{8}$ i.e., $\frac{2V}{8} \leq v_a < \frac{3V}{8}$, then $W_1 = W_2 = 1$ and the remaining all $W_{i,\ i=3,4,\ldots,7}$ become 0. In this circumstances, the digital output of the voltmeter should be Y_2= 0, Y_1= 1 and Y_0= 0 whose decimal value is 2 which is the indication that the input voltage resides in between $\frac{2V}{8}$ and $\frac{3V}{8}$ *exclusive of* $\frac{3V}{8}$.

The input-output relationship between $W_{i,\ i=3,4,\ldots,7}$ and $Y_{j,\ j=0,1,2}$ is provided in Table-1. According to Table-1, the logic expressions of the relationship between $W_{i,\ i=3,4,\ldots,7}$ and $Y_{j,\ j=0,1,2}$ will be more complex. For avoiding the complexity if XOR gates are used in the order like D7=w7⊕ 0, D6=w6⊕ $w7$, D5=w5⊕$w6$, D4=w4⊕$w5$, D3=w3⊕$w4$, D2=w2⊕$w3$ and D1=w1⊕$w2$, we get the output expressions given in equations (1), (2) and (3) and the relationships between all D and all Y are listed in Table-3. With the assistance of these equations we can draw an encoder (in Fig. 7(a)) which provides us the desired outputs through the terminals Y_2, Y_1 and Y_0.

Table-5

Input analog voltage (v_a)	output		
	Y_2	Y_1	Y_0
v_a<1	0	0	0
1≤ v_a<2	0	0	1
2≤ v_a<3	0	1	0
3≤ v_a<4	0	1	1
4≤ v_a<5	1	0	0
5≤ v_a<6	1	0	1
6≤ v_a<7	1	1	0
7≤ v_a	1	1	1

By using the simulator SIMON on the simulation circuit shown in Fig. 7(a), we would be able to draw digital/simulated results, some of which have been given in Fig. 7(b). We have taken the reference voltage 8mV, for our convenience. A theoretical figure of input-output relation is depicted in Table-5.

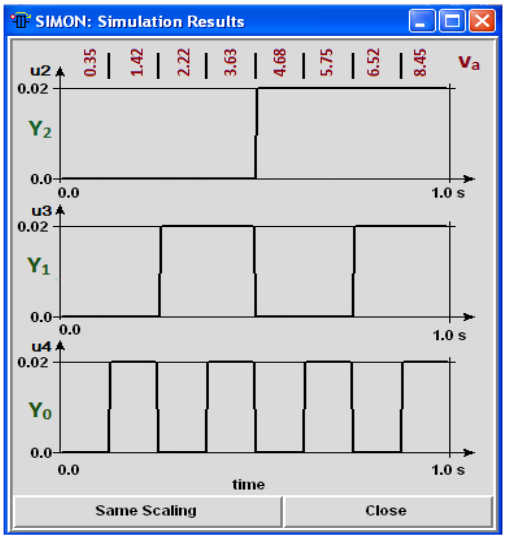

Fig. 7(b) Simulated result of Fig. 7(a)

From the simulated result, we have analog input 0.35← equivalent to 000, input 1.42← equivalent to 001, input 2.22 ← equivalent to 010, input 3.63 ← equivalent to 011, 4.68← equivalent to 100, 5.75← equivalent to 101, 6.52← equivalent to 110, and 8.45← equivalent to 111 and these relations are listed in Table-6. When comparing the simulated result with the theoretical result, we feel that they coincide. Hence the circuit we designed is correct.

Table-6

Input(v_a) analog voltage mV	output			Output Decimal value	Result in the range
	Y_2	Y_1	Y_0		
0.35	0	0	0	0	0-1
1.42	0	0	1	1	1-2
2.22	0	1	0	2	2-3
3.63	0	1	1	3	3-4
4.68	1	0	0	4	4-5
5.75	1	0	1	5	5-6
6.52	1	1	0	6	6-7
8.45	1	1	1	7	7 or more

The data being shown in the Table-6 tell us that when an unknown voltage is measured with the help of the circuit depicted in Fig. 7(a), we can decide that the result lies within a small range but not the exact value. If the number of registers (R) in the voltage divider part and the number of comparator are increased, the output voltage also be more accurate. So the Precision is increased. For the space limit, we are confined to the voltage divided circuit having only 8 resistors (R). The parameters used in the circuit shown Fig. 7(a) are given in tabular form in Table-7

Table-7

For gate	Parameters values
XOR	R_1=10MΩ, R_2=R_3=R_4=R_5=100KΩ, C_{j1}=C_{j2}=C_{j3}=C_{j4}=C_{j5}=1aF
4-input OR	Drain capacitance=0.5aF, Source capacitance=0.1aF, and for inverter: $C_1 = C_2 = 0.5aF$, $C_{g1} = C_{g2} = \frac{17}{4}C = 4.25aF$, $C_L = 9aF$, R1 = R2 =100KΩ, high logic voltage=16mV and low logic= 0 Voltage.

8. Speed/ Fastness, Delay and switching energy

When a complex circuit including combinational or sequential is constructed, we should keep in mind that some inevitable components which are combined together in a proper way to obtain the desired circuit. In this present work, we are concentrated in Parallel Comparator based voltmeter using single electron tunneling transistor, wherein we need some

inevitable components like 2-input XOR, 4-input OR and comparator. For the purpose of measuring of the efficiency of an electronic circuit whatever it may be either conventional or Nano- or Pico-, some factors are to be considered properly like- (i) number of components, (ii) speed or fastness (ii) time required for an execution, (iv) power consumption, (v) costs of materials, (vi) fan-outs, (vii) controlling charge, (viii) population density of components (ix) atmospheric temperature etc.

We are aware of CMOS/TTL based logic gate that the processing delay/ time delay for a gate like AND, NAND, NOR, XOR is 12ns [21-23], on the other hand the time required for tunneling through a SET is approximately 4ns [20-21]. For any XOR gate used only conventional logic circuits should have 16 transistors, whereas the same function can be implemented with just 2 SETs plus one extra junction [20] i.e. no. of nodes are reduced to 2 instead of 16. For finding out the processing/switching delays for a multi-input threshold logic circuit based on electron tunneling, we are to think of the critical voltage V_c and the tunnel junction capacitance Cj of multi-input threshold logic circuit. The processing delay for this circuit is to find out by using the logarithmic expression of probable error provided by the approach as given below [3-8, 17].

$$\text{Delay} = -(e|\ln(P_{error})|R_t) / (|V_j| - V_c) \cdots\cdots (3)$$

where, R_t = the internal resistance of the tunnel junction, V_c = the critical voltage and V_j is being the tunnel junction voltage.

Execution is done when an electron passes through the tunnel junction barrier. When the tunnel junction voltage V_j being a fraction of the bias voltage is greater than or equal to the internal critical voltage V_c of the tunnel junction i.e., when $|V_j| \geq V_c$, then a tunneling event occurs.

If this conditional expression $|V_j| \geq V_c$ is satisfied by a 2-input AND gate, junction voltage of the 2-input AND gate becomes V_j =10.80, the internal critical voltage V_c of the tunnel junction is found to be 11.58mV [3-5]. Given that the parameter values of tunnel resistance $R_t = 10^5\Omega$ and the probability of error $P_{error} = 10^{-12}$. Putting them in equation (3) we can calculate the gate delay = $0.062|\ln(\boldsymbol{P_{error}})|$ = 1.71ns. In a similar manner we can calculate the delays of distinct circuits and they are listed in Table-8 and 9.

While tunneling, an electron passes over the junction barrier, by changing the total energy present in the circuit. The energy changes before and after a tunneling event is measured by the equation (4) given below.

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel}$$
$$= -e(V_c - |V_j|) \cdots\cdots (4)$$

This is considered as the switching/tunneling energy $-e(V_c - |V_j|)$ that is consumed for a tunnel event in the tunneling circuit. We listed the energy consumptions for distinct and separate linear TLG circuits in Table-9 [23].

Table-8

Gate/ Device	SET-based delay (ns)	LTG-based delay (ns)	Speed-up (times)
2-input NOR	4	1.65	2.42
2-input OR	4	1.71	2.33
2-input NAND	4	1.71	2.33
2-input AND	4	1.71	2.33
inverter	8	0.60	13.33
3-input AND	8	1.98	4.04
3-input NAND	8	1.98	4.04
2-input XOR	4	2.21	1.81
3-input OR	8	2.01	3.98
3-input NOR	8	1.99	4.02
4-input OR	8	2.15	3.72
voltmeter	12	4.36	2.75

Table-9

Gate / Device	SET		TLG	
	Number of Elements required	Switching Energy $\times e^{-18}$ (Joule)	Number of Elements required	Switching Energy $\times e^{-18}$ (Joule)
2-in AND	24	3.30106	6	1.7301
2-in NOR	16	2.20781	6	1.7141
2-in OR	24	3.30106	6	1.7301
2-in NAND	16	2.20781	6	1.7301
inverter	8	1.10339	9	1.6661
3-in AND	32	4.41356	7	1.8551
3-in NAND	24	3.30106	7	1.8551
2-in XOR	9	1.24131	13	3.3962
3-in OR	32	4.41356	7	1.8551
3-in NOR	24	3.30106	7	1.8551
4-in OR	40	5.51695	8	2.2780
voltmeter	147	20.2748	90	21.9474

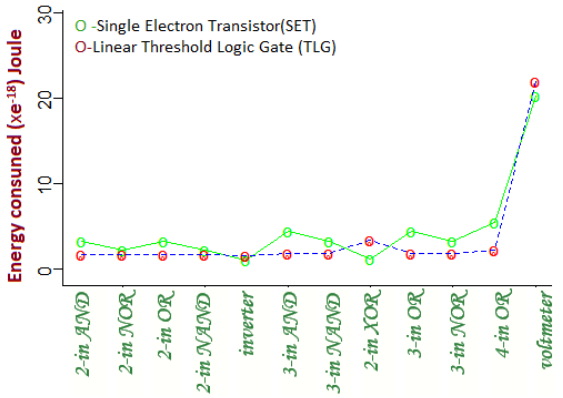

Fig. 8 Energy consumed vs. Gates of (SET+TLG)

Another comparisons related to CMOS, SET and TLG are given in Table-10.

Table-10

Name of parameter	CMOS circuit	SET circuit	TLG circuit
Switching Speed	$\frac{1}{10^{-9}s}$	$\frac{1}{10^{-10}s}$	$\frac{1}{10^{-12}s}$
Operating Temp	>300 Kelvin	Close to 1 Kelvin	Close to 0 Kelvin
Current range	nA	1.60217 $e^{-19}C/$ *tunneling*	1.60217 $e^{-19}C/$ *tunneling*
Voltage range	100mV	16mV	16-20mV

The number of prime elements like capacitors, resistors are needed for constructing a small elements like logic gate or circuit are counted. We have kept track of the parameter values essential from this work in relation to small element numbers, delays or late, and switching power. All of them are tabulated in Table-8 and Table-9. Power consumption ($\times e^{-18}$Joules) for each circuit vs. element numbers (n) is shown in Fig. 9 below. The processing delays for single electron Transistor (SET) and TLG based circuits in reference to the various elements are depicted by using the bar diagram side by side in Fig. 10.

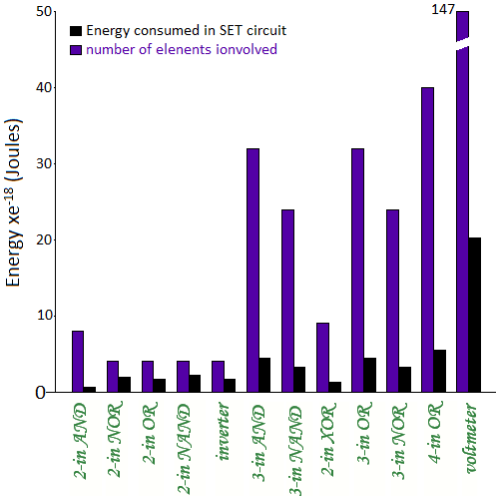

Fig. 9 switching energy vs. of no. of small Elements

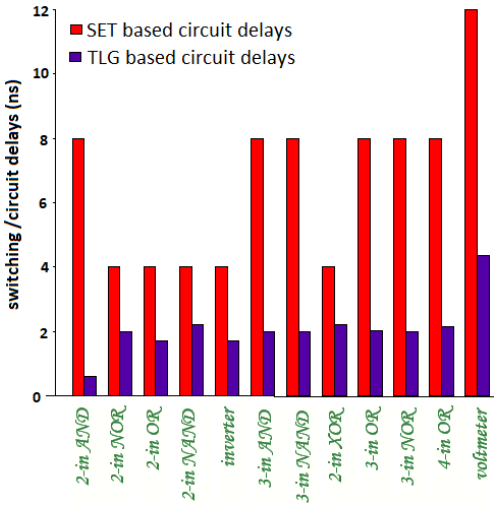

Fig. 10 Switching delays of SET/TLG vs. circuits

We are intended in bringing to light the circuit delays in connection with CMOS, SET-based and TLG-based. We have detected the processing delays as 12ns [5-11, 17-18] each for the case of a CMOS logic gate like AND, NAND, NOR and XOR. The tunneling time delay in the case of a single electron transistor (SET) [13-15] is approximately 4ns [4-10, 17-18]. The speed-up of linear TLG-based delays in connection to the corresponding delays of SET-based delays are listed in Table-8, and the two curves of (i) SET-based and (ii) TLG-based power consumption versus the different logic gates / circuits are depicted in Fig.8.

9. Switching delays for implemented voltmeter

A comparator's processing delay time is approximately 2.9ns (like LTC6752), the delay time of an XOR gate is 2.21ns and that of a 4-input OR gate is 2.15ns. As these three components are connected in series, the total delay time of the parallel comparator based voltmeter will be the sum of the cited delay times, i.e, 2.9+2.21+2.15=7.26ns. So, the first fan-out time is 7.26ns. Hence the fan out rate or output processing frequency $f_{out} = \frac{1}{7.26ns}$=137.442MHz.

III. CONCLUSION

Whether a potential or voltage source having a standard value or not is one of many factors to drive an electrical or electronic circuit/device. For volatile component involved in a process (means in processing) requires ceaseless voltage source. So the measurement of voltage level of a voltage source is essential. In this work, a voltmeter called "Parallel Comparator based voltmeter using single electron tunneling Transistor" is designed and implemented in order to measure a voltage range between 0 to 7^+ mV. In this voltmeter, energy consumed 20.2748×10^{-18} Jules per fan-out which is very small amount. The output fan-out rate is 137.442MHz. How much energy required for small components is shown by a graph. Total number of components and their processing delays and their power consumption are listed in distinct tables. The voltmeter implemented here does not indicate the exact result. But it gives an indication that the input voltage resides in a small range of voltage. We have compared the output of the designed voltmeter with the theoretical values and the result seems to us that they are matching with the theoretical values. Almost all of the circuits provided are verified by the simulator-SIMON and realized that the simulated results are squared with the theoretical aspects. Note that the temperature should be maintained at very close to 1Kelvin and it is a tough job. Scientists are trying to make a SET based circuit operating at very close to 0^oC.

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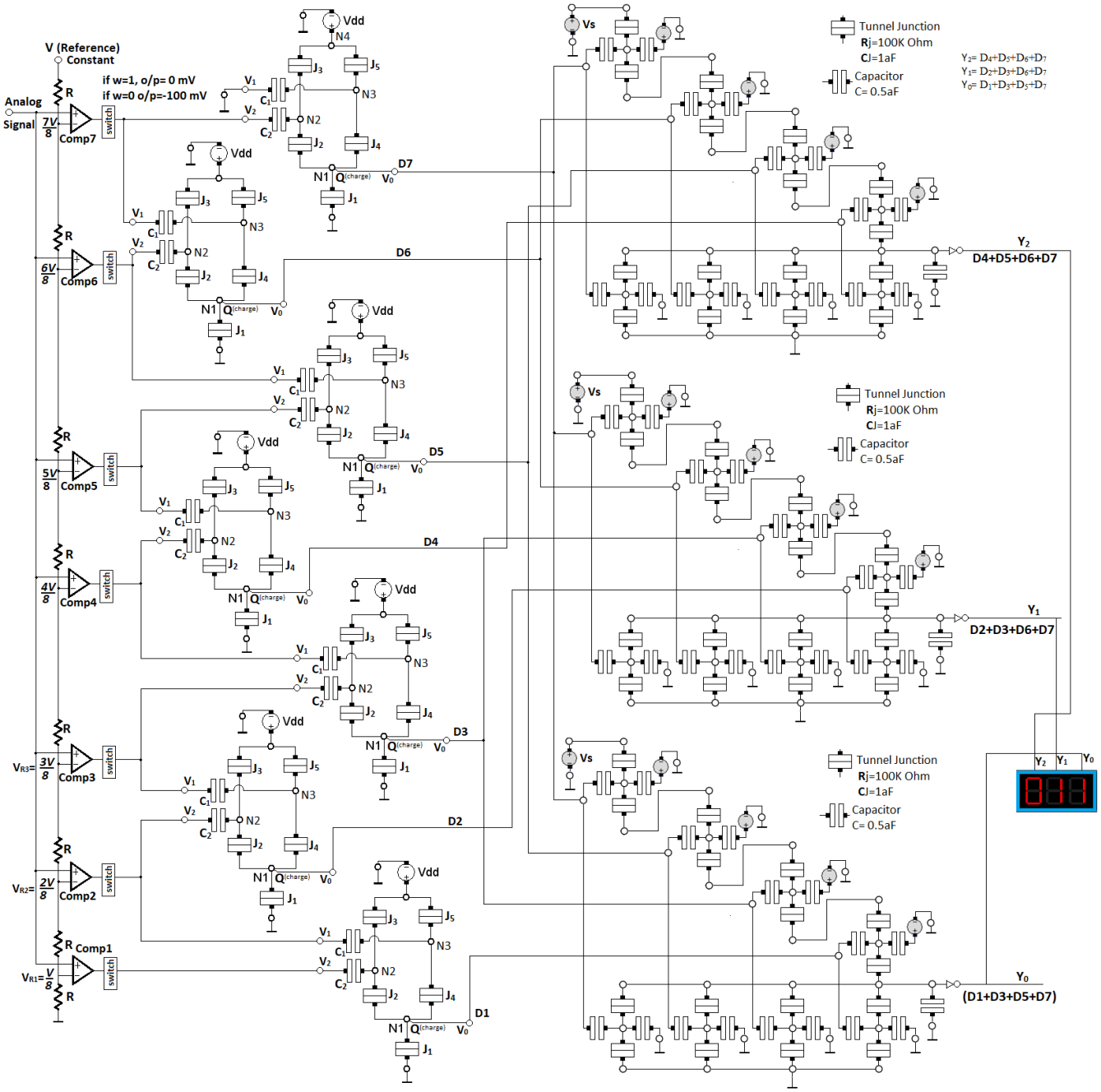

Fig. 7(a) Parallel Comparator based voltmeter using SET