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Recent and Old Developments in Tunnel Field Effect Transistor

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ABSTRACT

In this paper, from old developments to new/advanced developments in Tunnel Field Effect Transistor (TFET) is reviewed. The history, device Physics and performance boosting methodology has been investigated. The vertical and planer tunnel FET are contrasted. Further, Tunnel FET is benchmarked with CMOS technology. The on-current, transconductance and power conversion performance are extracted from reported works and a new perception on the extracted data is presented. The TFET is also presented as beyond FinFET. Based on the review made in this paper, impact of drain doping on capacitance is identified as left-out analysis. Thus, role of drain doping on capacitance is demonstrated using TCAD simulation.

Keywords—TFET, MOSFET, Tunneling, Silicon, Capacitance

I. INTRODUCTION

Silicon based CMOS technology shouldered the burden of semiconductor industry. TFET emerged as alternative device to CMOS based MOSFET.However, there are lot of limitations in practical implementation.Further, TFET might be also taken as hypothetical device. In this paper, a review of Tunnel FET is carried out.

II. HISTORY OF TUNNELING DEVICE

Tunnelling mechanism has a long history and implemented in semiconductor device, which is dated back to 1950s. Device with tunnelling progress opened a regime of semiconductor device. Advancements in the studies of tunnelling phenomena leads to the fabrication of tunnel diode. Negative resistance is the novel property in the tunnel diode. Further, the energy barrier does not vary monotonically with applied electric field. One can see the tunnel device is the next generation semiconductor device, on the perspective of "Beyond-CMOS". MOSFET works on the transport of carrier over a barrier while in tunnel FET (TFET) carrier tunnels. In tunnel FET, the carrier tunnels from source side valance band to channel side conduction band. The TFET can break the 60 mV/dec sub-threshold swing of MOSFET. The principle in MOSFET stems from thermionic transport over channel to source region. The tunnel FET is commonly characterized using band-gap barrier. The

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experimental and theoretical feasibility of this TFET is also possible. Experimental feasibility is also possible for silicon-on-insulator (SOI), strained semiconductor, graphene nanoribbons, double gate device, carbon nanotubes and III-V materials.

III. THE PHYSICS OF TFETS

In MOSFET, the carriers are injected thermionically over the energy barrier. In TEFT, inter-band tunnelling is the carrier transport mechanism, which is due to heavily doped P-N junction. Zener in 1934 identified this tunnelling mechanism. The TFET can be abruptly turned on and turned off by bending the band by means of gate voltage. This on-off function could be realized p-i-n stack, where, i is intrinsic layer. In principle, the Tunnel FET has n-type and p-type behaviour with dominant electron and hole conduction, respectively. Thus, by nature, the TFET is a bidirectional or ambipolar semiconductor device.

However, heterostructure can be used to restrict one-type of carrier movement or design of asymmetric doping profile can be used to widen the energy barrier at drain side. Therefore, ambipolar current is supressed. Apart from this, asymmetric doping concentration also has the capability of achieving lower off-state current [1].

IV. BASIS OF PERFORMANCE BOOSTING

The simultaneous achievement of highest on-current and lowest subthreshold voltage slope is the design goal of tunnel FET[1]. With this, the lowest possible off-current should be achieved. To outperform complementary metal oxide semiconductor device, the parameters targeted in tunnel FET are: drain voltage lower than 0.5 V, on-off ratio >105; on-current in the order of 100s of mill-amperes; sub-threshold swing (SS) distant below 60 mV/decade. As SS diminutives with gate bias, TFET are naturally targeted low and ultra-low power operation.

To achieve a steep slope and high on-current, tunnelling probability has to approach the unit for a tiny change in gate voltage. The tunnelling probability (Tprob) proportional to mass, which can be extracted from following expression

$$T_{prob} = exp\left(-\frac{4\gamma\sqrt{2m}\sqrt{E_g}^3}{3qh(E_g+\Delta\theta)}\right) \quad (1)$$

where, E_g andm are energy and mass, respectively.

V. DEVELOPMENTS OF TFET IN 2018 AND 2019

A. Low power applications

Vertical-Structured Electron-Hole Bilayer Tunnel Field-Effect Transistor (V-EHBTFET) decreases the device ON voltage with the help of workfunction engineering and using narrow bandgap materials at the virtual junction region. As a result of this the V-EHBTFET can be used for Low power applications.

Gate engineered InGaN DL-TFET (Dopingless) has improved drain current and reduced subthreshold swing which results the device will work properly for low power applications.

B. ESD protection devices

The electrostatic discharge due to double current flow in the device, which was suppressed as reducing the charge flow at source channel interface by the grounded gate TFET structure.

C. Digital Logic Circuits

The twofold TFET (TF-TFET) is a mixture of n-type and p-type TFETs. Since it has both n-type and p-type, the TF-TFET was used as an inverter. A single device will act as inverter as a result the number of transistors that was used in the logic circuits were reduced also the miller capacitance be reduced.

D. Biosensors

Circular gate TFET and heterojunction TFET are used as biosensors, by dielectric modulation, compared to MOSFET both the CG and HJ TFETs perform far more better in the biomolecules sensing.

E. Memory Design

The development of SRAM cell using TFET particularly Dual pocket double gate TFET shows improved current ratio and subthreshold swing. Due to this factors the memory cell was designed for low power applications and improved write margin.

F. Logic Circuit Implementation

Double Gate TFET (DG-TFET) with independently controlled gate is used in the realization of compact logic gates. This type of logic function implementation exhibits compactness, improved propagation delay and low power dissipation.

G. Low-Cost Radio Frequency and Low Power Application

In0.53Ga0.47As/In0.52Al0.48As Heterojunction Dopingless TFET (HDL-TFET) exhibits low subthreshold swing and effectively suppressed the ambipolar characteristics due to heterogate HfO2 /SiO2. As the result HDL-TFET exhibits cutoff frequency in the order of GHz with low power consumption.

VI. NEW DEVELOPMENTS IN TFET

A. Line-Tunneling and Buried N+ Drain FETs

Line tunnelling method can be to obtain simultaneous improvement of on-current and reduction of subthreshold slope[2].However, in this method, isolation drain and source is a challenging one. In normal tunnelling, the channel is next to source in lateral direction (source-to-drain direction). In the case of line tunnelling, the channel is placed over source in vertical direction (channel-to-gate direction). The leakage current degrades the off-state characteristics severely. Air-bridge or cantilever are the common method of cutting the leakage path. However, it brings additional process complexity and induces reliability issues. Buried +N doping also used to cut-off the leakage path. This N+ doping act as reversed P-N junction. The merit of N+

buried drain keep the device planner, so, this technique could be taken for future experimental investigation. In line tunnelling, carrier sees a longer path than that of direct tunnelling.

B. DRAM

In order to retain the data statistically, DRAM uses Negative Differential Resistance (NDR) and storage capacitor leakage. Retention of data statistically eliminates data refreshment. Design of TFET based DRAMachieves higher throughput, which is owing to removal of data refreshment[3].

C. SRAM

Forward p-i-n current in TFET is avoided to reduce leakage power conception. In contrast to 6 transistor (6T) based SRAM design, 10 tunnel FTET transistor (10T) is used to improve noise margin and reduce power conception[4].

D. TFET with Ternary CMOS

TFET with ternary CMOS method to obtain half supply voltage (drain voltage) operation. Two kind of tunnelling is used in T-CMOS such as: (1) source-drain tunnelling and (2) source-channel tunnelling[5].

E. Implanted Drain and Face-Tunneling

N-type ion can be implanted in drain side and this implantation is compatible with standard CMOS fabrication process flow. The drain ion implantation is an effective method to reduce the leakage. Along with ion implantation, face tunnelling can be used to achieve higher tunnelling current[6].

F. Anisotropic Insulator

Managing electrostatic field in MOSFET and TFET is important as it has great influence sub-threshold swing. Further, anisotropic insulator can outperform the HfO_2. The use of anisotropic insulator in TFET manipulates the electrostatic field. The anisotropic insulator can be implementedusing gate-insulator and spacer layer.In this implementation, permittivity modulates the fringing field between the contact metals. Permittivity also modulates the subthreshold voltage swing[7].

G. Transient Response for Sensing application

For sensing neutral and charged biomolecule, transient analysis a promising method as it provides good selectivity. In transient simulation, the variation is more sensitive to the variation of permittivity. Assorted permittivity could be used to mimic the presence of the variety of biomolecule in the sensing region[8].

H. 12 Transitor SRAM

The leakage current can be reduced in different level such as device level and circuit level. In circuit level reduction, 12 transistors effectively reduce the reverse current in SRAM. Adopting write-assist-circuit in 12T SRAM cell enable it perform well compared to 7T SRAM [9].

VII. BEYOND FINFET

For the past two decades, in the development of semiconductor products, Finfet technology started its footprint by replacing planar devices. Evolution is a slow process, as it doesn't allow any sudden changes, so, the Finfet technology uses some advancement from the earlier like the use of the high-k metal gate, varied source/drain structures. The worldwide accepted aspect that Finfet is replaced by TFETs. But this replacement cannot be explained clearly when the scaling of the device below 7nm. To overcome this and also incorporate the pros of Finfet into TFETs will be done by varying the structure of TFET resembles Finfet as FIN enabled area scaled TFET as proposed recently shown in FIG

The operation of the device is similar to TFET, as it has great control over the gate channel interface. Due to this the device performance is improved, shown in FIG from the simulation results, the performance of the device improved very well with 10nm gate length, from the following parameters as HIGH ON current, improved transconductance, output resistance, unity gain frequency. Also, the simulation results show reduced OFF current and Area of the chip. Ultimately the Subthreshold Swing has reduced very much in the order of 11mV/dec and the average SS is about 40mV/dec. Since the device exhibits tremendous improvement it is compatible with various analog, digital and RF applications.

VIII. BEYOND CONVENTIONAL SEMICONDUCTORS

In electronics applications, the role of 2D materials like Graphene, Nitrides and dichalcogenides are increased in recent times. Due to this inclusion of 2D materials, the developed electronics products are used in low power areas. The reason for these low power applications is channel properties, thin channel at the atomic level which leads to improved gate control and scalability. The flexibility of 2D materials and the uniform surface helps in the improvement of device reliability.

TMDC based TFET exposes increased gate control over tunnelling junction, absence of TAT leakage and broken band gap TFET architecture. Since the emerging technology has so many advancements it has to grow more to fulfil the needs of the semiconductor industry.

IX. ON-CURRENT

Gate work function, source doping, pocket and oxide material control the On-current (ION) [10, 11]. Ids increases in direct band-gap feature, smaller electron and hole effective mass in InGaN. Tunnelling gate (TG) act as virtual pocket and this leads to have higher field and smaller tunnelling distance. So TG enhances ion. ION improves with increasing “In” fraction in InGaN[10]. As gate/channel length reduces, current will increase, which is shown in Fig. 1. The on-current with respect to channel /gate length is expressed as

$$I_{ON} = -15L_G + C \qquad (2)$$

where ION and C are the On-current and level shifting parameter. The value of C is 600 μA/μm. The -15 in eq. (2) is the negative slope in drain current and it indicates that the On-current is inversely proportional to the gate length.

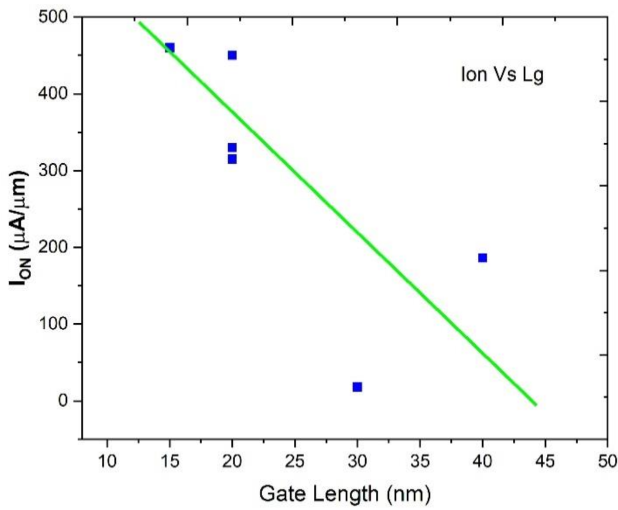

Fig. 1 On-Current versus gate or channel length.

X. DC-DC AND RF-DC POWER CONVERSION EFFICIENCY

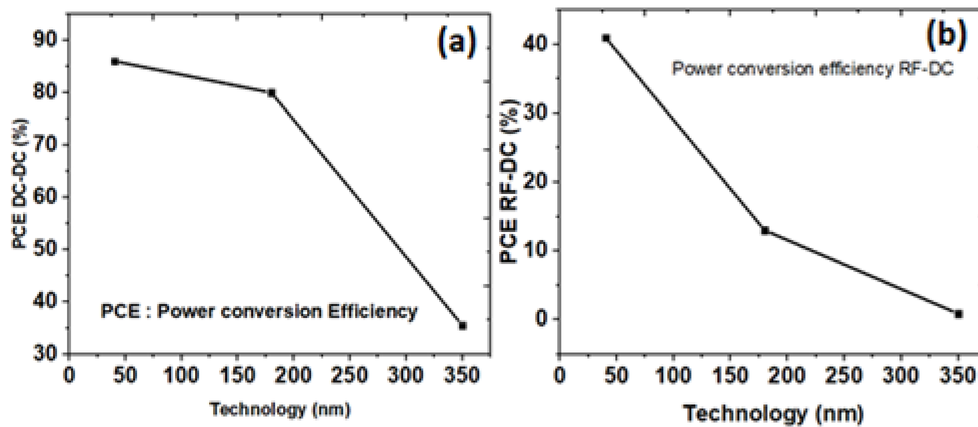

Fig. 2 (a) DC-DC and (b) RF-DC Power Conversion efficiency versus technology (nm).

The power conversion efficiency is very much important in front end RF receiver. In USA and Canada, the transmitted power is 4W at 915 MHz. The distance between transmitter and receiver is 30 m. Thus, the power at receiver antenna is 36 mW. This small received power demands for efficient power conversion device. The DC-to-DC and RF-to-DC power conversion efficiency versus technology node is shown in Fig. 2. As it can be seen, both DC-DC and RF-DC conversion efficiency diminishes with increase in technology node. It could be stated that lower technology node device is preferable for RF front end rectification.

Table I Transconductance and drain current.

VGS (V)	VDS (V)	ID (A/ μm)	Gm (S/ μm)	DEVICE STRUCTURE	REFERENCE SOURCE
-1V	-1V	4x10-8 A	4x10-8 S	P-CHANNEL CG-TFET	[12]
1.5V	0.7V	3x10-12 A/μm	3.18x10-5 S/ μm	SOI-TFET	[13]

1.5V	0.7V	--	4.28x10-5 S/ µm	SELBOX	[13]
1.5V	1V	4x10-10A/ µm	2.01x10-9 S/ µm	SOI-TFET	[14]
1.4V	0.5V	4x10-8A/ µm	1.6x10-7 S/ µm	C-TFET	[15]
1.4V	0.5V	4x10-6A/ µm	7.1x10-6 S/ µm	V-DMGTFET	[15]
1.5V	1V		4x10-8 S/ µm	CG-TFET	[15]
1.5V	1V		2.25x10-7 S/ µm	DCG-TFET	[16]
1.5V	1V	2x10-5 A/ µm	820x10-6 S	DOPINGLESS TFET	[17]
1.5V	1V	2x10-6 A/ µm	0 S/ µm	CONVENTIONAL TFET	[18]
1.5V	1V	6x10-6 A/ µm	0 S/ µm	L-TFET WITH HGD	[18]
1.5V	1V	1x10-3 A/ µm	2.15 S/ µm	L-TFET WITH Ge SOURCE AND HGD	[18]
1.5V	1V	1x10-4 A/ µm	2.15 S/ µm	L-TFET WITH Ge SOURCE	[18]

The drain current and transconductance of various tunnel FET is given in table I. It is observed that dopingless TFET, L-TFET WITH Ge SOURCE AND HGD, and L-TFET WITH Ge SOURCE demonstrate the higher transconductance.

XI. SIMULATION ANALYSIS OF DRAIN SIDE DOPING

The impact of drain side doping on capacitance not analysed yet. Thus, in this paper, doping impact on capacitance is analysed. The device considered for the analysis is shown in Fig. 3, which is reported by C. SheejaHerobin Rani et. Al [19]. The analysis is carried out using TCAD physical simulator. Various physics based model is used in the simulation.

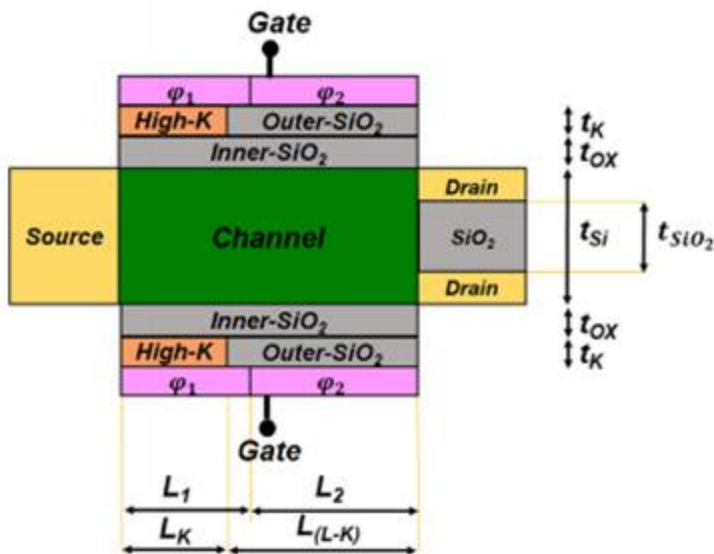

Fig. 3 Schematic of Tunnel Field Effect transistor with reduced High-K material.

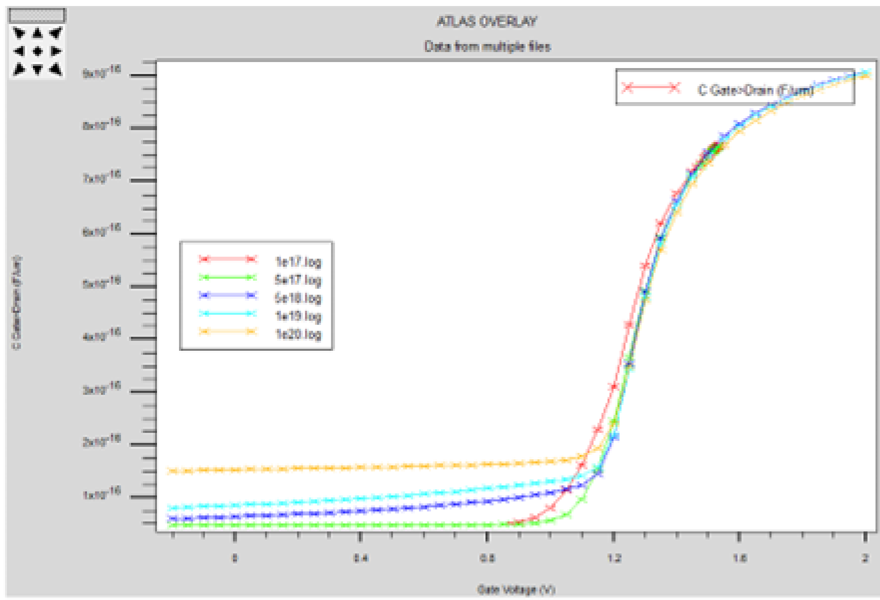

Fig. 4 Gate-source capacitance for various drain side doping ranging from 1e17 cm-3 to 1e20 cm-3.

Fig. 4 shows the gate-to-drain capacitance for various drain side doping. The doping in drain side is varied from 1e17 cm-3 to 1e20 cm-3. The gate voltage is swept from -2V to 2V at drain voltage of 5V. It is interesting to note that the drain side doping affects the gate-source capacitance only around subthreshold voltage and off-state region. In off-state region, it is found that the gate-drain capacitance increases with increase in drain side doping.

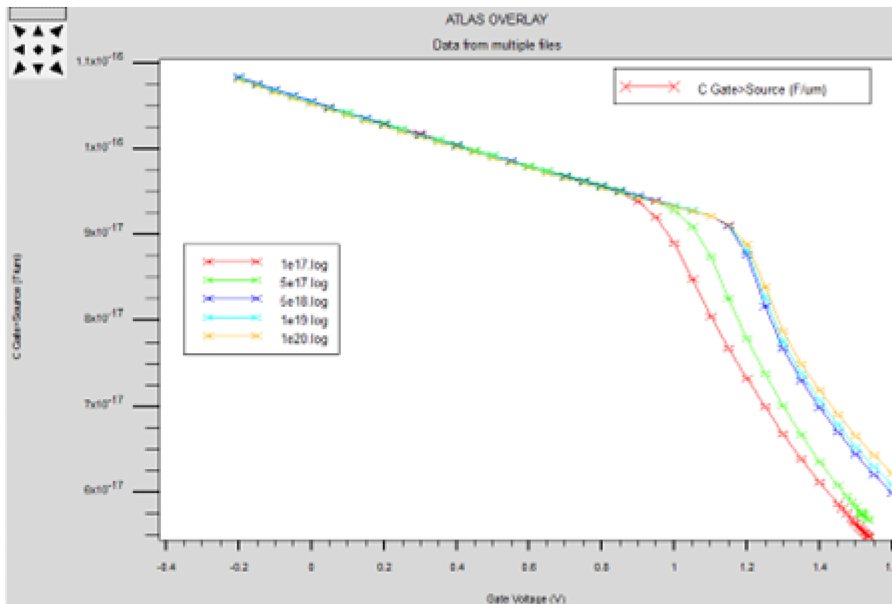

Fig. 5 Gate-source capacitance for various drain side doping.

Fig. 5 shows the gate-source capacitance (Cgs) for assorted drain side doping. The Cgs in Fig. 5 is comparable to the Cgd in Fig. 4. The trend of Cgs with Vgs is inverse to the trend of Cgd with Vgs. It is unlike behaviour to

the MOSFET. In MOSFET, both Cgs and Cgd increases with respect to Vgs. Further, unlike in Cgd, the doping in drain side effects the on-state gate-source capacitance.

XII.CONCLUSION

Tunnel FET is investigated in this paper. The development of TFET in 2018 and 2019 is presented. The new development in TFET is also presented. The performance metrics are collected from reported work. The on-current and power conversion efficiency are extracted from reported work and summarized in this paper. An in-depth inference of these collected data is provided in this paper. Furthermore, role of drain doping on capacitance of tunnel FET is investigated using TCAD simulator. The findings of this study are: (i) the gate-drain capacitance below subthreshold voltage increases with increase in drain doping and (ii) gate-source capacitance above subthreshold voltage decreases with increase in drain side doping.

Acknowledgment

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