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Error Detection and Correction for Golay Code & Extended Golay Code using Cyclic Redundancy Check

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ABSTRACT

In this paper certain optimization techniques are proposed to reduce the encoder and decoder computation time of cache memory that is affected by soft error and by implementing ECC such as cyclic and block codes. Error that is adjacent by a width of three and two bits are the prime concern of this thesis. Optimised Golay code (23, 12) and new block code size (32, 19) which is also optimised are presented. Nevertheless, cyclic code is efficient compared with block code however, the prime concern of the thesis is to address the triple and double adjacent errors which also includes single bit error, in this regard built-in capability of Golay code is optimised and used for comparison. The extended Golay code is implemented in term of number of slice, number of LUT and maximum combinational path delay compared with existing Golay code.

Keywords : Binary Golay Code (23, 12, 7), Extended Golay Code (24, 12, 8), Adder, Weight Measurement Unit

I. INTRODUCTION

Cyclic codes are sub classification of forward error correcting code which performs both error detection and correction through syndrome bit computation. Based on cyclic codes many codes are developed few well implemented and widely adopted codes are RS codes, CRC codes, BCH codes and Golay code and in this section the literature is presented in the same order [1]. In the case of cyclic codes, RS codes are used in optical disk encoding and decoding process. CRC codes are used in memory error correction. BCH codes is used in deep satellite communication, Golay code is adopted for generation of random sequence generation, used for testing purpose and These applications are not limited only for the codes specified these codes can be adapted to other application also, that involves data or information processing in a medium such as wireless etc., or in a solid state drives that is capable of storing data [2]. It made a study on cyclic code and concluded pseudo cyclic codes or better compared with cyclic codes for correction single errors at multiple levels. With this introduction few recent, early studies in cyclic codes are discussed below. They compared RS codes with Hermitian codes (algebraic geometric) over the field that contains elements 16, 64, 256, 512 and 4096 and concluded RS codes have a good coding gain over hermitians. But if the elements increase the bandwidth decreased. However systematic modified reed Solomon (SMRS) code proposed helps to increase

the bandwidth without trade off in coding gain. An efficient RS code should have less computation time, maximum error detection and correction capability, presented one such RS code which is capable of correcting bust error with minimum computation time through an efficient algorithm [3, 4].

Here by slightly increasing hamming sphere to half of the minimum distance results in increasing the error correction capability however RS codes or modified RS codes are more complex to design and at implementation its computational time and area of design increases this results in additional power and cost for implementation.

Accumulated charges in the diffusion layer will be undergoing a sudden change in velocity which leads to a change in value stored in the memory. This error can be corrected by radiation hardening circuits. To achieve this, an algorithm was proposed and compared with other error correcting codes. The circuit developed as SEU radiation hardening circuit deployed many EXOR gates, this design is good in detection and correction of errors but the results are considered only for the read and write time in the memory. Nevertheless it is not compared with any cyclic code [5, 6].

II. PROPSOED METHODOLOGY

In this section in concern to the main objective of this research optimised Golay code is proposed (23, 12). Extended golay code is not considered for this research because in general all the cyclic codes designed through irreducible polynomials are structured from the generation matrix followed by parity check matrix, its structure is realised through implementing flip flops for computing the syndrome bits. To realise the extended Golay code Equation (1) is used. In which two irreducible poly is shown, one poly with degree 16 holds a negative coefficient which is not suitable for realization moreover another poly of degree 8 is the only coefficient which also reduced the possibility of optimization, since the EXOR computation on the flip flop content is minimised this make the (24,12) code inherently the optimised code in form of matrix, to substantiate this proposed the major work in the design of parallel decoder and has not optimised the parity check matrix.

In the case of RS coded it is too complex to implement because the area overhead is high compared with other cyclic codes like BCH and Golay code. In addition recent study on RS codes are very few however few RS codes are being proposed in the area of non-binary RS codes which have its application in wireless channels. With this brief inherent ability of the golay code (23, 12) is explored and optimization is achieved in the generation matrix of this proposed work. Length of the proposed code ―n‖ is 23 bits, data bits ―k‖ is 12, and parity bits are 11.

$$(1 + D^{24}) = (1 + D^{8})(1 - D^{8} + D^{16}) \quad (1)$$

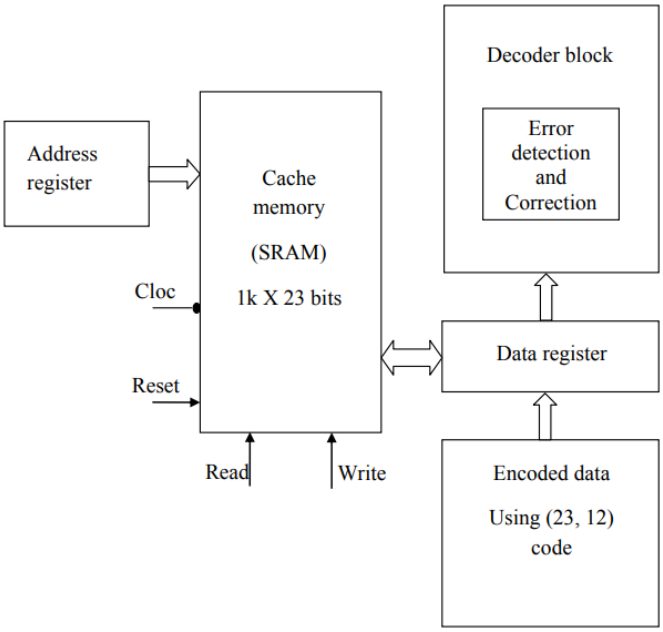

Figure 1: Flow Chart of Golay Encoder and Decoder

Figure 1 shown is the basic block diagram of proposed block code including memory. In which the capacity of the cache memory is 23 Kb that have 1 K rows and 23 columns. To address 1024 rows 10 bits address register is used. The data register size is same as the

width of the memory moreover few primary signals like, read, write, negative going clock, reset and the main blocks to encode and decode the data to and from the memory is also shown in Figure 1.

Golay Encoder:-

The encoding algorithm of Golay code is based on the cyclic redundancy check generation process and it includes Conversion of binary Golay code into extended Golay code.

Golay Decoder:-

First we gather the encoder yield information bits and to alter the decoder design utilizing expanded Golay code engineering. This design is to examination the in general encoder yield information. Then, at that point, to compute the greater part yield information bits and to look at the Golay code design information bit area. Then, at that point, to check the CRC key information bits. So we apply the CRC computation process and to tackle the last information bit in '0' level. Then, at that point, to gather the first message information bits. The result pieces are not equivalent to '0' level, so the blunder pieces are available in getting pieces.

Binary and Extended Golay Code Architecture:-

Binary Golay code has two types the first one is Golay (23, 12, 7). In this (23, 12, 7) Golay code, if we send 12 bit message, then we add additional 11 bits to it. After adding check bits which are obtained from CRC generation process to the 12 bit message, total will come to 23 bit now, we send this 23 bit. The 23 bit message obtained at receiver side is able to convert these 23 bit messages into 12 bit message even if there is distortion of 12 bit. This is applicable to all 23 bits and hence it is called a perfect Golay code. Another type is Golay (24, 12, 8).This code detects up to 4, but it can correct up to 3 bits error. The architecture of Golay code encoder is divided into two parts one is generation of G23 and other is conversion of G23 to G24.

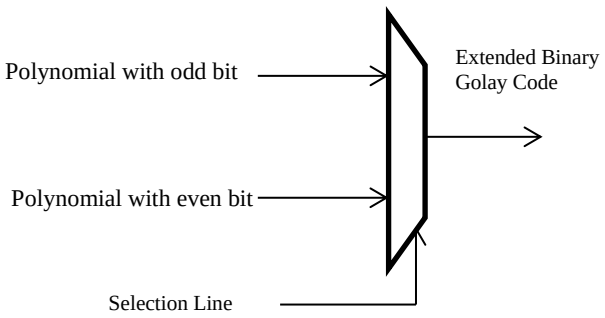

Figure 2: Binary Golay Code to Extended Binary Golay Code

III. SIMUALTION RESULTS

All the designing also test with respect to calculation that we have referenced in this paper is being created on Xilinx 6.1i refreshed form. Xilinx 5.2i has two or three the striking features, for instance, low memory essential, fast investigating, and insignificant exertion. The latest appearance of ISETM (Integrated Software Environment) plan mechanical assembly gives the low memory need estimated 27 rate low. ISE 6.1i that gives pushed gadgets like adroit request development with better use of their handling gear gives faster arranging end and better quality of results for a better time frame than organizing course of action. An ISE 6.1i Xilinx instrument gives more essential versatility for plans which impact embedded processors. The ISE 6.1i Design suite is joined by the appearance of chip scope ProTM 6.1i investigate and actually take a look at programming. By the aide of that item we examine the program successfully. Additionally included is the most current arrival of the chip scope Pro Serial IO Tool unit, giving streamlined investigating of rapid sequential IO plans for Virtex-2 FX and Virtex-2P LXT and SXT FPGAs. With the assistance of this device we can create in the space of correspondence as well as in the space of sign handling and VLSI low power planning.

1. CRC Technique

The architecture of CRC Golay code encoder has been implemented in field programmable gate array using Xilinx ISE tool.

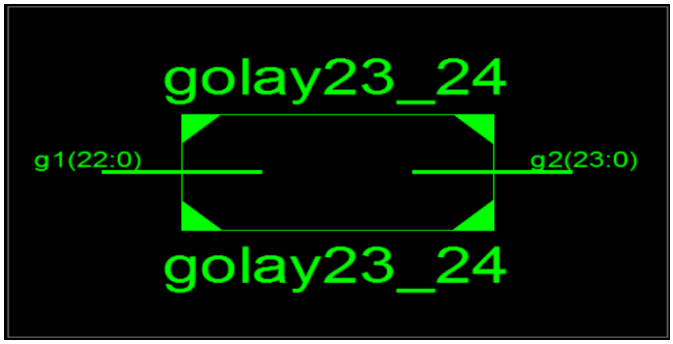

Figure 3: View Technology Schematic of CRC Technique

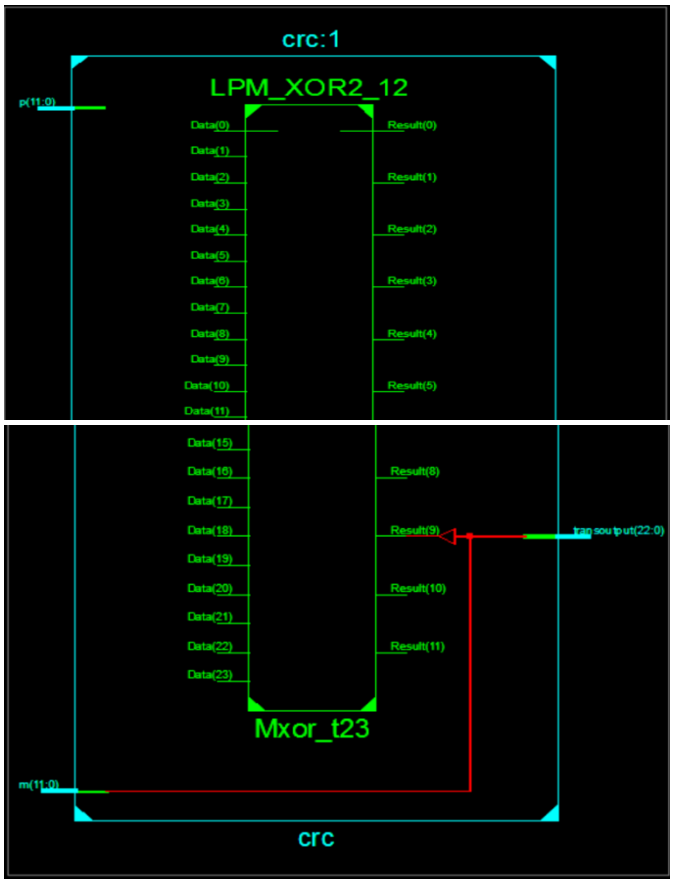

Figure 4: RTL View of CRC Technique

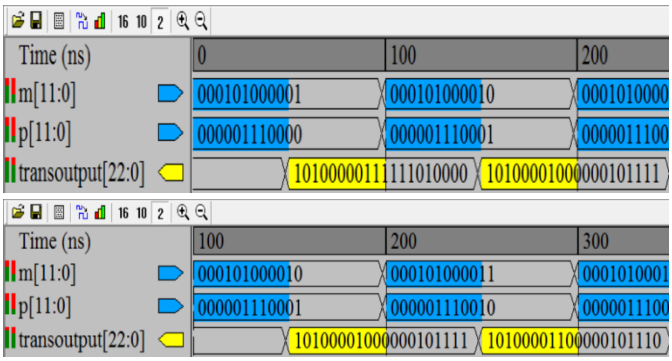

Figure 5: Output Waveform of CRC Technique

2. Binary Golay Code to Extended Golay Code:-

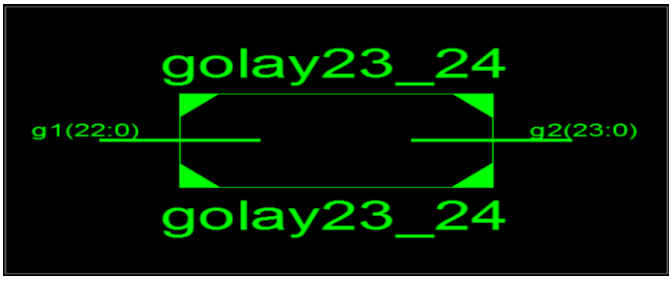

Figure 6: View Technology Schematic of Extended Golay Code

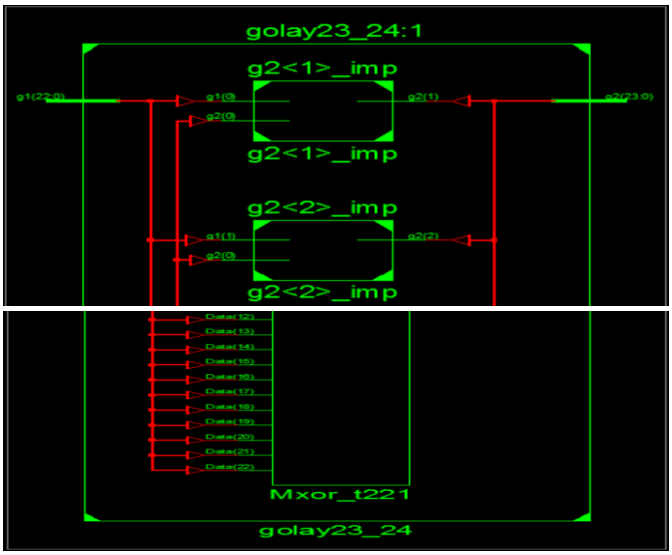

Figure 7: RTL View of Extended Golay Code

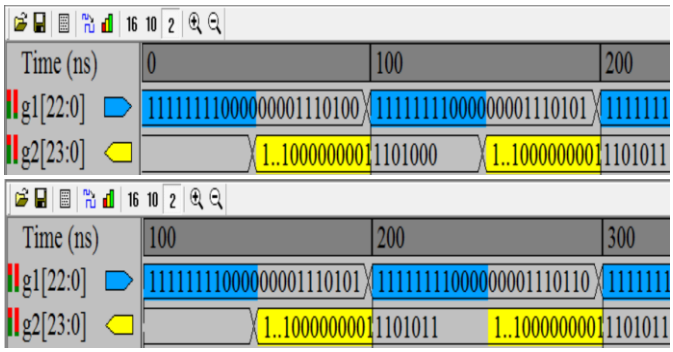

Figure 8: Output Waveform of Extended Golay Code

3. Weight Measurement Unit:

The weight measurement unit primarily counts the number of binary 1 in the sequence, which can be efficiently done by the circuit shown in Fig. 9, which results in less critical path delay.

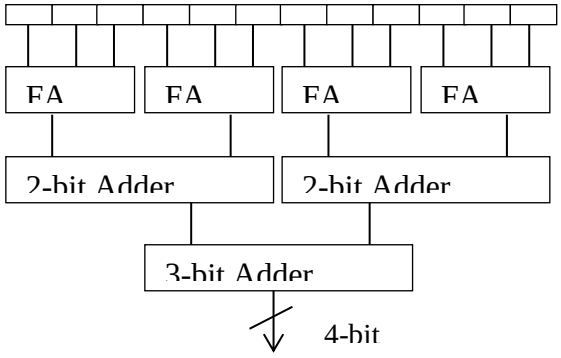

Figure 9: Structure of Weight Measurement

Table 1: Comparison result for weight measurement

Spartan-3			
Architecture	Slice	LUTs	Delay
Previous Algorithm	11 out of 768	19 out of 1536	13.069 nsec
Proposed Architecture	10 out of 768	18 out of 1536	11.823 nsec
Virtex-2			
Previous Algorithm	11 out of 256	19 out of 512	9.106 nsec
Proposed Architecture	10 out of 256	18 out of 512	8.139 nsec
Virtex-2p			
Previous Algorithm	11 out of 1408	19 out of 2816	8.205 nsec
Proposed Architecture	10 out of 1408	18 out of 2816	7.350 nsec

Table 2: Result for proposed Encoder and Decoder for Extended Golay code

Architecture	Slice	Flip Flop	LUTs	IOBs
Previous Algorithm	85	80	149	37
Encoder	17	3	27	39
Previous Algorithm	60	34	113	26
Decoder	53	23	92	47

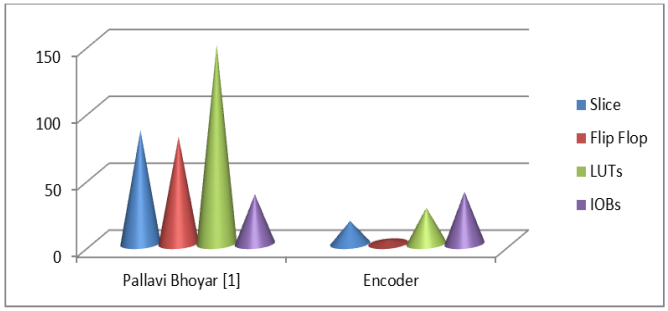

Figure 10: Shows the bar graph of the existing algorithm and proposed architecture

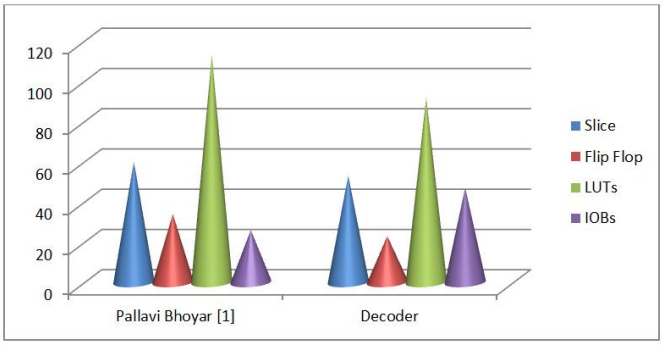

Figure 11: shows the bar graph of the delay in different device family

IV.CONCLUSION

From the simulation results it is observed that the prime concern on mitigating the soft errors more precisely the double and triple adjacent error that frequently occurs in the cache memory has been addressed and on implementation it shows the proposed cyclic code is the better optimized code for detecting and correcting double and triple adjacent errors including single bit error detection and correction. Moreover this proposed code is capable of detecting and correcting random errors to the maximum of six and three respectively however as the scope of the research proposed is limited to adjacent errors, random errors detection and correction is not considered in this proposed optimized cyclic code (23, 12).

V. REFERENCES

[1]. Nandivada Sridevi, K. Jamal and Kiran Mannem, “Implementation of Error Correction Techniques in Memory Applications”, Fifth International Conference on Computing Methodologies and Communication, IEEE 2021.

[2]. Kristjane Koleci, Paolo Santini, Marco Baldi, Franco Chiaraluce, Maurizio Martina And Guido Masera, “Efficient Hardware Implementation of the LEDAcrypt Decoder”, IEEE Access 2021.

[3]. P. Santini, M. Battaglioni, M. Baldi, and F. Chiaraluce, “Analysis of the error correction capability of LDPC and MDPC codes under parallel bit-flipping decoding and application to cryptography,”, IEEE Trans. Communication, vol. 68, no. 8, pp. 4648_4660, Aug. 2020.

[4]. J. Hu, M. Baldi, P. Santini, N. Zeng, S. Ling, and H. Wang, “Lightweight key encapsulation using LDPC codes on FPGAs”, IEEE Trans. Comput., vol. 69, no. 3, pp. 327_341, Mar. 2020.

[5]. D. Zoni, A. Galimberti, andW. Fornaciari, ``Efficient and scalable FPGA oriented design of QC-LDPC bit-flipping decoders for post-quantum cryptography,'' IEEE Access, vol. 8, pp. 163419_163433, 2020.

[6]. K.Koleci, M. Baldi, M. Martina, and G. Masera, ``Ahardware implementation for code-based post-quantum asymmetric cryptography,'' in Proc. 3rd Italian Conf. Cybersecurity (ITASEC), vol. 2597, Ancona, Italy, Feb. 2020, pp. 141_152.

[7]. D. Zoni, A. Galimberti, and W. Fornaciari, ``Flexible and scalable FPGA oriented design of multipliers for large binary polynomials,'' IEEE Access, vol. 8, pp. 75809_75821, 2020.

[8]. M. Baldi, A. Barenghi, F. Chiaraluce, G. Pelosi, and P. Santini, ``LEDAcrypt: QC-LDPC code-based cryptosystems with bounded decryption failure rate,'' in Code-Based Cryptography, M. Baldi, E. Persichetti, and P. Santini, Eds. Cham, Switzerland: Springer, 2019, pp. 11_43.

[9]. Shivani Tambatkar, Siddharth Narayana Menon, Sudarshan. V, M. Vinodhini and N. S. Murty, “Error Detection and Correction in Semiconductor Memories using 3D Parity Check Code with Hamming Code”, International Conference on Communication and Signal Processing, April 6-8, 2017, India.

[10]. Pallavi Bhoyar, “Design of Encoder and Decoder for Golay code”, International Conference on Communication and Signal Processing, April 6-8, IEEE 2016, India.

[11]. Pedro Reviriego, Shanshan Liu, Liyi Xiao, and Juan Antonio Maestro, “An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code”, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 34, No. 3, pp. 01-04, 2016.

[12]. Satyabrata Sarangi and Swapna Banerjee, “Efficient Hardware Implementation of Encoder and Decoder for Golay Code”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2014.

[13]. P. Adde, D. G. Toro, and C. Jego, “Design of an efficient maximum likelihood soft decoder for

systematic short block codes," IEEE Trans. Signal Process. vol. 60, no. 7, pp. 3914–3919, Jul. 2012.

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