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Design of Wireless Communication System by Integrating FPGA with Multicore SDR Development Platform

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ABSTRACT

Software defined radio is a feasible solution for reconfigurable radios, which can perform different functions at different times on the same hardware. The project uses integrating FPGA with multicore Software defined Radio development platform design wireless communication system. It constructs the system on the Matlab/Simulink environment in the way of Model-based Design, and realizes transmitter section with FPGA. Finally, it uses Hardware-in-the-loop co-simulation to observe the bits error rate of system under the white Gaussian noise channel disturbance of different SNR values. The performance of the baseband transmitter is analyzed using constellation and eye diagrams for different modulation techniques and different signal to noise ratios.

Keywords - Software defined radio, FPGA, Matlab / Simulink

I. INTRODUCTION

Modern society is increasingly dependent on digital communication systems in order to function properly a multitude of telecommunications standards in use today, ranging from mobile communication standards such as GSM, PHS, and UMTS, to wireless LAN standards such as WiMAX and IEEE802.11x as well as future standards based on UWB technology[1]. Wireless communication networks have become more popular in the past two decades since the advent of cellular communications. The rapid growth in cellular communications has proved that wireless communication is viable for voice and data services. Traditional wireless devices are designed to deliver a single communication service using a particular standard. With the steady increase of new wireless services and standards, single purpose devices with dedicated hardware resources can no longer meet the user's needs[2]. It is also expensive to upgrade and maintain a wireless system each time a new standard comes into existence.

A feasible solution to make communication systems more flexible and user friendly can be achieved through the software defined radio (SDR) concept, because as traditional transceiver technology requires users to have separate equipment for each standard however SDR offers the possibility of using one terminal to receive many standards through the use of wideband reconfigurable transceivers and software signal processing. The main challenge is to optimize the tradeoffs between performance, power consumption and cost.

II. SYSTEM OVERVIEW

The presentation includes the difference between the SDR and conventional radio, architecture and advantages of SDR, adoption and chain value of SDR, SDR related technologies, possible design issues, and the platform choices for implementing integrated FPGA with multicore SDR based wireless communication systems[3]. In the framework for the implementation of a wireless communication system in SDR is presented. This includes a brief introduction of wireless communication systems, with a block diagram of the end-to-end communication system architecture, and the methodology of implementation. An illustrative baseband communication system implementation, simulation and results are presented and discussed. Results of the simulation including constellation diagrams, eye diagrams, and output waveforms, for different modulation techniques are presented and analyzed[4]. The system is implemented on the Xilinx Spartan 3E FPGA (XC3S500E-4FG320C) platform. The results of the implementation are compared with the simulation results.

III. DEFINITION OF SDR

A number of definitions can be found to describe Software Defined Radio, also known as Software Radio or SDR. The Wireless Innovation Forum, working in collaboration [5].

Simply put Software Defined Radio is defined as: "Radio in which some or all of the physical layer functions are software defined".

A radio is any kind of device that wirelessly transmits or receives signals in the radio frequency (RF) part of the electromagnetic spectrum to facilitate the transfer of information. In today's world, radios exist in a multitude of items such as cell phones, computers, car door openers, vehicles, and televisions.

Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards[6]. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem, allowing multi-mode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades.

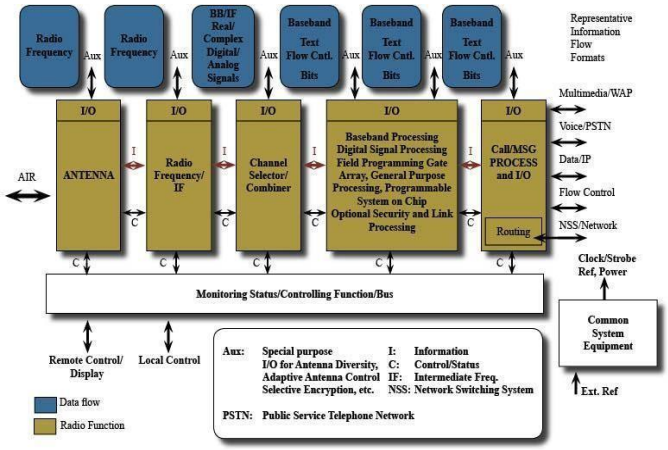

Figure 1 SDR

IV. ARCHITECTURE OF SDR

The RF section deals with up conversion from IF to RF and down conversion from RF to IF. The ADC/DAC blocks interface between the analog and digital sections of the radio system[7]. The ADC/DAC blocks perform analog-to-digital conversion and digital-to-analog conversion, respectively. DDC/DUC blocks perform digital-down conversion and digital-upconversion. Additionally, it performs modulation and demodulation of the signal. The baseband section performs baseband operations (connection setup, equalization, frequency hopping, timing recovery, correlation) and also implements the link layer protocol. The DDC/DUC and baseband processor are implemented digitally in a SDR and they require large computing power.

If the baseband section is implemented using ASICs, the function of the radio remains fixed reducing the flexibility of the radio. If DSPs are used for baseband processing, a programmable digital radio (PDR) system can be realized. In other words, in a PDR system baseband operations and link layer protocols are implemented in software. The limitation of this system is that any change made to the RF section of the system will impact the DDC/DUC operations and will require nontrivial changes to be made in DDC/DUC ASICs.

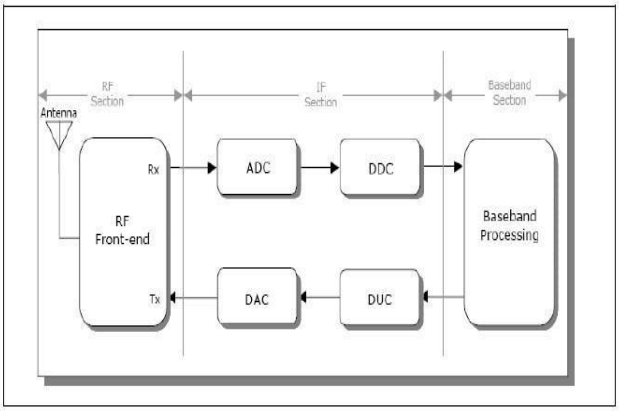

Figure2. Archtecture of SDR

In SDR system, the link-layer protocols and modulation/demodulation operations are implemented in software. If the programmability is further extended to the RF section (i.e., performing analog-to-digital conversion and vice-versa right at the antenna) an ideal software radio systems can be implemented[8]. However, the current state-of-the-art ADC/DAC devices cannot support the digital bandwidth, dynamic range and sampling rate required to implement this in a commercially viable manner.

V. SDR-RELATED TECHNOLOGIES

SDR can act as a key enabling technology for a variety of other reconfigurable radio equipment commonly discussed in the advanced wireless market[9]. While SDR is not required to implement any of these radio types, SDR technologies can provide these types of radio with the flexibility necessary for them to achieve their full potential, the benefits of which can help to reduce cost and increase system efficiencies:

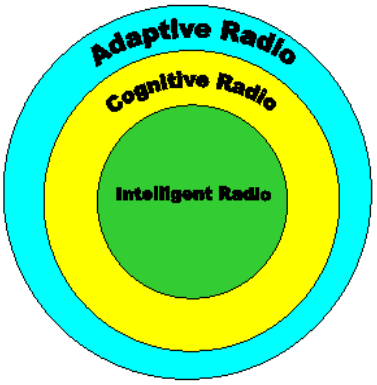

Figure 3 Defintion of SDR

• Adaptive Radio

Adaptive radio is radio in which communications systems have a means of monitoring their own performance and modifying their operating parameters to improve this performance. The use of SDR technologies in an adaptive radio system enables greater degrees of freedom in adaptation, and thus higher levels of performance and better quality of service in a communications link.

• Cognitive Radio

Cognitive radio is radio in which communication systems are aware of their internal state and environment, such as location and utilization on RF frequency spectrum at that location. They can make decisions about their radio operating behaviour by mapping that information against predefined objectives.

Cognitive radio is further defined by many to utilize Software Defined Radio, Adaptive Radio, and other technologies to automatically adjust its behavior or

operations to achieve desired objectives[10,13]. The utilization of these elements is critical in allowing endusers to make optimal use of available frequency spectrum and wireless networks with a common set of radio hardware. This will reduce cost to the end-user while allowing him or her to communicate with whomever they need whenever they need to and in whatever manner is appropriate and architecture of cognitive radio.

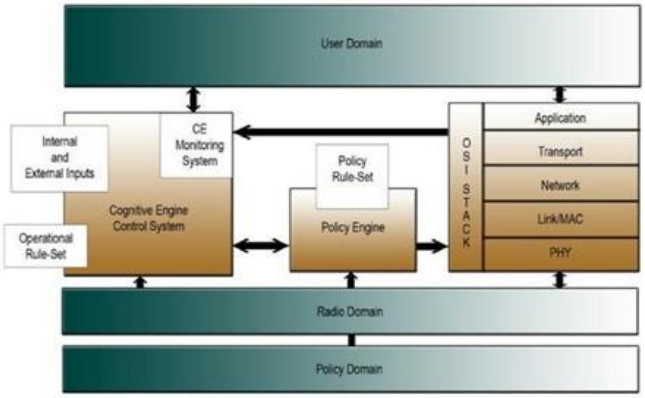

Figure 4 Cognitive Radio Architecture

• Intelligent Radio

Intelligent radio is cognitive radio that is capable of machine learning. This allows the cognitive radio to improve the ways in which it adapts to changes in performance and environment to better serve the needs of the end user.

In addition to utilizing SDR technologies, adaptive radio, intelligent radio and cognitive radio systems may all support dynamic spectrum access[11].

(DSA), allowing the systems to select the frequency spectrum in which they will operate at a given location and over a given period of time to optimize the use of available spectrum and avoid interference with other radios or other systems[12].

VI. SIMULATION WITH SIMULINK AND SYSTEM GENERATOR

In this paper, the algorithm is designed and simulated using Xilinx System. Generator system level tool. The Xilinx block set enables bit-true and cycle-true modeling and includes common parameterizable blocks such as finite impulse response (FIR) filter, fast Fourier transform (FFT), direct digital synthesizer (DDS), multipliers, and much more. The following are the key steps in the design simulation process using MATLAB SIMULINK and System Generator.

- Start the design by implementing the Xilinx blocks in the MATLAB SIMULINK model design.
- Select the Xilinx System Generator block and add it on the top of the design hierarchy.
- "Gateway In" and "Gateway Out" blocks are used to define the inputs and outputs to the Xilinx design. Xilinx gateway blocks automatically convert the double precision
- All the system components inside the gateway blocks should be Xilinx blocks only. However, any other MATLAB SIMULINK blocks such as scope, scatter plots and eye diagrams can be used to interface with Xilinx design and represented in system level. In this report, we used all three representations in the simulation.
- Then the design can be simulated and the outputs can be verified using visual output blocks like scopes or by writing the output to the MATLAB workspace.

Environment Required

Table 1 Requirement for simulation

Operating system	**Hardware**
Windows 7	• IBM-compatible desktop or laptop • Processor: Pentium i3 or better • RAM: 3 GB • Hard disk drive: 40 GB of free space or more • Display: 800 × 600 pixels or more
Software	
ARM/DSP development software • Texas Instruments, Code Composer Studio	

FPGA development software • Xilinx, ISE Foundation Xilinx Synthesis Technology(XST)
Model-based design software • The Math Works, MATLAB 7.11 (R2010b) • Simulink

VII. SYSTEM GENERATOR DESIGN

System Generator works within the Simulink model-based design methodology. Often an executable spec is created using the standard Simulink block sets. This spec can be designed using floating-point numerical precision and without hardware detail. Once the functionality and basic dataflow issues have been defined, System Generator can be used to specify the hardware implementation details for the Xilinx devices. System Generator uses the Xilinx DSP block set for Simulink and will automatically invoke Xilinx Core Generator to generate highly optimized net lists for the DSP building blocks. System Generator can execute all the downstream implementation tools to product a bit stream for programming the FPGA. An optional test bench can be created using test vectors extracted from the Simulink environment for use with ModelSim or the Xilinx ISE Simulator.

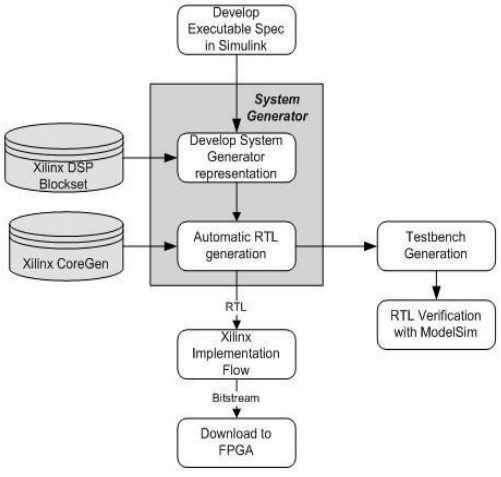

Figure 5 system generator design flow

A. TRANSMITTER MODEL

At the transmitter, the data from the source is input to the forward error correction block, which comprises of the convolutional encoder and puncturing system. The convolutional encoder is used for error correction in data transmission and it encodes the data sequence by inserting redundant bits. In the convolutional encoder, values are encoded by a linear feed forward shift register, which computes modulo-2 sums over a sliding window of input data.

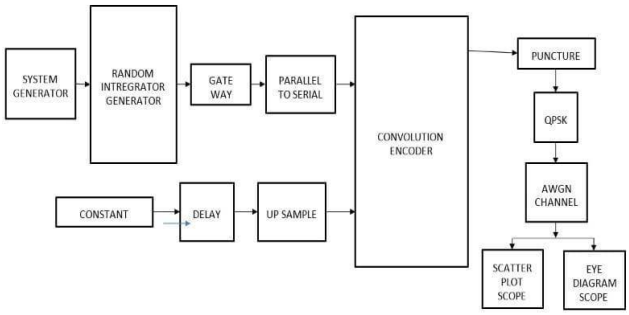

Figure 6. Transmitter design

In this report, a rate 1/2 convolutional encoder with constraint length 7 and code array 171 and 133 is used. Please note that the code array used is the optimal code array of constraint length 7. The constraint length denotes the number of shift registers over, the constraint length denotes the number of shift registers over, which the modulo-2 sum of the input data is performed.

The punctured data is modulated using QPSK modulation technique. The QPSK modulated data is then spread by pseudorandom noise (PN) sequence with a spreading gain of 16 before transmission. Please note that the spreading gain used in this thesis, is very small when compared with practical processing gains and is used only for illustrative purposes. The channel is modeled as an AWGN channel. Hence, only the AWGN model is considered in this report. Figure 4.5 shows the transmitter design for this project.

B. RECEIVER MODEL

At the receiver , the signal is first dispread and then demodulated. Then error correction is applied to the demodulated data. The signal is dispread with PN sequence generator with a spreading gain of 16 and demodulated using QPSK technique. The demodulated and dispread data is depunctured prior to decoding, by inserting nullsymbols in the punctured locations.

The depuncture blocks have the same depuncture codes as in the puncture blocks. Hence depuncture block 0 has a code of 10 and block 1 has a code of 11. Therefore, the null symbol is inserted after every other bit coming out of depuncture block 0. No symbols are inserted for block 1 as no bits were punctured. Since the bit B0 and D0 were punctured before transmission, null symbol is inserted in those locations and input to the Viterbi decoder along with the other bits.

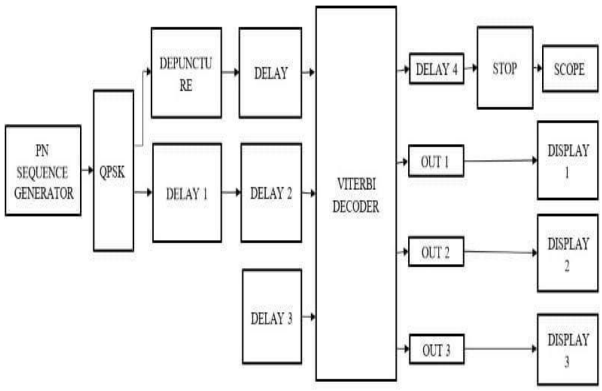

Figure 7. Receiver design

Viterbi decoder is used to decode the convolutionally encoded signal by finding an optimal path through all the possible states of the encoder. There are two steps to the decoding process. Either a Hamming or Euclidean metric may be used to determine the cost. The second step is to trace back through the trellis and determine the optimal path. The length of the trace through the trellis can be controlled by the trace back length parameter.

The constraint length of 7 and the code array 171 and 133 used for decoding are the same as in convolution encoder.The trace back length parameter, that is, the number of trellis states processed before the decoder makes a decision on a bit, is set to 48. The decoder outputs the data bits which are later grouped accordingly.

Convolution Encoder and Viterbi Decoder

The convolutional encoder of IEEE 802.16 Wireless OFDM PHY standard, which shall have native rate of 1/2, a constraint length equal to 7, and shall use the generator polynomials codes shown in Table 4.2 Equation to derive its two code bits:

$$\begin{cases} G_1 = 171_{OCT} & \text{for X} \\ G_2 = 133_{OCT} & \text{for Y} \end{cases}$$

For the 7th mode of channel coding, the Convolutional Code (CC) code rate is ½ is used in this project.

VIII. SIMULATION

The simulation model for punctured convolution encoder is shown in Figure 5.1. In this thesis, punctured convolution encoder of rate 2/3 with constraint length 7 is used. The data source random integer generator, output is input to the “Gateway In” block. This block converts the data in double precision to the Xilinx fixed point representation. From the “Gateway In” block, the data is parallel-to-serial converted and given to the data input port of the convolution encoder. The output from the data output port 1 of the encoder is serial-toparallel converted and given to the puncture block with puncture code 10. Every second, encoded output bit from data output port 1 is deleted by the puncture block after serial-toparallel conversion.

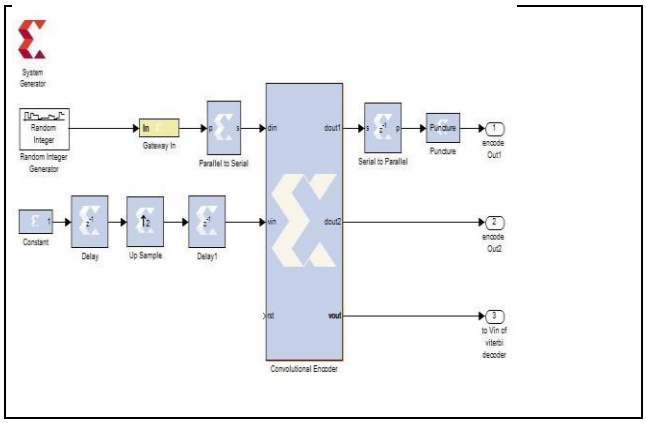

Figure 8 Encoding and puncturing

A constant value of 1 is used as input to the input port (Vin) to specify to the encoder that the data on its input port is valid and is ready to be encoded. When there is valid output on the output ports of the encoder, the valid output port (Vout).

Constellation point becomes a cloud around the central point. When the noise is more in the channel, the constellation points spreads around the central point. While demodulating in the receiver, the chances of misinterpretation of one point as other is more and this leads to incorrect demodulation and error.

IX. CONCLUSION

The project work proposes a wireless communication system on multicore SDR development platform and also seen that during simulation if signal to noise ratio (SNR) for AWGN channel increased the system expecting good results with less distortion.

Although some modes' BER are not good enough, it can be tried on FPGA integrated SDR development platform.

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