Print ISSN : 2395-1990
Online ISSN : 2394-4099
www.ijsrset.com

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IJSRSET

National Conference on "Innovative Research on Robotics, Circuits and Technology" (IRCT 2018)

Organised by
CIrcuit Branches of
Sri Chandrasekharendra Saraswathi Viswa Mahavidyalaya,
(EEE,ECE,EIE & Mechatronics)
Kanchipuram, Tamil Nadu, India

VOLUME 5, ISSUE 1, MARCH-APRIL-2018

INTERNATIONAL JOURNAL OF SCIENTIFIC RESEARCH IN SCIENCE, ENGINEERING AND TECHNOLOGY

UGC Approved Journal [Journal No : 47147]

Email : editor@ijsrset.com Website : http://ijsrset.com

National Conference on "Innovative Research on Robotics, Circuits and Technology" (IRCT 2018)

21st & 22nd March 2018

In Association With

International Journal of Scientific Research in Science, Engineering and Technology

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Transformer Protection by Using Microcontroller Based Differencial Relay

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ABSTRACT

The main objective of this work is to design and implement a system that uses to transformer protection by using the microcontroller based differential relay and other peripheral devices . The design implementation and testing of the system are also presented with peripheral devices to protect transformer.

Keywords: Transformer, differential relay, current transformer, fault current

I. INTRODUCTION

Power transformers are very expensive and vital equipment in electric power systems. The fault accurse rarely from insulation failures caused by atmospheric disturbances and switching surges. These faults can be classified into two main classes. The first class is internal faults due to faults between adjacent turns or parts of coils and faults to ground on terminals or on parts of windings. The second class is overload and externally applied conditions include over current,over voltage,external short circuits and reduced system frequency.

This study describes the design and implementation of the microcontroller based differential relay protecting system for the single phase transformer. In this study software and hardware of microcontroller based differential relay has been constructed and designed. The design implementation and testing of the system are also presented.

Electromechanical and solid-state relays were and still used for protecting power system for the past several years. Researchers have been studying the feasibility of designing relays using microprocessors (1).Due to the advancement in digital technology and decreases in digital hardware process, digital relays are now available and being used for power system protection. Which are contribute to improved reliability and reduced costs on electric power systems (2)

II. PROBLEM ASSOCIATED WITH DIFFERENTIAL PROTECTION SYSTEM

When the transformer is energizing the transient inrush of magnetizing current is flows in the transformer. This current is as large as 10 times full load current and its decay respectively. This magnetizing current is flows in the primary winding of the transformers due to which it caused a difference in current transformer output and it makes the differential protection of the transformer to operate falsely.

To overcome this problem the kick fuse is placed across the relay coil. These fuses are of the time limit

with an inverse characteristic and do not operate with short duration of the switch in the surge. When the fault accurse the fuses blow out and the fault current flows through the relay coils and operate the protection system. This problem can also be overcome by using a relay with an inverse and definite minimum type characteristic instead of an instantaneous type.

III. PRINCIPLE OF DIFFERENTIAL PROTECTION

Principle of differential protection scheme is one of simple conceptual technique .The differential relay (Figure 1) actually compares between primary current and secondary current of power transformer, if any unbalance found in between primary and secondary current s the relay will actuate and inter trip both the primary and secondary circuit breaker of the transformer. Suppose you have one transformer which has primary rated current Ip and secondary current Is. If you install CT(Figure 2) of ratio Ip/1Aat the primary side and similarly, CT of ratio Is/1A at the secondary side of the transformer. The secondaries of these both CTs are connected together in

such a manner that secondary currents of both CTs will oppose each other. In other words, the secondaries of both CTs should be connected to the same current coil of a differential relay in such an opposite manner that there will be no resultant current in that coil in a normal working condition of the transformer due to which the normal ratio of the transformer disturbed then the secondary current both transformers will not remain the same and one resultant current will flow through the current coil of the differential relay. Which will actuate the relay and inter trip both the primary and secondary circuit breakers.

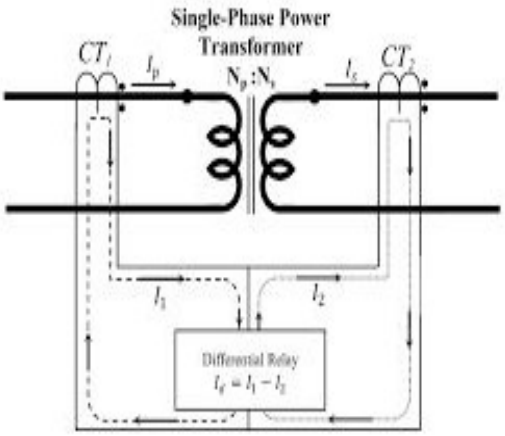

Figure 1. Single Phase transformer

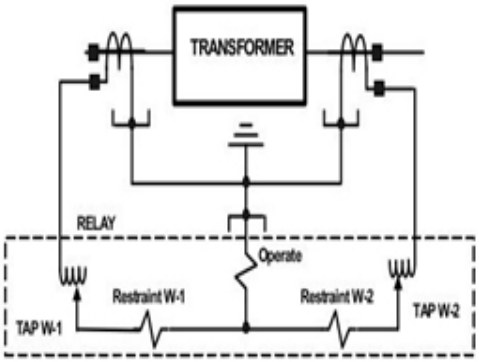

Figure 2. Basic Differential Relay

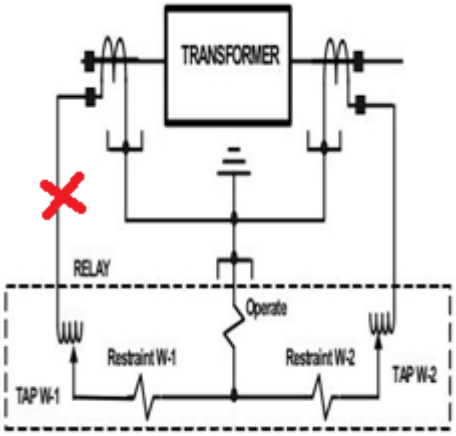

Figure 3. Identification of Fault current in CT

IV. PROPOSED BLOCK DIAGRAM FOR TRANSFORMER PROTECTION

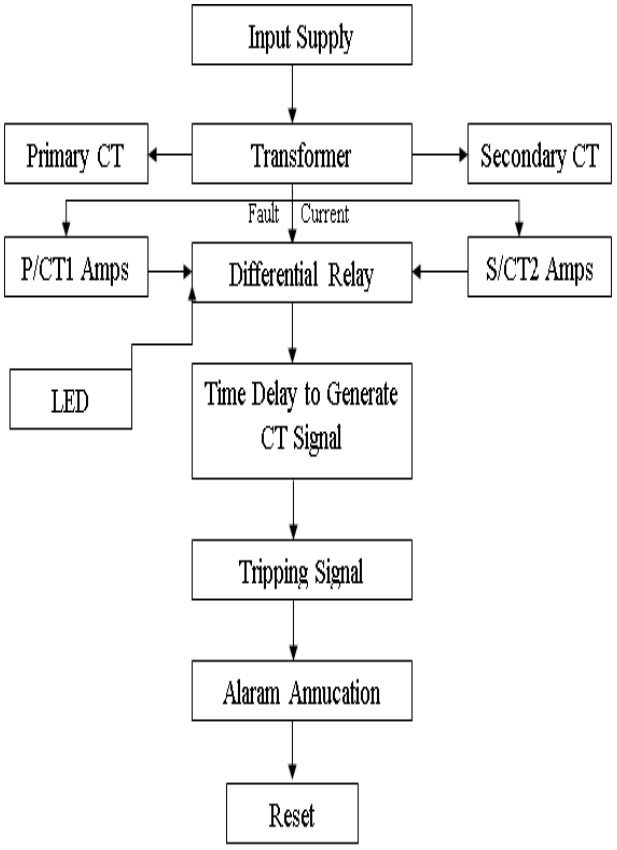

Figure 4

The relay which is used to check the difference between the output and input currents for power system current is known as differential relay. The basic function of this relay working according to the principle of Faraday.s current law. The difference amongst the currents may also be in phase angle or in magnitude or in each.

For hale and energetic operation, angle and magnitude variations must be zero. In case there's a difference which difference go beyond some value, the relay can work and interconnected electrical fuse can disconnect. How to measure and protect current transformer. Allow us to assume an easy example of an influence power transformer with transformation magnitude ratio relation 1:1 and (y/y) connection and therefore the CT1 and CT2 ensure a similar transformation magnitude relation as shown.

The current flows within the primary side and secondary side of power transformer are equal presumptuous ideal power transformer. The secondary current I_1 and I_2 are same in magnitude and reverse in direction Therefore the net current within the differential is nil at load situation (without any fault), and therefore the relay won't operate.

Assigning the previous one the power transformer with an external fault is shown. During this case the two currents I_1 and I_2 can increase to terribly high magnitudes values however there's no modification in phase angle. Hence net current within the differential coil continues to be zero and therefore the relay won't operate.

In the same condition internal fault occurs the fault current I1 and I2 are non zero value hence the difference current I_1 or I_2 whichever is high gives the relay to trip the circuit on both the primary and the secondary sides.

V. CONCLUSION

By using this set-up kit we can studied and to understand the basics of terminology in addition of this work The single phase transformer protection by using microcontroller based differential relay was constructed , designed and the function are verified successfully.This objective was achieved effectively and output results are verified practically by using set-up kit

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

A Survey on low power and memory efficient VLSI architecture for million bit multiplier Design

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ABSTRACT

The motto of this proposal is to design an area and memory efficient VLSI architecture for million bit multiplier design. The proposal work split the multiplier bit into 3FIFO architecture through NTT Ram technology. The final architecture include the Synchronizer, state control module as well as 3 state FIFO buffer module .The synchronizer module is used to synchronize the NTT RAM and state controller arbiter. The state controller module gives the control signal and priority of the multiplier design. The FIFO module is used for split the million bit multiplier into 8 bit multiplier i.e 256value.here we are going to design 3fifo module ,so we can achieve 256*256*256 bits of value aprx million bit, Based on this technology we have to achieve high speed as well as low power dissipation finally memory efficient vlsi architectures.

Keywords: VLSI, FIFO, NTT, Synchronizer, Statecontroller.

I. INTRODUCTION

This brief proposes a double modulus number theoretical transform (NTT) method for million-bit integer multiplication in fully homomorphism encryption[1]. The employment of double modulus enlarges the permitted NTT sample size from 24 to 32 bits and thus improves the transform efficiency. Based on the proposed double modulus method, we accomplish a VLSI design of million-bit integer multiplier. Implementation results on SPARTON-6 FPGA

Most of the earlier works focus on reducing the multiplication time but give small concern to area efficiency. Area efficiency is also moderately significant, because high area cost implementations normally require a high-end field-programmable gate array (FPGA) platform or a high gate count ASIC platform, both of which are too costly for practical applications. The purpose of this brief is to design a fast million-bit integer multiplier without compromising its area efficiency in hardware NTT[1].

In previous works, First implemented technologies on million-bit integer multiplier using FHE processing and then consider hardware employing fast Fourier transform using recursive multiplication Algorithm[2]. Third existing an architecture design of 768k-bit multiplier on Stratix-V FPGA.In these paper consider high speed and low power dissipation memory efficient architectures[3].

FPGA Implementation of a large number multiplier for FHE explains about 1st plausible scheme for FHE and it also advance development in the field of

information security[6]. They have long latency FPGA Implementation is twice as fast as the same FFT algorithm.

Accelerating Integer Based fully Homomorphic encryption using combo multiplication explains about allows computation on encrypted data[5]. But it is not used for real time applications.

VLSI design of a large number multiplier for FHE explains discuss about power efficient based on FHE and FFT operations[7]. Optimized multiplication architectures for accelerating FHE[2] shows that speed improvement by factor of 130 is possible

II. EXISTING SYSTEM

In these design, two 1024k bits integers A and B are divided into 64k pieces of 32-bit words (the first 32k pieces are padding zeros). A and B modulo $p2 = 216 + 1$ is computed and the 17-bit result together with the unique word (modulo $p1$) are input into two 81 × 216 bits RAMs: NTT_RAM_A and NTT_RAM_B, correspondingly.

Then, two pipeline double modulus NTT units are employed to designed NTT *(A)* and NTT *(B)*.

The NTT results are put back into NTT_RAM_A and NTT_RAM_B. In the 2nd stage, the digit wise multiplication results of $C[i] = NTT(A)[i] * NTT(B)[i]$ are designed and the results are stored in a 81 × 216 bits

RAM (INTT_RAM_C). One pipeline double modulus INTT unit is employed to designed INTT*(C)* and the results are put back into INTT_RAM_C. Lastly, the INTT results are input to a pipeline CRT-accumulation unit to obtain the final multiplication result.

They use schonhage-strassen large integer multiplication algorithm with a maximum word length of a few million bits. Number theoretical transform: It is generated by fast Fourier transform by replacing with a primitive root of unity[1].

Schönhage–Strassen algorithm is a special kind of discrete Fourier transform (DFT) defined over a finite field $Zp = Z/pZ$.Let ω be a primitive nth root of unity in Zp.$\boldsymbol{a} = (a0, a1, \ldots, an-1)$ be a vector of degree n, where coefficient$ai \in Zp$, $i = 0, 1, \ldots, n-1$. The n-point NTT of vector $\boldsymbol{a}$ (denotedby $NTTn\omega(\boldsymbol{a})$) is defined as$Ai = NTTn\omega(\boldsymbol{a})i = n-1_j=0 a j\omega i j \bmod p$.

(1)The n-point inverse number theoretical transform (INTT) of vector A (denoted by $INTTn\omega(\boldsymbol{A})$) is defined as$INTTn\omega(\boldsymbol{A})\, i = n-1 * NTTn\omega-1(\boldsymbol{A})\, i=n-1 * n-1_j=A j\omega-i j \bmod p$.

Each NTT point is generated by two modules and the result can be generated by chines remainder theorem. They can design and implement 12 bit in a NTT module. In this Existing they have high end field programmable gate array. Its is very much costly for practical applications. High area cost implementation

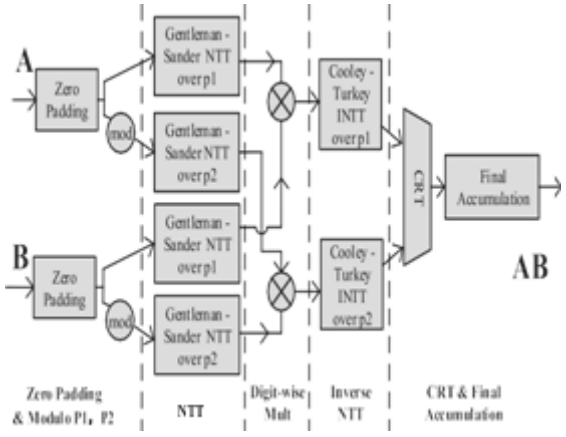

Figure 1. multiplication architecture based on double modules NTT.

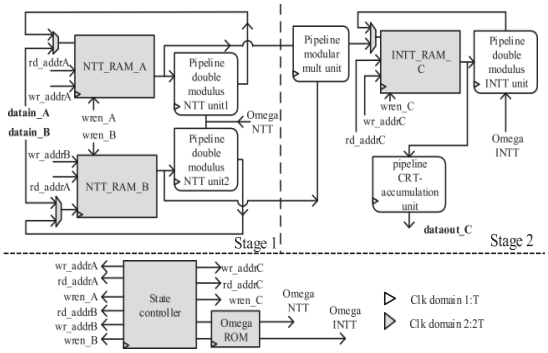

Figure 2.VLSI architecture of integer multiplier

It shows that multiplication architecture based on double modules NTT and VLSI architecture of integer multiplier.

III. PROPOSED SYSTEM

In this proposed system to design a area and memory efficient VLSI architecture for million bit multiplier design. In this to split the multiplier bit into 3FIFO architecture through NTT RAM technology. It includes Synchronizer, State control module and 3FIFO buffer module. The synchronizer module is used to Synchronizer the NTT RAM and state controller arbiter. The state controller module gives the control signal and priority of the multiplier design.

Figure 3. NTT RAM through FIFO

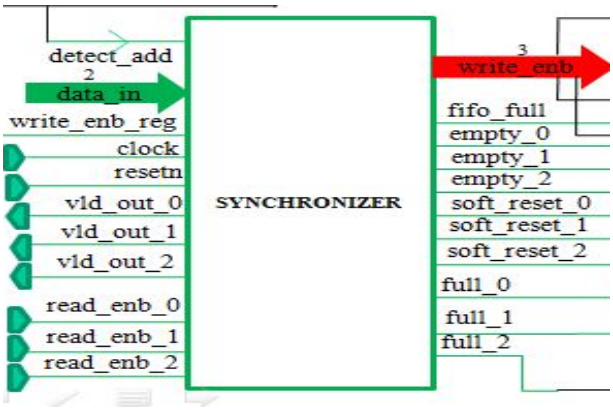

Figure 4. Synchronizer

Figure 5. State controller arbiter

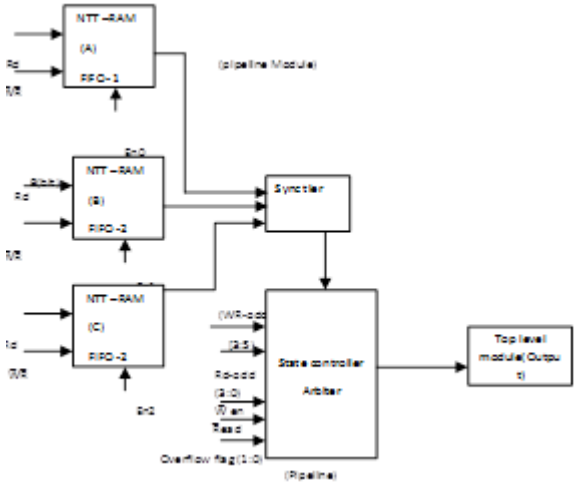

Figure 6. Proposed Block diagram

The FIFO module is used for split the million bit multiplier into 8-bit multiplier i.e. 256 value. Here we are going to design three FIFO module, so we can achieve 256*256*256 bits of value approximately million bits, based on this Technology. We have to achieve high speed as well as low power dissipation. At last, efficient VLSI architecture.

FIFO module means buffer module commonly used in Digital communication, Digital signal processing, VLSI. This FIFO modules are verified using in test benches by writing and reading values to and from the FIFO while observing the RAM data and the condition of output flags.

The synchronizer module is to synchronizer the NTT RAM and state controller arbiter. The state controller arbiter gives the control signal and priority multiplier of the design.

IV. CONCLUSION

Based on these technology, they have more area efficient, significant reduction on computing time,Less costly than the cache architecture. We can achieve 256*256*256 bits of approximately million bit integer multiplier design.

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Artificial Sleep Inducer Using Geo-Magnetic Field

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ABSTRACT

The magnetic field which originates naturally in the earth is called Geo magnetic field. It is also called earth's magnetic field. It is developed within earth which extends into space and interacts with solar wind charged particles from the sun. It generated by electric current in the conductive material of its core. People usually feel that they sleep well in the natural contiguous like tent or hut. This is because of our ability to perceive natural earth's magnetic field without our knowledge. At times people with sleep sickness mess a lot during night times. The amount of sleep a person requires depends on many factors, mainly for elder's 8-10 hrs of sleep. Geomagnetic field varies with place and also intensity. There is no proper method to find its level. Hence this paper presents a sleep inducer for insomniac and depressed people to create this type of magnetic field artificially. It is difficult to generate radiation with electrical circuits and it is unsafe as well. Out design will reason currents to ring at specific frequency. A glorified coil of wire and pair of separated metal plate called LC circuit can produce oscillating currents. Hence, it creates electromagnetic field through a radiator coil. This will help people those who are powerless to sleep and pretentious by insomnia, depressions. Even for twitchy kids this sleep inducer helps at times. This set up should be placed under a pillow of the subject. This will induce soporific sleep.

Keywords: Geomagnetic Fields, Depression, Sleep Inducer, LC Circuit, Insomniac, Radiator Coil

I. INTRODUCTION

Our body needs sleep to rest and recover energy. If the sleep is inadequate, then the performance of brain and body goes down. One becomes irritable and cannot concentrate on their work. After several days of inadequate sleep, one may start hallucinating. Usually people use sleeping pills or other drugs for restful sleep. But these drugs may cause some side effects and health issues. Hence in order to induce deep, restful, prolonged sleep without drugs magnetic field is generated which imitates geomagnetic field. This magnetic field produces sleep patterns similar to waves produced during deep sleep.

Sleep is natural and periodic state of rest during which consciousness of world is suspended. Human being spends 36% of their life in sleeping. Sleep is actually an active period during which lot of processing, restoration and strengthening occurs.

Table 1. Sleep time requirement at various age.

People classified according to age	Sleep requirement (hours/day)
Infants	12-15
Toddlers	11-14
Pre-school children	10-13
School-age children	9-11
Teenagers	8-10
Adults	7-9

Sleep is a restoration stage at which the brain accumulates metabolic wastes. Sleep plays an important role in cleaning out brain each night and these toxins can be flashed out during waking hours. Sleep helps us to solidify and consolidate memories. Each and every day our brain collects lot of information in short term memory. This information are processed during sleep and transferred to long term memory. Sleep having superior power and influence metabolic health.

SLEEP DISORDERS

Sleep disorders is also called as somnipathy. It is a disorder that causes changes in sleep patterns in brain. This leads to diverse effects like day time drowsiness, irritability, lack of concentration and other physical disorders.

Types Of Sleep Disorders

- ✓ Snoring
- ✓ Sleep apnea
- ✓ Insomnia
- ✓ Sleep deprivation
- ✓ Restless leg syndrome

II. METHODOLOGY

EFFECT OF MAGNETIC FIELD ON SLEEP

By accelerated theory of transition, deep sound sleep can be induced by using low strength magnetic field. This magnetic field induces prolonged and sound sleep without drugs. The main advantage of this effect is not harmful for users. It will create a moment to sleep deeply without any commotion.

MAGNETIC EFFECT OF EARTH AND SLEEPING POSITION

Our earth has magnetic dipole which is stretched from north to south positive pole is at north and negative pole is at south. This north-south direction retards the blood flow through brain capillaries and affects the brain cell function. When a person sleeps by facing towards north, it causes disturbed blood flow, restlessness and disturbed sleep. Because the magnetic field of earth and body is not oriented. When a person sleeps by facing towards south, there is mutual attraction exists between body and earth's magnetic field. This effect of magnetic field helps in sleeping and wake up fit and fresh. Similarly when we sleep facing our head towards eastwards, the magnetic lines of force enters through head and exits through feet which cools up the head and induces sleepiness. So, it is better to sleep by facing our head towards eastwards or southwards. Like this, sleeping position also helps us in sleeping.

III. BLOCK DIAGRAM

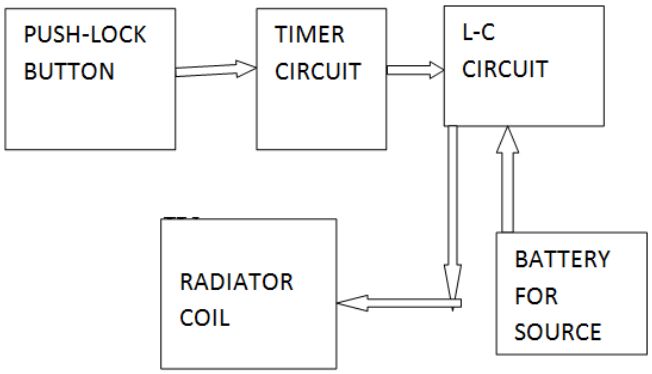

Figure 1. Block diagram to generate geomagnetic field.

TIMER CIRCUIT

This device consists of one timing circuit which is used to preset the period of time the electromagnetic field should be produced. There are two modes of operation 'stop' and 'alternate' modes which are regulated using switch. When the switch is opened then it operates at 'alternate' mode and starts producing electromagnetic field until the preset time and switch gets closed. When the switch is closed it operated at 'stop' mode and electromagnetic field production gets stopped.

LC TANK CIRCUIT

LC circuit is used for producing oscillating current which creates electromagnetic field through radiator coil. LC circuit is oscillating at its natural frequency, so it can able to create electrical energy. LC oscillator comprises of an inductor L and a capacitor C. If the

inductor and capacitor are connected in series, it provides voltage magnification. But in our project we need to magnify current hence the inductor and capacitor pair is connected in parallel which forms a tank circuit. In current amplification, capacitor and inductor are connected in parallel along with switch and voltage source.

IV. WORKING

This device is based on Faraday's law of electromagnetic induction .

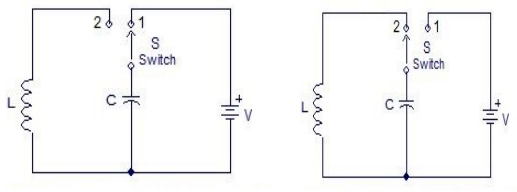

Figure 2. Two different Tank circuits

In first case, the switch is connected across the capacitor and voltage source whenever the switch gets closed the capacitor starts charging. In second case, the switch is connected in between capacitor and inductor whenever this switch gets closed the capacitor starts discharging through the inductor. Due to discharging, the voltage across capacitor starts decreasing consequently current across inductor increases. This current is used to create electromagnetic field by using radiator coil.

Timing option is selected using one rotator switch. It has two made of operation 'stop' and 'alternate'. It is chosen by using another rotary switch. When this switch is closed it operates on stop mode. The electromagnetic radiation stops after the preset time. When the switch is opened, it operates on alternate mode. This mode operates for preset time, and then pauses for same amount of time, this cycle repeats. This set up should be placed under the pillow while sleeping.

V. RESULTS AND DISCUSSION

This device produce electromagnetic field which makes the surrounding fit for deep, sound sleep. Mainly, it avoids the use of sleeping pills by the people who are unable to sleep. It induces prolonged sleep. Using this device, we can able to research further more. This device helps depressed and insomniac people for their deep sleep. It makes the surrounding suitable to sleep well. It does not produce any side effects

VI. CONCLUSION

At first, The electromagnetic coil produced by this device is having strength of very small range. Hence the measurement of magnetic field is difficult. By getting propesources from tank circuit the radiator coil started working automatically. So this device is not harmful to the brain. Hence it is grateful for sleep disorder cases. It helps insomnia patients to sleep well. They can easily recover from sleep disorder. It is easy to operate.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

A Study and Analysis of Bone Fracture Detection Methods

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ABSTRACT

Image processing is famous in modern data storage and data transmission especially in progressive transmission of images, video coding (teleconferencing), digital libraries, image database, and remote sensing. Nowadays image processing is widely used in medical image processing which comprises medical image enhancement and visualization, and edge detection. One of its major applications is fracture detection using X-ray images. Fracture in bone occurs when an external force exercised upon the bone is more than what the bone can tolerate or bear. The fracture can occur in any bone of our body like wrist, heel, ankle, hip, rib, leg, chest etc. In this paper we discuss about the types of bone fracture that commonly occur, types of filters we can remove the noise from degraded image and the edge function is used to detect edges, which are those places in an image that correspond to object boundaries.

Keywords: Bone Fracture, Medical Imaging, Edge Detection, X-ray images.

I. INTRODUCTION

Medical imaging is the technique of crafting visual representations of the internal parts of a body for clinical analysis and medical intervention, as well as visual representation of the function of some organs and tissues. As per the last years, the amount of medical image data grew from Kilo- to Terabyte[1]. The method of processing the medical image further for the better view by using the image processing technique is called Medical Image Processing. This is mainly due to improvements in medical image acquisition systems with increasing pixel resolution and faster reconstruction processing. Radiations are passed through the body of the human to view take images of the interior portion of the human. There are two types of radiations are used. They are ionising radiation and non-ionising radiation. Ionizing radiation in medical imaging embraces x-rays and γ-rays. X-rays are mainly taken to view the bones. The most common ailment of human bone is fracture [2]. A bone fracture is a

Medical condition in which there is a break in the continuity of the bones. Sometimes fracture is not clear in x-rays, Image processing helps in such cases to detect fracture. Computer detection of fractures can promote the doctors by flagging suspicious cases for closer examinations and thus improve the timeliness and accuracy of the diagnosis.

II. TYPES OF BONE FRACTURE

The human body has 206 bones with various shapes, size and structures. The common problem for the bone is fracture. Fracture in bone occurs when an

external force exercised upon the bone is more than what the bone can tolerate or bear. Depending on the impact of the force, some of the fractures are more terrible and dreadful than others. Sometimes the specific bone involved, and the age of the person and general health conditions also determine the severity of the fracture.

Comminuted fracture:

A comminuted fracture is a break or flake of the bone into more than two fragments [3]. It is caused by high-impact trauma such as in vehicular accidents. Treatment: a comminuted fracture often requires open surgery to restructure the bone to normal anatomy [3].

Greenstick fracture:

A greenstick fracture is a fracture in a budding, soft bone in which the bone bends and breaks. The fracture usually occurs in children and teens because their bones are flexible, unlike adults whose more brittle bones usually break [3]. Treatment: Removable splints result in better consequences than casting in children with torus fractures of the distal radius.

Transverse fracture:

A fracture in which the break is among a bone, at a right angle to the long axis of the bone. Transverse fracture results from a direct blow, but it can also sporadically occur when people do things repetitively, like running. Treatment: surgically put the bone back together, and they may employ things like metal pins, plates, or screws so that the bone will stay in place and heal completely [3].

Avulsion fracture:

An avulsion fracture is an injury to the bone in a location where a tendon or ligament attaches to the bone. It is caused by the tendon or ligament pulls off a piece of the bone while the bone is moving in the opposite direction. It is more generic in children[3]. Treatment: when the shatter of bone is pulled more than numerous centimetres from its normal position does surgery need to be considered.

Oblique fracture:

An oblique fracture is a relatively common fracture in which the bone breaks diagonally. It can vary in severity, depending on what bone is affected and how large the break is. It tend to occur on longer bones like the femur or tibia[4].

Spiral fracture:

A spiral fracture (torsion fracture) is a bone fracture occurring when torque (a rotating force) is applied along the axis of a bone. It often occur when the body is in motion while one extremity is planted[3]. For eg., a spiral fracture of the tibia (the shinbone) can occur in young children when they fall short on an extended leg while jumping.

Impacted fracture:

A bone fracture in which one of the shatter is driven into another fragment[5]. An impacted fracture is when a force mashes against both ends of the bone, pushing the broken ends together.

Fissure fracture:

Fissure fracture a crack extending from a surface into, but not through, a long bone.

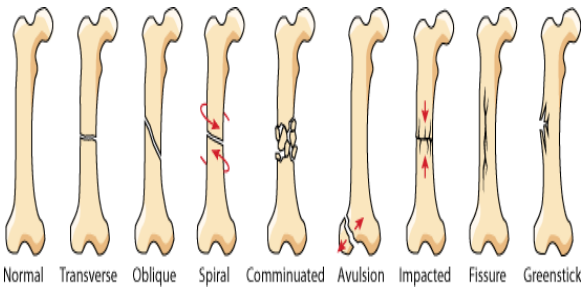


Figure 1

III. STEPS INVOLVED IN BONE FRACTURE DETECTION

By surveying various papers we concluded the steps involved to found the fractured bone. First user must give an x-ray image as an input to be processed, the image will then be carried filtering to remove noise

that exist in the image. Then, Edge detection is used for assimilation of blurred frame broad classification among smooth and rough surface classification of cement and asphalt[6]. A broken bone is expressed when the line has an end, and do not have a connection with another line. A broken bone stated, if the lines form an angle under 145 degrees, even supposing the line still has a connection with the other lines. The modules for bone fracture detection are shown in the block diagram:

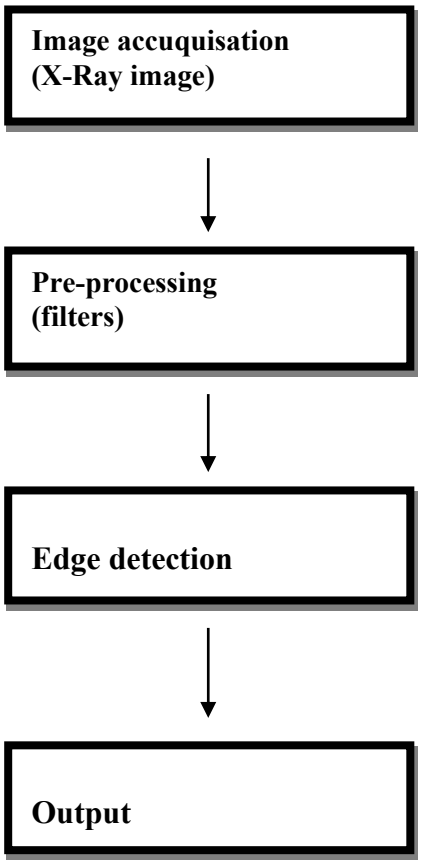


Figure 2

In the following section we discuss about the types of filters is to remove the noise from degraded image and types of edge detection function is used to detect edges, which are those places in an image that correspond to object boundaries.

TYPES OF FILTERS

Image filtering makes possible several useful tasks in image processing[1]. A filter can be applied to reduce the amount of unwanted noise in a particular image. Another type of filter can be used to reverse the effects of blurring on a particular picture. There are several types of filters exsist some of them are discussed below.

Mean filter:

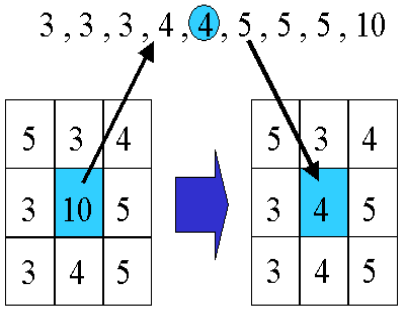
Mean filtering is a simple, intuitive and easy to implement method of smoothing images, i.e. reducing the amount of intensity distinction between one pixel and the next. It is often used to reduce noise in images[4].

1/9	1/9	1/9
1/9	1/9	1/9
1/9	1/9	1/9

Two main botheration in the mean filter is that a single pixel with a very unrepresentative value can significantly affect the mean value of all the pixels in its adjacency[7]. When the filter adjacency straddles an edge, the filter will interpolate new values for pixels on the edge and so will blur that edge. This may be a squeeze if sharp edges are required in the output.

Median filter:

Median filtering is to run through the signal entry by entry, redressing each entry with the median of neighboring entries. It is a nonlinear operation often used in image processing to reduce "salt and pepper" noise[2]. It is more effective than convolution when the goal is to synchronously reduce noise and preserve edges.



Weiner filter:

The Wiener filter is a filter used to produce an compute of a desired or destination random process by linear time-invariant (LTI) filtering of an observed noisy process, assuming know stationary signal and noise spectra, and additive noise[11]. The Wiener filter attenuates the mean square error between the estimated random process and the desired process[9]. The original image spectrum is guessed by taking the product of X(u,v) with the Wiener filter G (u,v):

$$\hat{S}(u,v) = G(u,v)X(u,v)$$

TYPES OF EDGE DETECTION

Edge detection is an image processing technique for detecting the boundaries of objects within images[12]. It works by detecting discontinuities in brightness. Edge detection is used for image segmentation and data extraction in areas such as image processing, computer vision, and machine vision. However, the quality of edge detection is highly dependent on lighting conditions, the presence of objects of similar intensities, density of edges in the scene and noise[8]. There are different algorithms for edge detections such as Canny, Laplacian of Gaussian(LOG), Sobel and Prewitt Edge Detection.

Sobel edge detection:

The Sobel operator, sometimes described as Sobel–Feldman operator or Sobel filter, is used in image processing and computer vision, particularly within edge detection algorithms where it creates an image emphasising edges[8].

Robert cross edge detection:

The Roberts Cross operator performs a light, rapidly compute, 2-D spatial gradient measurement on an image. It thus highlights regions of high spatial frequency which often correspond to edges[10]. In its most generic usage, the input to the operator is a grayscale image, as is the output. Pixel values at each and every point in the turn out narrate the enumerated absolute magnitude of the spatial gradient of the input image at that point[5].

Prewitt edge detection:

The Prewitt operator is used in image processing, peculiarly within edge detection algorithms. Technically, it is a discrete differentiation operator, computing an resemblance of the gradient of the image intensity function. At each and every point in the image, the conclusion of the Prewitt operator is either the computing gradient vector or the norm of this vector[10]. The Prewitt operator is depended on convolving the image with a small, separable, and integer valued filter in horizontal and vertical directions and is therefore relatively inexpensive in terms of computations like sobel and kayyal operators[4]. On the controversy, the gradient resemblance which it produces is relatively crude, in exclusive for high frequency variations in the image.

Laplacian of Gaussian(LOG):

The Laplacian is a 2-D isotropic estimate of the 2nd spatial derivative of an image. The Laplacian of an image high spots regions of rapid potency change and is on account of often used for edge detection (zero crossing edge detector)[9]. The Laplacian is often assigned to an image that has first been smoothed with something approximating a Gaussian smoothing filter in order to reduce its sensitivity to noise, and hence the two version will be described concurrently here. The operator normally takes a single gray level image as input and produces another gray level image as output[9].

Canny edge detection:

Canny edge detection is a technique to take out useful structural information from different vision objects and dramatically reduce the amount of data to be processed. It has been comprehensively engaged in miscellaneous computer vision strategy[5]. Canny has establish that the demand for the application of edge detection on diverse vision systems are relatively similar. Thus, an edge detection solution to dispatch

these requirements can be implemented in a wide range of situations[12]. The general paradigms for edge detection include Detection of edge with low error rate, which means that the detection should accurately catch as many edges. The edge point detected from the operator should accurately localize on the center of the edge. A given edge in the image should only be inscribed immediately, and where possible, image noise should not create false edges[3].

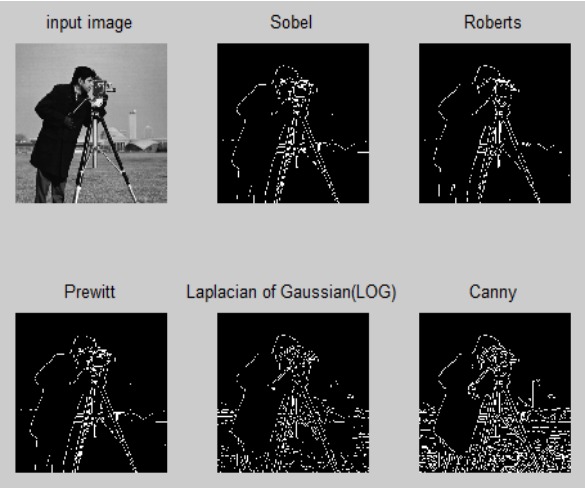


Figure 3

IV. CONCLUSION

So far we have discussed about the types of bone fracture theat commonly occur in human bones, steps involved to detect the bone fracture, types of filters and types of edge detection. For this work many bone fracture detection paper are studied. After reviewing all the bone fractured paper we concluded that the median filter is the best filter for removing salt and pepper noise and simultaneously preserves edge. We compared various types of edge detection methods such as sobel, Roberts, prewitt, laplacian of Gaussian(LOG) and canny. Among all canny edge detection is the best one widely used for bone detection because it traps the noise by creating false edge.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Segmentation of coronary artery using graph cut technique

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ABSTRACT

Accurate segmentation of coronary artery is very essential in order to find the depth of arterial disease. In this paper we propose an accurate automatic algorithm based on graph cut technique for the segmentation of coronary artery. To achieve the optimal segmentation vesselness measure, geodesic path and edge extraction technique are combined with graph cut technique.we evaluate the proposed method on the public images from coronary artery stenoses detection. The experimental results prove that segmentation results of the proposed method perform well with respect to centerline extraction and vessel border detection.

Keywords: segmentation, coronary artery, centerline, coronary angiography

I. INTRODUCTION

Automatic enhancement and perfect segmentation of coronary artery helps the doctors for more accurate and fast patient data analysis. Segmentation of coronary artery is one of the difficult tasks in image processing. Segmentation accuracy determines the eventual success or failure of computerized analysis procedure. For this reason considerable care should be taken to improve the probability of rugged segmentation. However accurate vessel segmentation is still challenging; highly reliable, fully automatic methods are not established till now.

In this paper we use graph cut technique to model vessel structure. To extract the centerline and vessel borders and to obtain minimum average segmentation error optimal thresholding technique is used. However the existing graph cut technique cannot be directly used for the segmentation of coronary arteries because it suffers from the following drawbacks:1)unable to segment tubular structure like blood vessels 2)cannot be applied directly on X-ray images because the X-ray images are characterized by low signal to noise ratio, poor vessel appearance, vessel bifurcation and variable image contrast.3)design of energy terms are not proper to assure optimal image analysis 4)original graph cut technique produces small contour corresponding to minimal cut.

We propose a novel graph cut technique to the vessel segmentation problem. The novel graph cut technique incorporates the following1) the local vessel appearance using vesselness measure 2) connectivity to other vessel structure using geodesic path and 3) edge extraction using canny edge detector for the accurate vessel boundary detection. Finally the proposed method is applied on the public images to evaluate the effectiveness of the algorithm.

II. BACKGROUND

In this section, we present the graph cut technique and the vesselness measure, which are used in our method.

A.Graph-Cuts:

Consider an arbitrary set of data elements (pixels) *P*

and some neighborhood system represented by a set N of all (unordered) pairs $\{p, q\}$ of neighboring elements in P. For example, P can contain pixels in a 2D (or 3D) grid and N can contain all unordered pairs of neighboring pixels under a standard 8 neighborhood system. Let $\boldsymbol{L} = (L1, \ldots, Lp, \ldots, L|P|)$ be a binary vector whose components Lp specify *assignments* to pixels p in P.Each Lp can be either "object" or "background". Vector $\boldsymbol{L}$ defines segmentation. Then, the soft constraints that we impose on boundary and region properties of $\boldsymbol{L}$ are described by the cost function

$C(\boldsymbol{L}) = \lambda \cdot R(\boldsymbol{L}) + B(\boldsymbol{L})$ Where

$R(\mathbf{L})=\Sigma\, Rp(Lp)$ *(regional term)* $B(\boldsymbol{L})=\Sigma B(p,q)$ $\delta(Lp, Lq)$ *(boundary term)* $\delta(Lp, Lq)=\{$ *1 if* $Lp = Lq$

0 otherwise

The coefficient $\lambda \geq 0$ in specifies a relative importance of the region properties term $R(A)$ versus the boundary properties term $B(\boldsymbol{L})$. The regional term $R(\boldsymbol{L})$ assumes that the individual penalties for assigning pixel p to "object" and "background", correspondingly Rp("obj") and Rp("bkg"), are given. For example, $Rp(\cdot)$ may reflect on how the intensity of pixel p fits into given intensity models (e.g. histograms) of the object and background.

B.Optimal solution using graph cut:

To segment a given image we create a graph $G =< V, E>$with nodes corresponding to pixels $p \in P$ of the image. There are two additional nodes: an "object" terminal (a source S) and a "background" terminal (a sink T). Therefore,

$V=P \cup \{S,T\}$ The set

of edges E consists of two types of undirected edges: *n-links* (neighborhood links) and *t-links* (terminal links). Each pixel p has two t-links $\{p, S\}$and $\{p, T\}$ connecting it to each terminal. Each pair of neighboring pixels $\{p, q\}$ in N is connected by an n-link. Without any ambiguity, an n-link connecting a pair of neighbors p and q is also denoted by $\{p, q\}$.Therefore,

$E =N \cup \{\{P,S\},\{P.T\}\}$

The following tables gives weights of edges in E.

Table 1

Graph arc	Cost
(p,q)	$B(p,q)$ *for* $(p,q) \in N$
(s,p)	λ *Rp(background) for* $p \in I, P \in (o \cup B)$ K *for* $p \in o$ *0 for* $p \in B$
(p,t)	λ *Rp (object) for* $p \in I, P \in (o \cup B)$ *0 for* $p \in o$ K *for* $p \in B$

III. PROPOSED METHOD

In this section, we present a fully automatic method for vessel segmentation method for vessel segmentation based on graph theory.

A. Seed selection technique:

In order to extract the foreground object (vessel) from background region we want to accurately choose the threshold value.

1. Sketch the histogram of the given image and choose the threshold value in the deep valley region.
2. Segment the given image using threshold value which is obtained in step1.This will produce two group of pixels with gray level values >T and G2 consisting of pixels with values <T.
3. Compute the average intensity values μ1 and μ2 for the pixels in regions G1 and G2.
4. Compute a new threshold value using the formula T=O.5(μ1+μ2).
5. Repeat steps 2 through steps 4 until the difference in T in successive iterations is smaller than a predefined a predefined parameter T.

B. Geodesic distance map:

In order to find the connectivity between various vessel regions we use the concept of geodesic distance map. Geodesic distance is nothing but the shortest distance between the two pixels. From the set of all possible path between the two pixels, we select one pixel with minimum distance. The path is computed using Dijkstra shortest path algorithm. we compute the geodesic distance map D and assign the cost to each path. Finally we choose the path having the least cost. The path having the least cost is called as object pixel(vessel regions) and the path having the highest cost(non vessel region) is called as background pixel.

C. Boundary detection

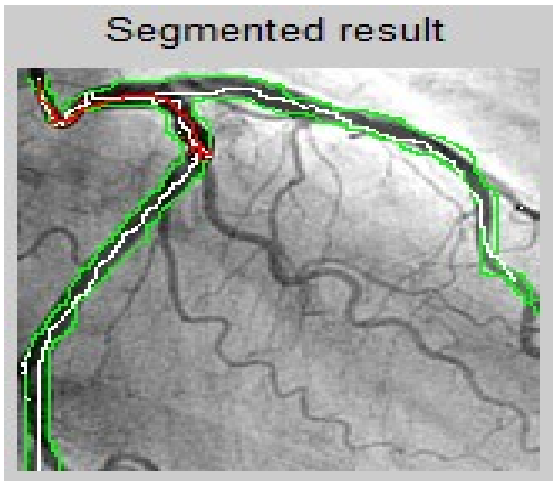
Edge is nothing but the boundary between the two regions of an image with relatively distinct gray level properties. Edge is also defined as set of connected pixels that lies on the boundary between two regions of an image. Edge normally contains more valuable boundary information. In this paper we use canny edge detection algorithm for detecting the edges.

D. Graph cut segmentation:

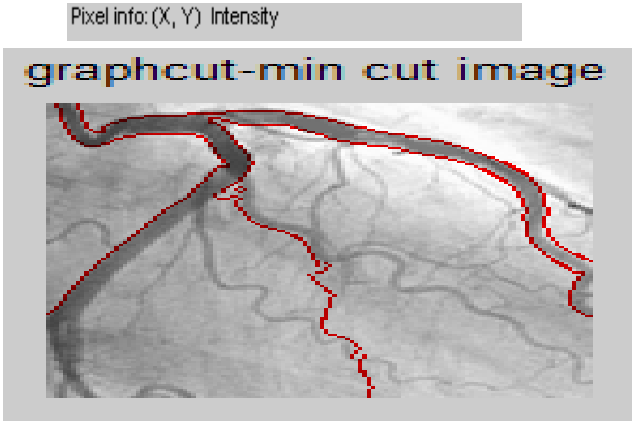
Finally we apply the proposed graph cut algorithm on the boundary detected image .Then, once we obtain the segmentation from graph cut technique, we keep only the biggest connected component in the final segmentation. An example of final segmentation is shown in the figure given below.

IV. EXPERIMENTAL RESULTS

For our experiment we have chosen Matlab. Then we applied our proposed algorithm on the coronar artery image. Following are the series of images from that results from our experiment.



Vessels & background extraction



geodesic distance map

V. CONCLUSION

In this paper we propose a novel approach for coronary artery segmentation using graph cut technique. The proposed approach produces a very effective result of coronary artery segmentation. In our future research we deal with irregularity at bifurcation and crossings and try to use a supervised method to optimize the threshold value and a method to segment overlapped arteries based on contrast liquid opacity.

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National Conference on 'Innovative Research on Robotics, Circuits and Technology' (IRCT 2018)
Organized By : CIrcuit Branches of SCSVMV, (EEE, ECE, EIE & Mechatronics) , Kanchipuram, Tamil Nadu, India
In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Analysis Prefetching Mechanism for VM Snapshot Deduplication Metadata in Cloud Storage

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ABSTRACT

Cloud computing enables hardware and software resources to be accessed over the Internet. IaaS is one of the cloud services which offers computing power on demand by providing virtual machines to the consumers. As the number of users increase, IaaS cloud generates more number of VM images and snapshots. Hence, it is necessary to optimally utilize the storage space of IaaS to improve the performance. A well-known deduplication technique is used for efficient utilization of storage space. Since, the metadata generated is huge with the deduplication technique, it can only be maintained in the hard disk. Hence, prefetching a suitable subset of metadata is essential to improve I/O throughput. Thus, the objective of this paper is to compare the effectiveness of the similarity and locality indexing mechanisms with a common set of performance metrics to suggest a better indexing mechanism for IaaS cloud.

Keywords: Cloud storage, Deduplication, Storage optimization, Prefetching, Indexing mechanisms

I. INTRODUCTION

Cloud computing is a model that enables the consumers to access a shared pool of configurable computing resources over the Internet. It has several advantages that includes high availability, reliability, ease of management, disaster recovery and flexibility. Infrastructure as a Service (IaaS) is one of the cloud services that provides virtualized computing resources for the consumers to utilize. Due to the advantages of cloud computing, the adoption rate of IaaS consumers increases largely [15]. It has resulted in explosion of the number of virtual machine (VM) images and snapshots. While VM images create virtual machines, their corresponding VM snapshots preserve the state and data at a specific point in time. There may be different VM images related to different operating systems utilized by the consumers. Similarly, there may be several VM snapshots representing different states of virtual machines. As these VM images and VM snapshots are larger in size varying from several MBs to GBs, they occupy considerable amount of storage space.

In order to effectively utilize the storage space, it is necessary to identify and eliminate the redundant data among the various VM snapshots. A well-known optimization technique, namely, deduplication is helpful in eliminating the redundant data. It attempts to store only one instance of the data in the storage. The redundant data is substituted with a reference to the existing one in the storage. Though this technique saves storage space, the associated metadata overhead is huge. The metadata includes *Fingerprint Index* and *File Recipe* which are utilized to detect duplicates and to retrieve the files respectively. As this metadata is huge, it is typically saved in the hard disk. However, the challenge with inline deduplication of VM snapshot is to reduce the high latency due to the cost involved in accessing the metadata from the hard

disk. There are several indexing mechanisms that are available to prefetch a set of metadata entries into the RAM.Consequently, it becomes important to identify a better suited indexing mechanism for VM snapshot deduplication. Currently, these mechanisms have been analyzed individually by utilizing the performance metrics, namely, deduplication throughput and efficiency. However, the effectiveness of the prefetched set of metadata entries can be well estimated by the amount of space utilized in RAM and time taken to detect duplicates. Hence, the objective of this paper is to analyze the performance of the similarity and locality indexing mechanisms using a common set of evaluation metrics, namely, RAM footprint, duplicate detection time, deduplication throughput and space savings.

A. Contributions

The main contribution of this paper is to analyze the performance of similarity and locality indexing mechanisms for VM snapshot deduplication and to suggest a better suited indexing mechanism for IaaS cloud.

B. Paper Organization

The remainder of this paper is organized as follows. Section 2 reviews the related works in applying deduplication for VM snapshots. Section 3 describes the design of the performance evaluation system. Section 4 deals with the system implementation and Section 5 deals with the detailed performance analysis. Section 6 concludes the paper.

II. RELATED WORKS

Many research works have been proposed for prefetching the metadata into the RAM [7-13], as it is an important and challenging task in deduplication.

The pattern of the VM images is analyzed in the following two works. Jin et al. [6] have studied both the inter and intra similarity of various VM images. It is found from the experimental results that the VM images of same operating system or the versions of operating system are considered to have more duplicate blocks than the VM images of different operating system. Jayaram et al. [5] have performed an empirical analysis on 525 VM images of a public cloud storage. Both fixed and variable size chunking of various block sizes (4 KB, 8 KB, 16 KB, 32 KB and 64 KB) are applied on the VM images and it is seen that both the chunking mechanisms yield the same deduplication ratio. If the inter similarity among VM images is higher, more number of duplicates can be expected.

The Three Level Index (3LI) [1] is used to prefetch a suitable subset of fingerprints based upon the prefix from the disk. The fingerprints are organized in the hard disk in the form of several Hash node Tables (HTs). Each HT consists of fingerprint entries based on a certain prefix. The prefix of the fingerprint can be obtained by a 3LI which is maintained in the RAM. During the write operation, first, second and third 8 bits of any incoming fingerprint is compared against the entries present in the first, second and third level indices respectively using a comparator. If the prefixes are found, subset level will be checked. Otherwise, the new value is updated in the index. If the first 24 bit entry of the fingerprint matches in the 3LI, the corresponding HT is prefetched from the disk to RAM to detect duplicates. The motivation behind the 3LI is not clear.

In Two Level Index [2], the existing VM snapshots available in the disk are partitioned into 128 MB block groups. The groups are further divided into 4 KB blocks. The $(n+k)$ bit prefix fingerprint entries corresponding to every block in a block group and the block address where the fingerprint resides are maintained in 2LI. At first level, the first n bit of the fingerprint and a pointer to the second level is stored. Subsequently, the second level consists of the next k bits and the location of the block group. During the read of VM snapshots, every $(n+k)$ bit prefix of fingerprint is compared against the 2LI. If the $(n+k)$

bit prefix matches the 2LI, the block groups which have this fingerprint are prefetched into the RAM. These prefetched block groups help in identifying the future fingerprints. This speeds up the lookup process of VM snapshots. The 2LI prefetches more than one group based on the locality.

III. SYSTEM DESIGN

When deduplication is adopted in the cloud storage, it incurs the overhead of maintaining metadata, namely, *Fingerprint Index* and *File Recipe*. Since this metadata is huge, it is typically maintained in the disk. However, it increases the cost of finding the duplicates as it involves many disk seeks. Thus, a suitable indexing mechanism to prefetch the most relevant set of fingerprints is required to reduce the write latency for VM snapshots. Hence, the proposed Performance Evaluation System (PES) compares two existing indexing mechanisms to find a suitable one for VM snapshot deduplication. The PES consists of chunker, similarity detector, locality detector and the prefetcher as shown in Figure 1.

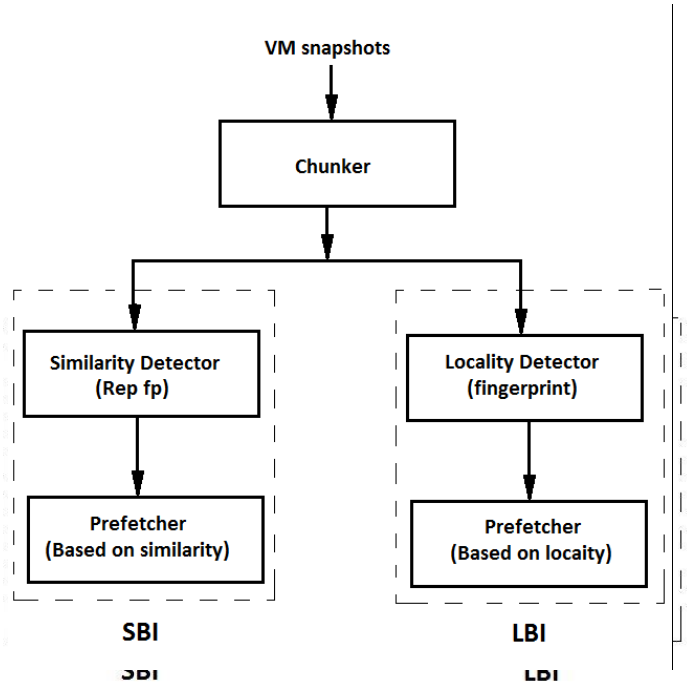

Figure 1. Design of PES

C. Chunker

The chunker divides every incoming VM snapshot into a set of fixed or variable sized blocks. Further, a cryptographic hash algorithm, namely, SHA1 is used to generate fingerprints corresponding to these blocks. These fingerprints are the unique identifiers for those corresponding blocks.

D. Similarity Based Index

The *Similarity Detector* utilizes Similarity Based Index (SBI) [3] to prefetch the fingerprints based on the similarity of files. Every incoming VM snapshot is divided into the variable sized blocks by using the variable-size chunking mechanism. Subsequently, the fingerprints are found for those blocks and the representative fingerprint is found. The representative fingerprint is the minimum fingerprint in a set of fingerprints corresponding to that VM snapshot. According to Broder's theorem, if the minimum fingerprints of two files are equal, the contents of two files are said to be similar up to 80%. The SBI consists of two levels as shown in Figure 2. For every VM snapshot, the first level consists of the fingerprint corresponding to the whole VM snapshot, the representative fingerprint and a pointer to the second level index for every VM snapshot. This representative fingerprint is helpful in finding the similar VM snapshots. The second level consists of the fingerprints corresponding to the similar VM snapshots.

During write operation, the *Similarity Detector* finds the fingerprint for the entire incoming VM snapshot. If a match is found, then the snapshot is found to be a duplicate. Otherwise, the snapshot is divided into a set of variable sized blocks. Further, the representative fingerprint of an incoming VM snapshot is compared against the first level. If it matches, then the incoming VM snapshot is similar. Hence, the fingerprints of VM snapshot are compared against the second level. Further, if the fingerprints are present in the second level index, then the

reference counts are updated. Otherwise, the entries are inserted into the second level index.

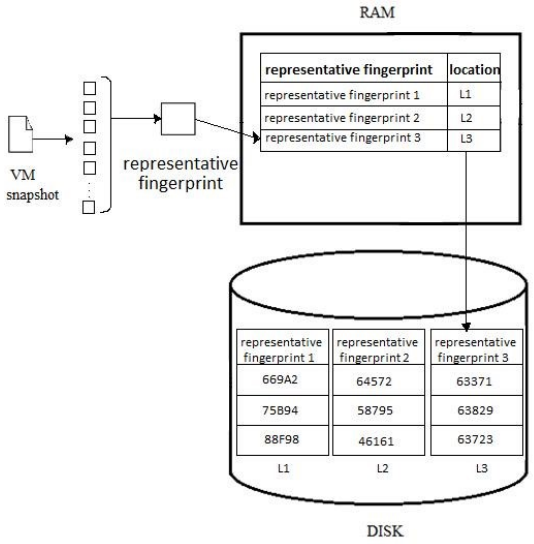

Figure 2. Similarity Based Index

E. Locality Based Index

In Locality Based Index (LBI) [4], every incoming VM snapshot is divided into a set of variable sized blocks. The fingerprints of these blocks are saved in the same order of arrival in the *fpstore* as shown in Figure 3. The *fpstore* and the blocks are maintained in a *container*. During the read operation of VM snapshots, when a fingerprint is matched in the *fpstore* of a *container*, the entire *fpstore* of the *container* is prefetched from the disk to RAM to match the future fingerprints by using Locality *detector*.

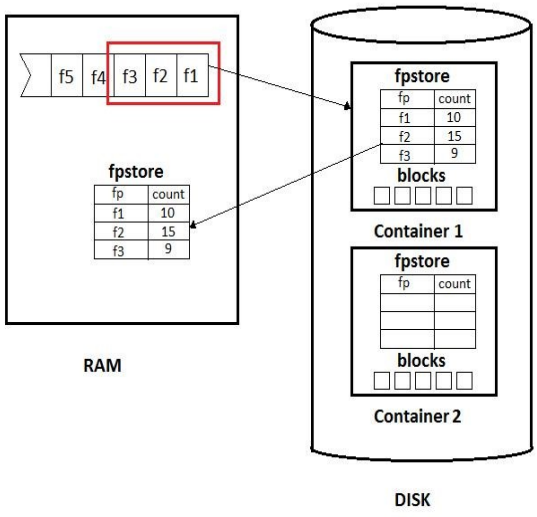

Figure 3. Locality Based Index

IV. SYSTEM IMPLEMENTATION

This section discusses the implementation and dataset used to construct SBI and LBI.

F. Implementation

The experimentation of the PES is performed on Intel Core i7 2.93 GHz machine with 8 GB RAM on Cent 64-bit operating system. To improve the precision of PES evaluation, each test is run three times under the same experimental settings.

In SBI, the fingerprint of the entire VM snapshot, representa -tive fingerprint and the location of the second level index are maintained as an in-memory *HashMap*. The representative fingerprint of the incoming VM snapshots is found and checked against the first in-memory *HashMap* table using *containsKey()* method of *HashMap* class. If a match is found, then the entire set of fingerprints corresponding to the incoming VM snapshot are compared against the second level in-memory *HashMap* table using *containsKey()* method of *HashMap* class.

In LBI, the fingerprints of every incoming VM snapshot are placed in a text file by processing according to the order of arrival. The text file represents the *fpstore*. Further, the text file and the corresponding blocks are stored in a folder which represents the *container*. When an initial fingerprint of the incoming VM snapshot matches the first fingerprint of the *container*, then the *fpstore* of the corresponding *container* is prefetched into the RAM. The fingerprints of the incoming VM snapshot are compared against the prefetched fingerprints using *containsKey()* method of *HashMap* class for deduplication. If a match is not found, then the fingerprints of the incoming snapshot are saved into a new *container*.

G. Dataset

The dataset for PES is a set of VM snapshots collected

from VMware cloud data center [14] as shown in Table 1. This dataset consists of VM snapshots of most popular operating systems, namely, Debian, Fedora, Mint, OpenSUSE and Ubuntu. This dataset is utilized for analyzing the performance of both indexing mechanisms.

Table 1. VM snapshots dataset

OS Type	No. of Snap-shots	Size (in MB)
Debian	10	28.25
Fedora	30	84.9
Mint	20	48.5
OpenSUSE	15	54.25
Ubuntu	50	86.1
Total	125	302.25

V. RESULTS AND DISCUSSION

This section deals with the detailed performance analysis of SBI and LBI mechanisms by utilizing a common set of evaluation metrics.

H. Metrics for evaluvation

The indexing mechanisms, namely, SBI and LBI have been compared using a set of common metrics, namely, RAM footprint, duplicate detection time, space savings and deduplication throughput.

1) **RAM footprint**

The fingerprints prefetched from the disk utilize a considerable amount of RAM memory during deduplication. The performance of a system depends on the utilization of the RAM memory.

2) **Duplicate detection time**

During write operation, the fingerprints of every incoming VM snapshot are compared with the prefetched fingerprints in order to find duplicates. The time taken to perform this operation is the duplicate detection time. The lower the duplicate detection time is, the higher will be the performance of the indexing mechanism

3) **Space savings**

Space savings refers to the amount of disk space saved after the application of deduplication. It is measured by the difference in the size of the snapshot before and after deduplication. The space saving depends on the prefetched subset of fingerprints.

4) **Deduplication throughput**

Deduplication throughput is found to evaluate the effectiveness of the indexing mechanisms. It represents the number of blocks written into the disk per unit time. The higher the deduplication throughput is, the higher will be the performance of the indexing mechanism.

I. *Analysis of PES*

The dataset has been split into two parts, namely, index building dataset and a deduplicating dataset. The index building dataset consists of 30 VM snapshots of size 50 MB. The average size of a VM snapshot is 10 MB. The deduplicating dataset consists of 20 VM snapshots of size 25 MB. Experiments have been conducted to build the indices SBI and LBI by utilizing the index building dataset. Further, the deduplicating dataset has been given as input to analyze the performance of the indexing mechanism.

1) **Comparison of indexing schemes for RAM footprint**

The fingerprints prefetched from disk are maintained at in-memory *HashMap* table. The RAM utilization is found by using Runtime class in Java library.

Figure 4. Average RAM footprint

While LBI prefetches the fingerprints of a single *container*, SBI prefetches the fingerprints of all similar VM snapshots. Hence, the average RAM footprint of the LBI is less when compared to that of SBI as shown in Figure 4.

2) **Comparison of indexing schemes for duplicate detection time**

A Timer *startTimer* is started immediately after chunking the snapshots into blocks by using chunker and *endTimer* is stopped immediately after duplicate detection using *check(fingerprint)*. The difference between the *startTimer* and *endTimer* gives the duplicate detection time in millisecond by using *System.currentTimeMillis()* of Java library. In order to improve the accuracy, it is also measured in nanosecond, *startNanoTimer* and *endNanoTimer* is calculated by using *System.nanoTime()* and *System.currentTimeMillis()* method of Java library.

Since the considered workload for deduplication is characterized by the VM snapshot corresponding to Linux distribution, the inter-similarity was more. Hence, the probability of the fingerprints of incoming VM snapshots to get matched with entries in the SBI is more when compared to LBI as shown in Figure 5.

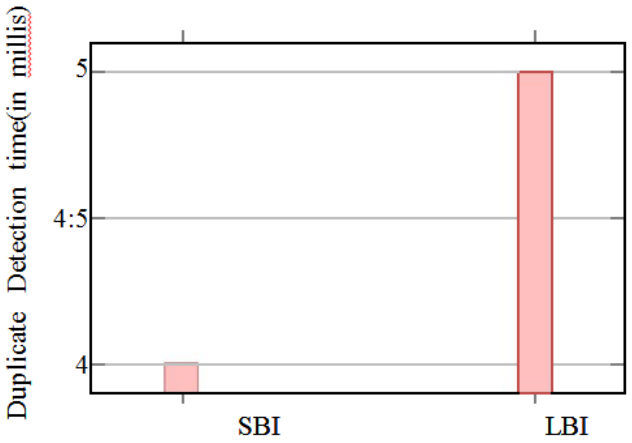

Figure 5. Average duplicate detection time

3) **Comparison of indexing schemes for space savings**

Space savings signifies the amount of storage space used by the snapshot by utilizing the index. The size of the directory is measured by using *FileUtils.sizeOfDirectory()*. The files used for deduplication is saved in *filesUsed* directory and the files are chunked and saved into the *chunkDirectory*. The difference between the *filesUsed* and *chunkDirectory* returns the space saving. The number of duplicates detected for SBI is more when compared to LBI. Hence, the average space savings of SBI is higher than LBI as shown in Figure 6.

4) **Comparison of indexing schemes for deduplication throughput**

The throughput is measured in terms of number of blocks written per second by using *DIRECTORYNAME.length()*. The throughput has been found by using sample dataset as shown in Table 1.

The number of fingerprints prefetched from the disk is maintained as in memory *HashMap* table. The SBI prefetches the fingerprints based on the similar VM snapshots, whereas LBI prefetches the fingerprints corresponding to a particular snapshot. Due to the higher inter similarity between the snapshots, the SBI prefetches more number of blocks when compared with LBI. Hence, the number of blocks prefetched from the disk is higher for SBI when compared to

LBI. The throughput analysis of the indexing mechanism is shown in Figure 7.

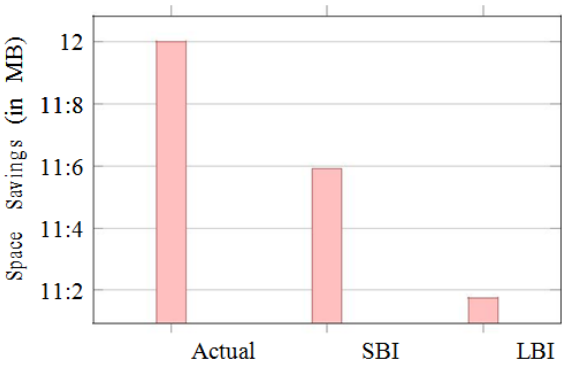

Figure 6. Average space savings

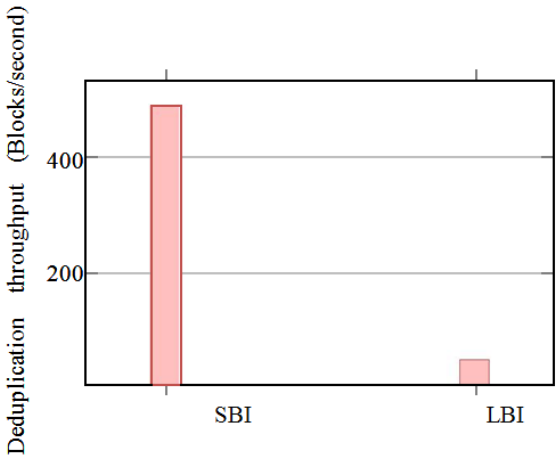

Figure 7. Average deduplication throughput

VI. CONCLUSION

The existing indexing mechanisms, SBI and LBI have been implemented. The index building dataset of size 50 MB has been utilized to build the indices. Further, the deduplicating dataset of size 25 MB has been given as the input to perform deduplication. During deduplication, the average RAM footprint consumed, the time involved for detecting duplicates, space occupied for storing the deduplicating dataset and the numbers of blocks written per second for each indexing mechanism have been found. From the experimental investigation, it is found that the RAM footprint, duplicate detection time and the throughput of SBI are 15%, 20% and 90% more and space savings is 5% less when compared to that of LBI.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Embedded System Design Processor using GAA

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ABSTRACT

Electronics system design is the evolutionary task which is concentrating on the system design for various things like processor, SoC for real time system, embedded systems, reconfigurable system design and more where the Processor design is one of them; it may be a single core, or more than one cores depends on the requirement Specification. There are various hardware description languages used to design and fabricate the processor, among them Verilog, VHDL, SystemVerilog and Bluespec System Verilog are few of them. Bluespec is the one of the modern hardware synthesizable language with guarded atomic action(GAA), which has many advantages over the others. This paper presents the design and implementation of pipeline based 64-bit processor using bluespec, also presents the analysis of number of clock cycles per instructions, implementation of RISC V instruction sets and working principle of pipeline processor using bluespec.

Keywords: Processor, Hardware Description Language, bluespec, Pipeline, Register Files, RISC V, Instruction Set Architecture.

I. INTRODUCTION

Digital electronics circuits design is ever increasing field in all the technology. In that Integrated Design(IC) design is the one of the important and challenging task in the electronics field. The IC's can be used in many areas like Digital signal processing, computer architecture system, SoC, embedded systems and robotics architecture etc. An important task of computer architecture is the design of the instruction sets for the processor [4]. Processor design is the complex task involving in most of the modern hardware designer. There are two general types of instruction set architecture for processor design perspectives; one is CISC and another is RISC, each one has its own advantages and disadvantages. CISC has more number of instruction sets, slower clock speed, little general purpose register, more addressing modes and others[2][4]. In today's technology RISC processors are playing important role, because of simple and reduced instruction sets, shorten the execution time by reducing the clock cycle per instructions, it can address enormous amount of memory and more general purpose register in term of register files[2].

There are number of tools and board could be used to design a chip. FPGA-Field Programmable Gate Array is widely used to design the IC's in an easy ways of prototyping and verifying the functional design without fabrication [3]. It supports large number of gates which are easily inheritable and also can be used to solve complex hardware design with respect to the chip dimensions and register level transfer[3][4].

The older versions of hardware description languages such as Verilog, VHDL and SystemVerilog are few of them. These hardware description languages are having many advantages and disadvantages over the others, but in some point it may not support. Atomic transaction is the core of the hardware design technology because the hardware components should always work concurrently; Bluespec[1] is the only language support Atomic transactions [1],[6] in much

more. Processor design using the language like Verilog, SystemVerilog, and VHDL may have less flexibility in all aspects for example register files, loading instructions, pipeline concept implementation and many more. But in Bluespec, including the above mentioned and Atomic Transactions Control-Adaptive Parameterization Modern, High-Level Language Facilities, Mainstream Technologies are the key advantages [1][5][6].

Pipeline processor design is another new trend to design processor in such a way that to increases the throughput and efficient handling of data, instructions. These features could be implemented efficiently using bluespec[5],[6].

The proposed work has the following module; 1). Test Bench, 2). Load the instructions in to register files, 3). Perform all operations through pipeline concepts, 4). Write the result into data register files. The working principles will be explained in the later chapters.

II. RELATED WORKS

In [7] Rakesh M.R has implemented 9 bit RISC processor using pipeline concepts with various blocks including fetch, decode, execute and store the data. He used separate data and instruction memory. He used Verilog and Modelsim for programming and simulation respectively. The advantages of this method are to execute one instruction cycle for 4 stage pipeline.

In [8] Navneet kaur et al, they proposed 64 bit RISC processor desing using VHDL. VHDL programming language is used to develop the RISC in Xilinx 14.2 ISE design suit and functionality simulated on Modelsim 10.1 b simulator. They tested 33 instructions are functionally verified. In device utilization report the number of slices are 34%, Number of Slice Flip Flops 3%, Number of 4 input LUTs 24%, minimum period is found 1.862ns, maximum frequency 539.913MHz, minimum input arrival time before 111.930ns, maximum output required time after clock 9.408ns and it uses 64 bit for both data bus and address bus. it achieves optimized result.

In [9] Imran Mohammad et al had given a proposal to implement 64-bit RISC processor design and verified with Xilinx simulator. It also presents architecture, data path, and instruction sets of the RISC processor. It can address up to 16 Exabyte's. They declared that it can be used in many applications like robotics workshop, gaming kits and ATMs.
They tested with 33 instructions and could be implemented for more number of instructions for future works.

In [10] P. Devi Pradeep proposed 64 bit RISC processor design for industry automation and tested with BUT-Built under test. They used collection of registers, instruction commands, 64 bit data and address bus to handle data and addresses. They used Verilog HDL simulator to implement this processor and it capable of perform JUMP, SKIP and HALT instructions. It consumed 18080.18uw.

In [11] Nirav Dave proposed a designing a reorder buffer using bluespec. it synthesized high level description in the form of guarded atomic actions GAA into high quality structural RTL. This paper explores the design of reorder buffer for an out-of – order super scalar processor with MIPS I ISA.

III. BLUSEPC AT A GLANCE

Bluespec is the highly level abstract and Object oriented Hardware Description Language which is compiled in to RTL. It has package, modules, rules, states and interfaces. Module is actual unit which gets compiles in to hardware; each module roughly corresponds to a verilog module. Module consists of three things; stages, rules which modify the state, and interface which allow the communication and interact with module [11],[1].

a). Bluespec Syntax

Bluespec has it own syntax; for example module, rules,registers could be used to represents circuits in Bluespec. it wraps around an actual verilog module or a standard module with state elements including other module, rule and interfaces[11],[1]. All the state elements such as registers, flip flop, clocks, memories and others are included in the module. The behaviours can be represented in the form of rules which consists of change of state on the hardware state of the module action and condition required for the rule to be a valid one[11],[1]. The interfaces could be used to communicate with outside world to intereact between modules. Each inteface has guard which restricts when should the method may be called and what should not be called. This method may be any kind of operation like read, write or both. There are three kind of methods[12],[1] they are Value, Action and ActionValue; Value which is return a value to the caller, and have no actions that is when these methods are called, there is no change of state, no side-effect. Action which cause actions that is state changes to occur. ActionValue couples action and Value methods , causing an action to occur and they return a value to the caller[12].

```
Package pack1
        // import sytatemtns
        Import package2……
        Module mkTb(interfacename)
           Rule rule1( conditions)
                rule implementations…
           Endule
           Rule rule2( conditions)
                Rule implementation……..
           Endule
             …….
          Method implementation here
          ……
        Endmodule
EndPackage

Package pack2
        // import sytatemtns
        ……
        Module mkTb(interfacename)
           Rule rule1( conditions)
                ……..
           Endule
           Rule rule2( conditions)
                ……
           Endule
             …….
          Method implementation here
          ……
        Endmodule
EndPackage
```

b).Guarded Atomic Transactionsin Bluespec

Hardware should work high efficiency in atomic or independent, an atomic transaction is the core of the hardware design technology. Atomic transactions simplify complex concurrency, improve the communication between modules, and elevate the description and synthesis of system, control [12]. Bluespec[12][1] is the only technology providing such a solution and also it provide hardware modeling, verification and rapid prototype design[13].

The bluespec also has concurrent rule execution and scheduling rules into clocks [13]. To get maximum performance of any operations using bluespec, we might use to execute many rules as possible concurrently [12]. In BSV, we abstract out the hardware-specific constraints into a simple semantic model of scheduling constraints on pairs of methods.

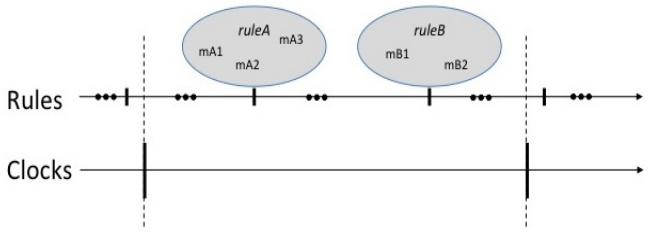

Figure 1. Two atomic rules in a clock, and their methods

The above image shows, how more than one rules executing from many methods concurrently that means many rules running within a single clock [13].

IV. RISC V INSTRUCTIONS

The following are the RISC V instructions and its binary code for processor developments [15].

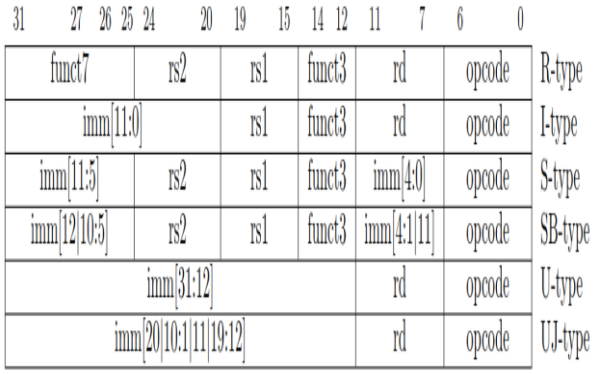

Figure 2. RISC V instruction types [15]

In this work we have used the following instructions for implementation of the pipeline processors [15].

Instructions	Opcode(7)
JAL rd,imm	1101111
LW d,rs1,imm	0000011
SWrs1,rs2,imm	0100011
ADDI rd,rs1,imm	0010011
SLTI rd,rs1,imm	0010011
XORI rd,rs1,imm	0010011
ORI rd,rs1,imm	0010011
ANDI rd,rs1,imm	0010011
SLLI rd,rs1,shamt	0010011
ADD rd,rs1,rs2	0110011
SUB rd,rs1,rs2	0110011
SLL rd,rs1,rs2	0110011
SLT rd,rs1,rs2	0110011
XOR rd,rs1,rs2	0110011
OR rd,rs1,rs2	0110011
AND rd,rs1,rs2	0110011
SD rs1,rs2,imm	0110011
MUL rd,rs1,rs2	0110011
DIV rd,rs1,rs2	0110011

Figure 3. RISC V instruction equivalent codes

DESING AND IMPLEMENTATION OF PIPELINE PROCESSIR

a).Pipeline Processor Architecture

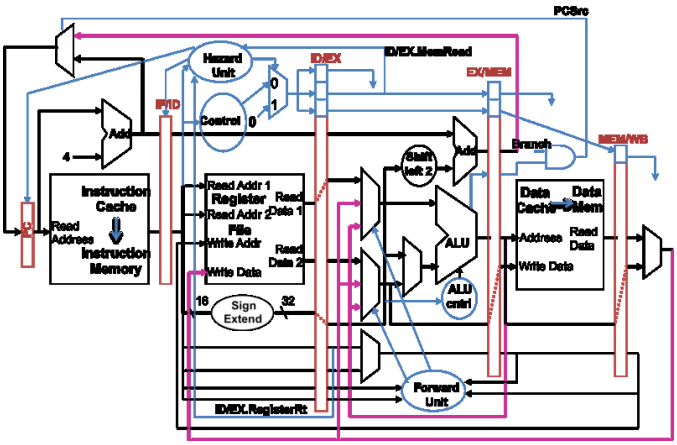

Figure 4. Five stage pipeline Architecture [14]

b). Implementation steps

The proposed method consists of the following components

- Test bench
- Main package
- parameter declarations
- Instructions format
- Instructions implementations

Test bench could be used to provide instructions to the main package through rule which will run atomic transactions and passing instruction to the main package. The main package having method to implement load instructions, return result to test bench and halt the operations. Pipeline could be implemented in this package having many rules running concurrently by passing parameters to each instruction. All instructions should pass through into all the stages in the pipeline. The rules can be used to implement pipelines using FIFO concepts [11], [13]. Fig 5 shows the instruction to be passed from instruction test bench to main processing units. This

shows the format in which the input are provided to the main function, this could be designed in instruction format unit having syntax as follows.

```
Instruction ins_code [4] =
{
        tagged LW  {    rd:R0,  rt:R0,  im:01 },
        tagged ADD {    rd:R2,  rt:R0,  rs:R1   },
        tagged SW  {    im5:0,  rt:R2,  rs:R0,im7:00 },
        tagged SUB {    rd:R5,   rt:R0,  rs:R1  },
        tagged JAL {    rd:R3,  jtgt:01}
}
```

Figure 5. Instructions given through test bench

The above Figure 5 shows the arithmetic units having definition of each instruction to be stored. Here we used enum[13],[12] keyword to design instructions for example from the above diagram we can represent binary value for ADD is 00000, SUB is 00001, SLL is 00010 etc.. These values can be used when we are going to decode the instructions.

```
//Arithmetic instructions
typedef enum {
        ADD,SUB,SLL,SLT,SLTU,XOR,
        SRL,SRA,OR,AND,MUL,MULH,
        MULHSU,MULHU,DIV,DIVU,REM,
        REMU,LUI,AUIPC,
        ADDI,SLTI,SLTIU,
        XORI,ORI,ANDI,
        SLLI,SRLI,SRAI
   } ALU_op deriving(Eq,Bits,FShow);
```

Figure 6. Arithmetic instructions type definition

Figure 6. shows the parameter declarations section which is used to declare all the parameter used for the entire pipeline processor design for example data length, address length in terms of bits. This file could be imported wherever we need it.

```
`define ENTRY_ROB_SIZE 16
`define ENTRY_ROB_INDEX_SIZE 4
`define IQ_SIZE 8
`define TOTAL_THREADS 4
`define REG_WIDTH 64
`define SIMD_REG_WIDTH 256
`define PRF_SIZE 64
`define FETCH_WIDTH 2
`define ISSUE_WIDTH 4
`define MEMQ_SIZE 16
`define DCACHE_SIZE 4294967296
`define ICACHE_SIZE 4294967296
`define IMM_BUF_SIZE 8
```

Figure 7. Predefined variables

Instruction decode stage will decode the instructions which is after reading instruction from the FIFO line based on the instruction you are passed from test bench. It will read the instruction, extract the bits, assign into the variables and return the result into the main FIFO stage, and then this could be used for input to the next stage through FIFO. For example the pseudo code used in the FIFO pipeline stage is shown.

```
Rule fetch_stage (condition)
        FIFO.first
        Call fetchinstruction
        FIFO1.enq(fetched_instructions)
endrule
 Rule Decode_stage (condition)
        FIFO1.first
        Call decode(fetched_instruction)
        FIFO2.enq(decoded_instructions)
endrule
Rule MemoryAccess_stage (condition)
        FIFO2.first
        Call
MemoryAddress_calculation(decoded_instru
ction)
        FIFO3.enq(calculated_address)
endrule
Rule execute_stage (condition)
        FIFO3.first
        Call Execute (calculated_address)
        FIFO4.enq (executed_value)
Endrule

Rule execute_stage (condition)
        FIFO4.first
        Call write_back(executed_value)
Endrule
```

b). Pipeline Processor desing and its Stages

In the proposed method have five stages of pipeline [13]; these are Fetch the instruction (IF), Decode the instructions (ID), execute stage (EX), memory acces stage (MEM), write back (WB). The five stage pipeline can be implemented in main package. It has

many rules and each rule is to perform certain task. Here there are five stages of operations were implemented using FIFO concepts.

Figure 4 show the five stage processor design which is having program counter to count the number of instruction to be performed, clock register is used to count the number of clock pulse is needed to complete in one stage. Each pipeline stage has its own register to store the intermediate result after each stage to be executed. For example IF register can be used to store the fetched instruction to be stored, ID is used for decoded instruction to be stored, MEM this register can be used to store the calculated address, EX register can be used to store the executed result to be stored and finally WB register can be used to store write the result in to registers.

c). Execution and Simulation result

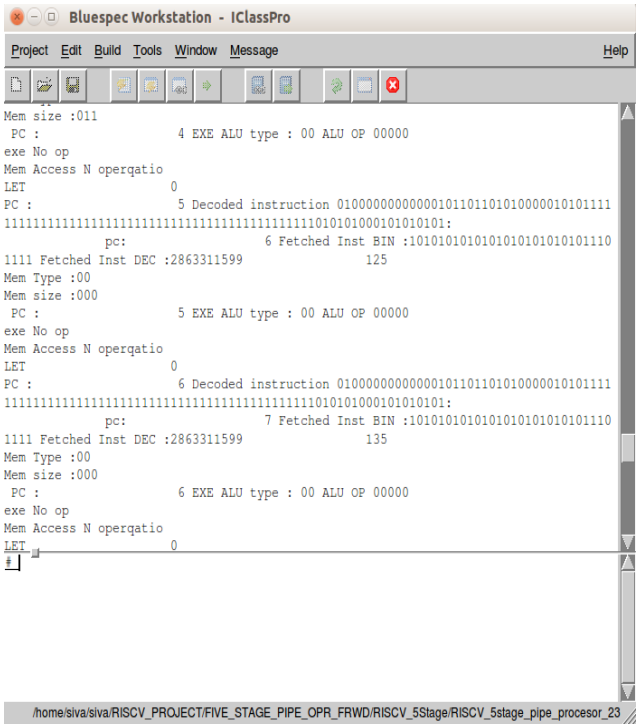

Figure 8. Execution result

Simulation Results

The following section discuss about the analysis of pipeline processor execution result in terms of time taken to load instruction in to the register file, time taken from the register file to fetch stage, time taken to decode the each instruction, execution time of each instruction and write back time. From the table 1. We can understand that the loading instruction in to the register files will take 15 ms for every instruction and for other operation like fetch, decode execute will take incrementally 15 ms, but for execute to write back instruction will take some different time variations, why because there may be falling in bubbles in between the these instructions. The bubbling time can be reduced through some different way. Through the guarded atomic transactions we could able to reduce the bubbling in the pipeline stages. If we increase the no of stages will lead the increase the throughput. But for some instruction like JUMP, HALT etc will not require execute time so there is bubble formed the subsequent instruction to be executed.

Table 1. instruction running time in five stages

Instructions	Running time for instructions in Bluespec(ms)				
	Load into memory	Fetch Stage	Decode	Execute	Write back
LW	15	145	155	165	175
LW	25	155	165	175	195
ADD	35	165	185	195	215
LW	45	185	205	215	235
LW	55	205	225	235	255
ADD	65	225	245	255	275
LW	75	245	265	275	295
LW	85	265	285	295	325
ADD	95	285	305	315	335
LW	105	305	325	335	355
LW	115	325	345	355	375
ADD	125	345	365	375	395

The simulation results shows the five stage instruction execution and the work shown in this paper is an alternate Hardware design Language other than Verilog, System Verilog, VHDL which is very simpler and high level abstraction language than those development languages that offers reconfiguring and code reusability which is not available in Verilog or others. The module design

reusability often makes more convenient for the hardware designer to utilize the same modules for different functionality.

V. CONCLUSION

This work presents the design and implementation of 64-bit RISC V processor using pipeline concepts using bluespec. In this work we have implemented about 40 instructions and the performance of the processor in terms of loading time, instruction in each stages and its execution time were tabulated and analyzed. In this work we have used RISC V 32 bit and 64- bit (extended version) instructions, which is simple to implement. Through the guarded atomic transaction we have achieved better performance. We are concentrated on number of clocks to be reduced for each instruction. We have left some of the work like reducing bubbles in pipeline stage, reorder buffer, instruction and data parallelism could be performed in future.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Mathematical Modeling for Software Defined Networks

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ABSTRACT

Software-defined networking (SDN) makes it possible to control an entire network in software, by writing programs that tailor network behavior to suit specific applications and environments. Unfortunately, developing correct SDN programs is easier said than done. SDN programmers today must deal with several complications. Our goal is to provide a mathematical foundation for software-defined networking that can be used to build and verify high-level SDN tools.

Keywords: SDN, Open flow architecture, COQ

I. INTRODUCTION

Two-tiered architecture

An SDN "program" has two distinct components: the controller program itself and the packet-processing rules installed on switches. These pieces have intricate dependencies that make reasoning difficult—e.g., installing or removing a rule can prevent the controller from receiving future network events. Hence, a programmer must reason about the behavior of the controller program, the rules on switches, and the interactions between the two via asynchronous messages.

Low-level operations

SDN platforms such as Open Flow force programmers to use a low-level API to express high-level intentions, which makes reasoning about SDN unnecessarily hard. Recent revisions of Open Flow expose even more hardware details, such as multiple typed tables, port groups, and vendor-specific features, which makes the problem worse.

II. EVENT REORDERING

Hardware switches employ a number of techniques to maximize performance, including reordering controller messages. This makes the semantics of SDN programs highly non-deterministic, further complicating reasoning. For example, in the absence of barriers, a switch may process messages from the controller in any order.

A programmer who uses these tools will be assured that certain specified formal guarantees will not be violated. To this end, we have developed a low-level model of SDN, called Featherweight OpenFlow. This model is based on the informal OpenFlow specification, but has a precise mathematical definition that makes it suitable for formal reasoning. We have implemented Featherweight OpenFlow in the COQ theorem prover as an executable artifact that can be used to build practical, high-level tools.

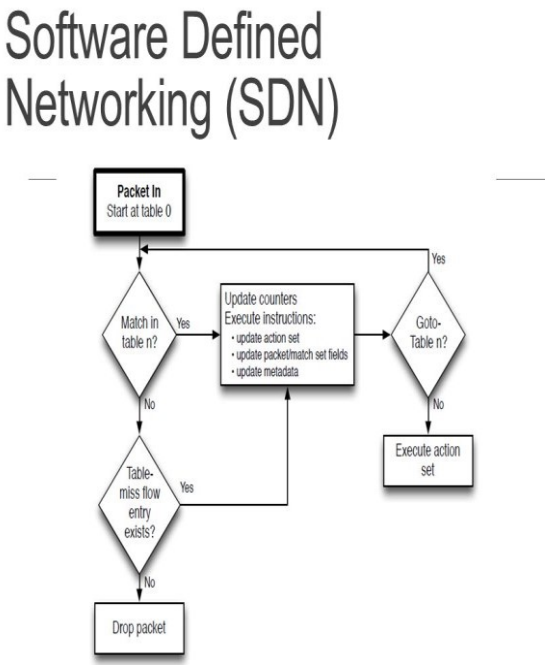

Figure 1. Flowchart of SDN

Our vision is a mathematical foundation for SDNs that enables and facilitates formal network reasoning. Recent advances in for-mal methods have made it possible to precisely model systems of realistic size. In particular, operational semantics have been used to model the behavior of complex systems such as the C programming language, x86 processors, and even whole operating systems.

We seek to develop detailed models of SDNs that support reasoning about essential network functionality such as forwarding, as well as complex features such as bandwidth, queues, controller resources, and failures. With these models, researchers can communicate their ideas concisely and unambiguously; developers of SDN controller platforms and tools can verify that their features are implemented correctly and users

III. SIMPLE CONTROLLER CORRECTNESS PRINCIPLES

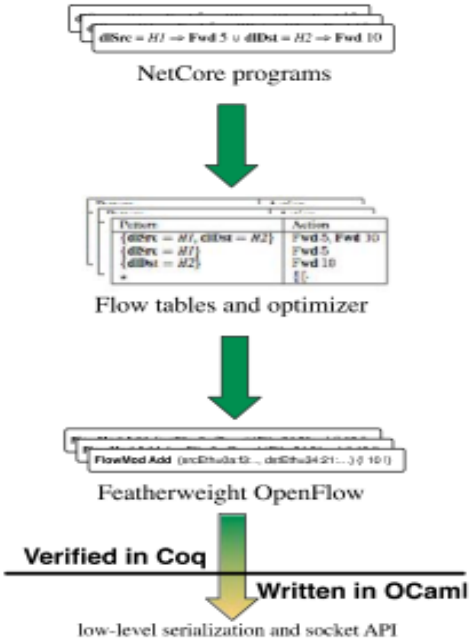

Figure 2. Controller Stack Diagram

Proving from scratch that a given controller correctly implements a given packet-processing function is a formidable task. Doing so requires reasoning about intricate details such as asynchrony in the network and the possibility of message reordering. We have developed a generic reasoning technique that dramatically simplifies the proof task. To verify a controller, it is only necessary to prove two natural properties: (i) the controller program must implement the packet-processing function, and (ii) each switch must approximate the packet-processing function and otherwise send packets to the controller. For most controllers, proving these properties is straightforward.

This result encapsulates a large amount of intricate reasoning about OpenFlow pro-grams and packages it up into a generic controller-correctness theorem. This is a powerful result: to establish correctness for a new controller, we do not have to start from scratch; we only have to prove two simple properties. Thus, controllers that use our technique can safely provide high-level abstractions to SDN applications.

IV. CONCLUSION

We hope that our SDN model will serve as a useful foundation for building other tools. For example, the model could be used as a test-oracle for OpenFlow switches, or as an engine for an OpenFlow software model-checker, in the style of NICE. The model could also be used to develop property-checking tools for high-level abstractions. We have built such a tool for NetCore based an encoding in first-order logic extended with fixed points.

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Optimal Placement of Energy Storage Devices in Microgrids Via Struture Preserving Energy Function

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ABSTRACT

As system transient stability is one of the most important criterions of microgrid (MG) security operation, and the performance of an MG strongly depends on the placement of its energy storage devices (ESDs), optimal placement of ESDs for improving system transient stability is required for MGs. An MG structure preserving energy function is firstly developed for voltage source inverter based MGs since the existing energy functions, based on synchronous generators and the conventional power system, are not applicable for MGs. The concept of internal potential energy of distributed energy resource is presented instead of the kinetic energy term in traditional energy function. And then, a novel approach for the optimal placement of ESDs is proposed based on MG structure preserving energy function for improving MG transient stability. Simulation and experimental results show that the proposed method can be used to find the optimal placement of ESDs, and to improve the system stability effectively.

Keywords: Transient stability , structure preserving energy function, energy storage devices, optimal placement, micro grids.

I. INTRODUCTION

Environmental concerns and fuel cost uncertainties associated with the use of conventional energy sources have resulted in rapid growth in the amount of the renewable energy resources (RES). For instance, between 2005 and 2030, the share of RESs in the 27 European Union member states gross power generation will be more than double from 14.3% to 36.1%. In fact, the share of intermittent RESs will reach 20.7% of the total power generation in 2030. With respect to wind and solar as the most use of renewable generation, however, when the renewable resource penetration reaches sufficiently high levels (about 20%–30% of total generation), the intermittent nature of such generation can begin to have noticeable, negative effects on the entire grid. Recently, the integration of ESDs with RESs has become one.of the most viable solutions for facilitating increased penetration of renewable DG resources. Beginning with the U.S.Department of Energy (DOE) “Grid 2030 Vision” Conference in April 2003, energy storage emerged as a top concern for the future. In 2007 the DOE convened an Electricity Advisory Committee (EAC) to make recommendations for an energy road map for the United States including energy storage. These dispatch able storage technologies will provide lots of benefits such as greater reliability, improved power quality, and overall reduced energy costs for utilities, DG owners, and customers. However, ESDs benefits are strictly related to their location and sizing as well as storage technology, which have been frequently

addressed in the literatures by using a variety of optimization techniques.

BLOCK DIAGRAM

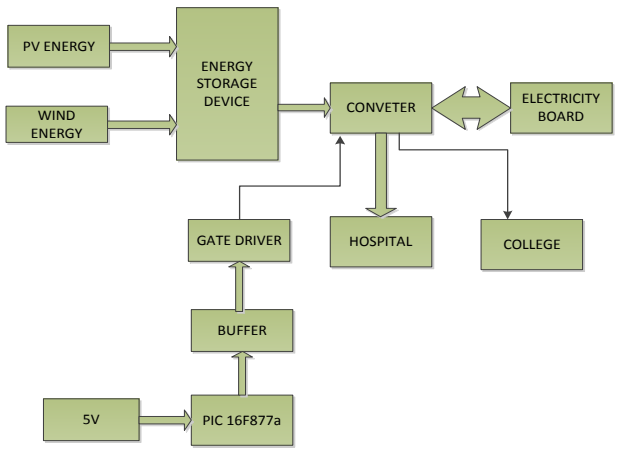

Figure 1

II. EXISTING SYSTEM

Existing energy function is derived based on synchronous generators andthe large power system. Synchronous generators store energy through rotor, so there is kinetic energy in existing energy function. The large power system is a high-voltage system which is inductive. However, MG is a low-voltage system which is mainly resistive, and also the different load character needs to be considered. Specifically, inverter-based DG units do not have rotating parts, which means that the kinetic energy term in traditional energy function does not exist. Therefore, the components and analysis have a big difference between the large power system and MG. So existing energy function can hardly be used to analyze the stability of MG. It is worthwhile to develop an energy function based on MG for assessing stability of MG effectively.

III. PROPOSAL SYSTEM

A novel approach for the optimal placement of ESDs is proposed based on MG structure preserving energy function for improving MG transient stability. Simulation and experimental results show that the proposed method can be used to find the optimal placement of ESDs, and to improve the system stability effectively.

Energy Storage

- ✓ Energy is stored to use it at a different time than when it was generated
- ✓ The process of converting the energy to storable form means that some energy is lost due to inefficiency and heat
- ✓ Additional energy is lost when the energy is released or recovered due to a second inefficiency
- ✓ Ideally, storage is avoided to have a more efficient process
- ✓ Shifting the energy from usage peaks to low-use times helps the utility, and customers would be rewarded by lower charges
- ✓ Renewable energy is often intermittent (like wind and sun), and storage allows use at a convenient time
- ✓ Compressed air, flywheels, weight-shifting (pumped water storage) are developing technologies
- ✓ Batteries are traditional for small systems and electric vehicles; grid storage is a financial alternative
- ✓ Energy may be stored financially as credits in the electrical "grid"

MATLAP CIRCUIT

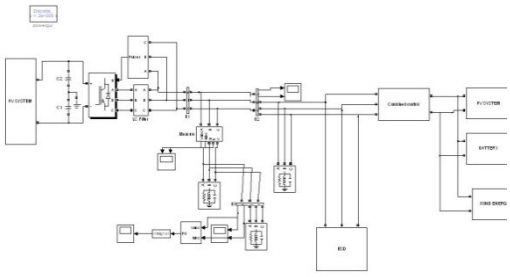

Figure 2

SIMULATION OUTPUT

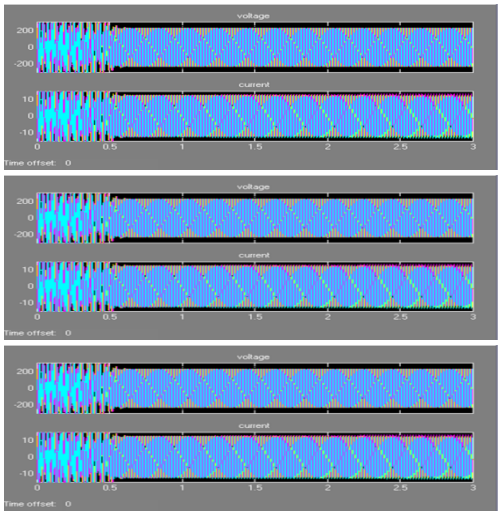

Figure 3

Abovediagram shows first node output, second node output, third node output.

ADVANTAGE

As the world moves towards renewable energy generation and acts to counter climate change, micro grids offer a range of benefits which can provide assistance both locally and nationally in terms of the environmental benefits.

- ✓ Reduced Electricity Bill
- ✓ Diverse application
- ✓ Low maintenance cost
- ✓ Wind is a renewable energy resource and there are no fuel costs. ...

HARDWARE

Figure 4

IV. CONCLUSION

This paper studies the optimal placement of ESDs on the basis of MG structure preserving energy function. Firstly, a MG structure preserving energy function has been proposed based on the voltage-source inverter based MG. Secondly, a novel approach for optimal location of ESDs is proposed based on the MG branch transient energy function to improve MG transient stability. For the sake of system stability, the proposed stability-oriented optimizing method sacrifices economy for faster recovery time and less overshoot. In other words, the proposed method provides a more specific method to improve reliability and stability that ESDs contribute to system. Finally, the simulations and experimental results verify: 1) the validity and practicality of the proposed method in optimizing placement and mitigating transient unbalance energy; 2) the proposed method further improves system transient stability compared with existing and state-of-art research. Other issues such as the ESS cost analysis and the integration of probabilistic nature of failures and multiple and/or cascading failures into the proposed method will be investigated in future work.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Single Phase TSC Analysis

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ABSTRACT

A single-phase electric machine invokes a great reactive power demand in operation, resulting in a large voltage fluctuation in the supply system. Furthermore, the frequent and rapid operating characteristics of an electric welding machine cause a serious voltage flicker problem. The operation of welding equipment also generates significant harmonic current distortion, and distorts the voltage waveform of the supply system. Hence, this study focused on designing and applying a thyristor switched capacitor (TSC) bank for voltage flicker improvement. However, the single-phase TSC should also satisfy the reactive power demand and compensation speed, considering proper ratings of TSC to bear high harmonic distortion. This study shows the calculation results and discusses the impact of different capacities and different step numbers on TSC design. In addition, thyristor switches and a single-phase power factor controller were designed and implemented. The experimental results are also presented.

Key words: TSC, Thyristor valve, capacitor bank, Voltage stability

I. INTRODUCTION

A single-phase electric machine invokes a great reactive power demand in operation, resulting in a large voltage fluctuation in the supply system.[1] Furthermore, the frequent and rapid operating characteristics of an electric welding machine cause a serious voltage flicker problem[2]. The operation of welding equipment also generates significant harmonic current distortion, and distorts the voltage waveform of the supply system[3]. Hence, this study focused on designing and applying a thyristor switched capacitor (TSC) bank for voltage flicker improvement. However, the single-phase TSC should also satisfy the reactive power demand and compensation speed, considering proper ratings of TSC to bear high harmonic distortion[4]-[6]. This study shows the calculation results and discusses the impact of different capacities and different step numbers on TSC design[7]. In addition, thyristor switches and a single-phase power factor controller were designed and implemented. The experimental results are also presented.

II. LITERATURE SURVEY

The development of an optimal solution to network problems was initiated by the desire to find the minimum of the operating cost for the supply of electric power to a given load (Kichmayer 1958). The problem evolved as the so called dispatch problem. The principle of equal incremental cost to be achieved for each of the control variables or controllers has already been realized in the pre-computer era when slide rules and the like were applied.

A major step in encompassing not only the cost characteristics but also the influence of the network, in particular the losses were the formation of an approximate quadratic function of the network losses

expressed by the active injections. Its core was the B-matrix which was derived from a load flow and was easily combined with the principle of equal incremental cost 19 thus modifying the dispatched powers by loss factors. The formulation of the problem must be considered as a remarkable improvement as shown by Squires, Carpentier, however, still there was no effective algorithm available. At that time the ordinary load flow made considerable progress (Tinney et al 1967, Scott 1974) and the capabilities of computers showed promising aspects.

Peschon et al (1968) proposed a method to minimize the transmission power losses by selecting of reactive power injections in to the systems and using transformer tap changing settings. They have included a suitable method to get the solution from a feasible optimal point, but it is more time consuming.

Dommel and Tinney (1968) presented a method to find the optimal power flow using a non linear optimization technique. They have used a non linear objective function of cost or losses using kuhn-tucker conditions, but control variables are not coordinated due to slow convergence. This is not suitable for large systems.

Hano et al (1969), proposed a new method of controlling the system voltage and reactive power distribution in the system. They followed the sensitivity relation ship between controlled variables and loss sensitivity indices and the implemented direct search algorithm to minimize the losses.

Narita et al (1971) developed the sensitivity analysis using method of base optimization technique to minimize the voltage deviation and minimize the system losses. To obtain successful operation they used voltage and reactive power regulating devices installed at various points. 20 Scott (1974) proposed power flow calculations to perform power system planning, operational planning and control. the OPF is solved by varities of methods i.e, successive linear programming method. Minimization of transmission losses can be achieved by controlling system devices such as generators, capacitors, reactors and tap changing transformers; it is possible to minimize the system losses by reactive power redistributions in the system.

Mamandur et al (1981) proposed an efficient algorithm to minimize the transmission loss. Considering the network performance constraints and the constraints on the control variables, they were applied a dual linear programming technique to find optimal adjustments to the control variables satisfying many constraints. This method is used to improve voltage profile and minimize system losses under operating condition. The result is showing to zigzagging due to slow convergence.

Shahidehpour et al (1990) discussed an overview of the reactive power allocation in electric power systems. Optimal reactive power control is the most important functions giving inadequate reactive power bring up some problems such as low voltage profile, extra loss and equipment overload. They have carried out to solve this problem, using nonlinear and linear programming methods.

Bhatele et al (1985) proposed a mathematical formulation of optimal power control problem to minimize and control the voltage profile. They have developed reduced gradient and Fletcher's update algorithm to solve this problem. In most of the studies, only they have considered system losses minimization. They are not considered light load conditions when the generators are under exited.

III. EXISTING METHOD

3.1 Ways of Improving Voltage Stability And Control

Reactive power compensation is often most effective way to improve both power transfer capability and voltage stability. The control of voltage levels is

accomplished by controlling the production, absorption and flow of reactive power. The generating units provide the basic means of voltage control, because the automatic voltage regulators control field excitation to maintain scheduled voltage level at the terminals of the generators. To control voltage throughout the system we have to use addition devices to compensate reactive power . Reactive compensation can be divided into series and shunt compensation. It can be also divided into active and passive compensation. But mostly consideration will be focused on shunt capacitor banks, static var compensator (SVC) and Static Synchronous Compensators (STATCOM), which are the part of group of active compensators called Flexible AC Transmission Systems (FACTS). The devices used for these purposes may be classified as follows

- ✓ Shunt capacitors
- ✓ Series capacitors
- ✓ Shunt reactors
- ✓ Synchronous condensers
- ✓ SVC
- ✓ STATCOM

IV. PROPOSED METHOD

Thyristor switched capacitor:

Thyristor switched capacitor (TSC) is a type of equipment used for compensating reactive power in electrical power systems. It consists of a power capacitor connected in series with a bidirectional thyristor valve and, usually, a current limiting reactor (inductor). The thyristor switched capacitor is an important component of a Static VAR Compensator. A TSC normally comprises three main items of equipment: the main capacitor bank, the thyristor valve and a current-limiting reactor, which is usually air-cored.

1) Capacitor bank

The largest item of equipment in a TSC, the capacitor bank is constructed from rack-mounted outdoor capacitor units, each unit typically having a rating in the range 500 – 1000 kilovars (kVAr).

2) TSC reactor

The function of the TSC reactor is to limit the peak current and rate of rise of current (di/dt) when the TSC turns on at an incorrect time. The reactor is usually an air-cored reactor, similar to that of a TCR, but smaller. The size and cost of

3) Thyristor valve

The thyristor valve typically consists of 10-30 inverse-parallel-connected pairs of thyristors connected in series. The inverse-parallel connection is needed because most commercially available thyristors can conduct current in only one direction. The series connection is needed because the maximum voltage rating of commercially available thyristors (up to approximately 8.5kV) is insufficient for the voltage at which the TCR is connected. For some low-voltage applications, it may be possible to avoid the series-connection of thyristors; in such cases the thyristor valve is simply an inverse-parallel connection of two thyristors.

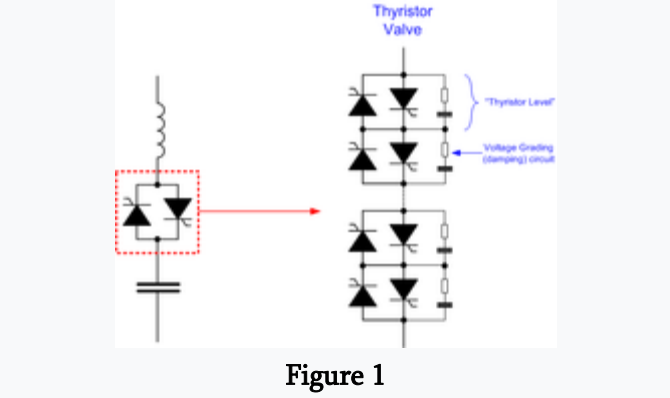


Figure 1

4) Typical TSC valve

In addition to the thyristors themselves, each inverse-parallel pair of thyristors has a resistor–capacitor ''snubber' circuit connected across it, to force the voltage across the valve to divide uniformly amongst the thyristors and to damp the "commutation overshoot" which occurs when the valve turns off.The thyristor valve for a TSC is very similar to that of a TCR, but (for a given AC voltage) generally has between 1.5 and 2 times as many thyristors connected in series because of the need to withstand both the AC voltage and the trapped capacitor voltage after blocking.The thyristor valve is usually installed in a purpose-built, ventilated building, or a modified

shipping container. Cooling for the thyristors and snubber resistors is usually provided by deionised water.

Special types of TSC

Some TSCs have been built with the capacitor and inductor arranged not as a simple tuned LC circuit but rather as a damped filter. This type of arrangement is useful when the power system to which the TSC is connected contains significant levels of background harmonic distortion, or where there is a risk of resonance between the power system and the TSC.In several "Relocatable SVCs" built for National Grid (Great Britain),[3] three TSCs of unequal size were provided, in each case with the capacitor and inductor arranged as a "C-type" damped filter. In a C-type filter, the capacitor is split into two series-connected sections. A damping resistor is connected across one of the two capacitor sections and the inductor, the tuned frequency of this section being equal to the grid frequency. In this way, damping is provided for harmonic frequencies but the circuit incurs no power loss at grid frequency.

Circuit Diagram of TSC:

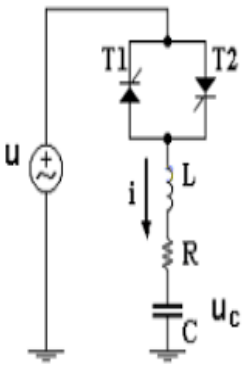


Figure 2

I

nternal structure of Microcontroller:

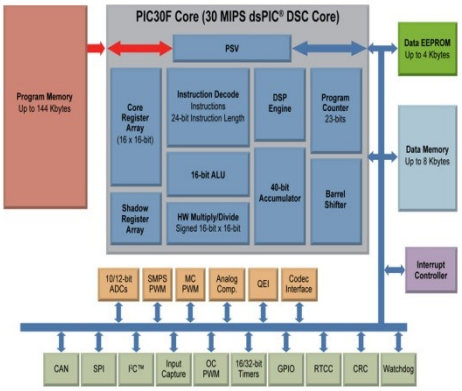
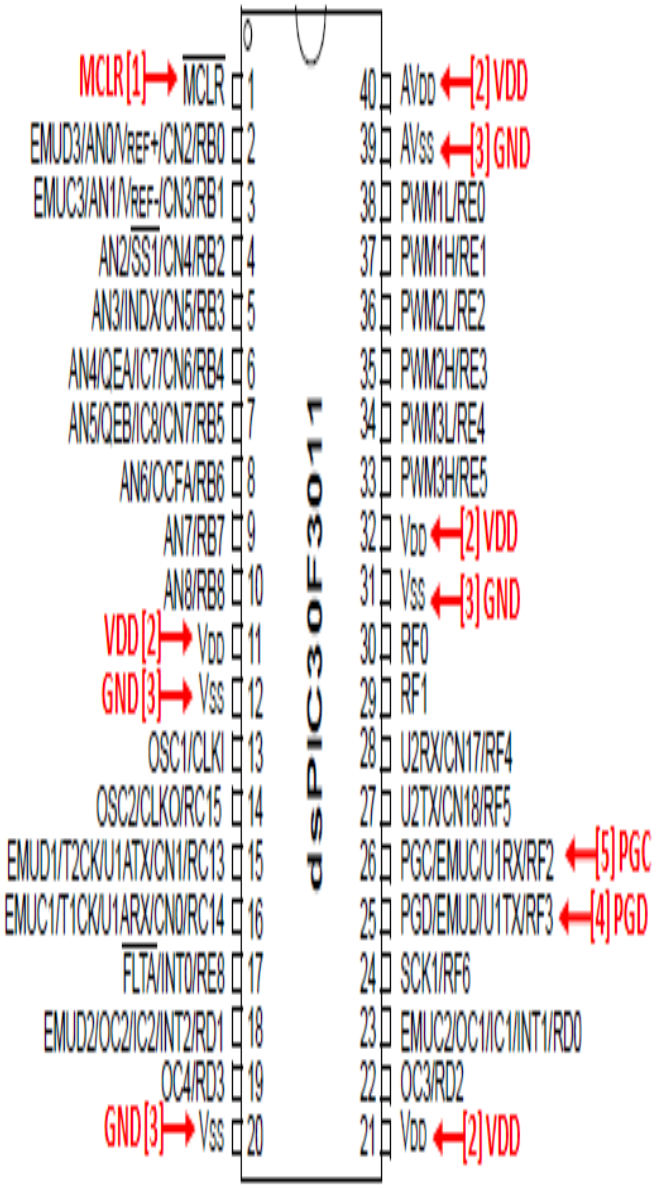


Figure 3

Dspic 30F 4011 pin details:



FFigure 4

Block diagram:

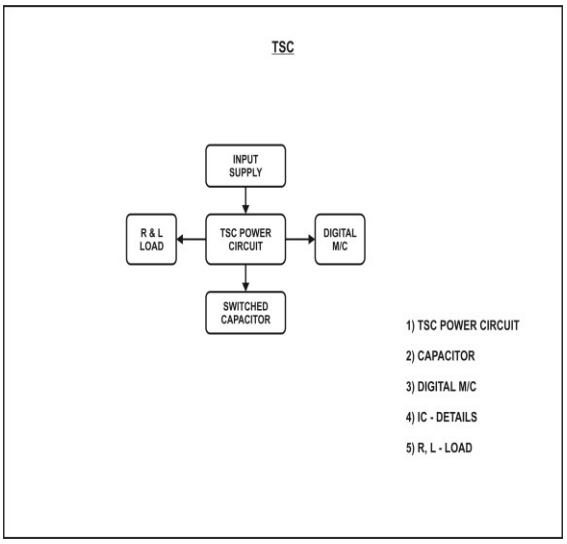


Figure 5

Hardware details:

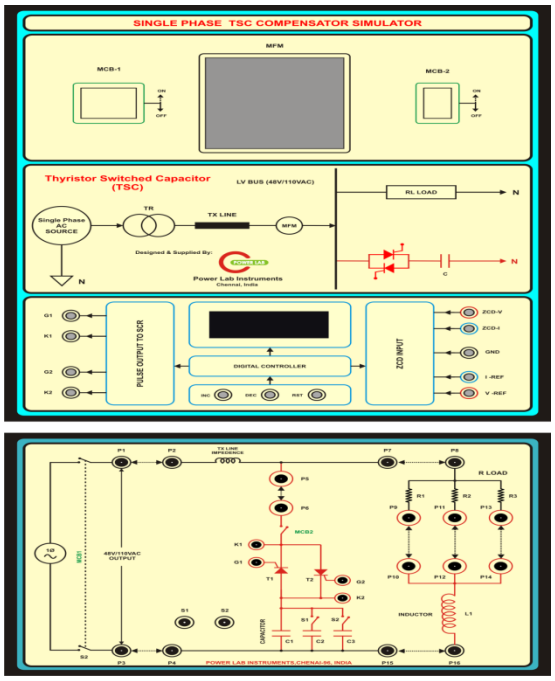


Figure 6

- ✓ This setup consist of Two number of ON/OFF mcb
- ✓ Dspic 30F4011 based Micro Controller
- ✓ Power factor meter
- ✓ Scr driver board
- ✓ Capacitor bank
- ✓ shunt Reactor
- ✓ R-L load
- ✓ Designed this setup is 110v

SCR Driver board:

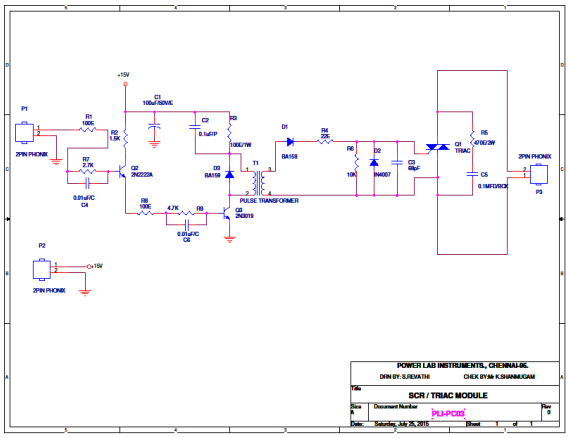


Figure 7

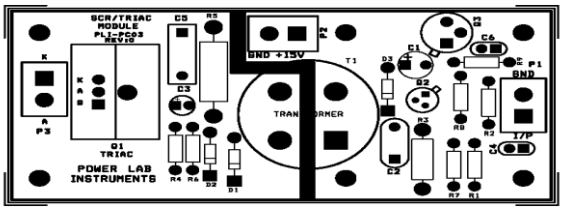


Figure 8

V. CONCLUSION

This presents switching of capacitor bank for power factor improvement. Power factor improvement is very useful. The microcontroller based Thyristor Switched Capacitor is providing a better power factor to nearly unity with light loading and can be maintained to around 0.9 with increase in system loading .

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Micro Controller Based Earth Fault Relay

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ABSTRACT

One of the most common electrical motor used in most applications is inductor motor. This paper presents microcontroller based control system for protector of a Induction motor from earth fault. Due to electrical fault the windings of motor get heated which leads to insulation failure and thus reduce the life time of motor. This protection scheme protects the induction motor from earth fault from initial stage of insulation failure. It also measures the leakage current. Three phase induction motors are industry's workhorses and widely used as electromechanical energy conversion devices. Although induction machines are considered relatively reliable and robust due to their simple design and well-developed manufactures technologies, failure do occur and may severely disrupt industrial process and even lead to disastrous accidents. To prevent these failure happen, many techniques have been developed for early condition monitoring. The computer based protection methods are costlier then old classical methods and complex. Hence to protect an Induction, motor easily a microcontroller based fault detection and protection is proposed. The proposed system is tested with setting of values presetted values, from the results, it is observed that the results are satisfactory, reliable gives quick response, cost effective and highly resatile.

Keywords: Earth fault, Microcontroller, Induction motor.

I. INTRODUCTION

A large number of motors are being used for general purpose in our surrounding from house-hold equipment to machine tools in industrial facilities. Among all these motor Induction motors are the most widely used motor they are robust, reliable and durable. Although Induction Motors are reliable, they are subjected to some undesirable stresses, causing faults resulting in failure. Failure of such Induction motor may cause plant shutdown, personal injuries and waste of raw material. However, induction motor faults can be detected in an initial stage in order to prevent the complete failure of an induction motor and unexpected production costs. The main reason for the motor faults are 1. mechanical and 2.electrical stresses. Mechanical stresses are caused due to overloads and abrupt load variations. The electrical stresses may produce stator winding short circuits and final result in a complete motor failure.

The electrically related faults such as over voltage, over current, under voltage, under current, over temperature. Various protection methods are available in voltage and current relays are used. 1.The protection using solid state relay has been

discussed by designing motor current signature analysis [MCSA] with wavelet transformer methods. 2.Artificial intelligent fault monitoring approach 3.Fourier spectral analysis using motor current FFT and 4.MATLAB programming for fault frequency methods and 5.Zig Bee based methods are proposed.

The above said methods are simulation base methods. Recently the PLC based protection systems including all variable parameters of three phase induction motor have been proposed. This method is based on computer and programmable integrated circuit (PIC). This reduces most of the mechanical components. But they are highly complex system and costlier. In order to overcome these problems, the induction motor is monitored by using microcontroller which plays a major role. The presented methods monitor the operating induction motor continuously with the minimum interactive of human. Microcontroller based protection is having advantages. Thease are low cost, simple and higher accuracy. The protection of induction motor by different faults such as over/under voltage, over current, over speed, phase failure, frequency and over temperature,earth fault are possible We consider the earth fault in this proposed work.

These are various components which cause engine disappointment. The most well-known are:

- ✓Overload
- ✓Single staging
- ✓Voltage unbalance
- ✓Voltage too high/low
- ✓Bearing disappointment
- ✓Rapid obligation cycle
- ✓Restricted ventilation
- ✓Moisture and vibration

On the off chance that mechanical disappointments are wiped out. Shielding the engine windings from over temperature is the prime function of motor protection.

But even bearing failures can result in motor windings failure if not detected in time. There are a number of ways that motors can be protected with respect to the needs of ways that motors can be protected with respect to the needs of plant management. Table I below classifies these functions. There is no substitute for the proper application of motors or proper maintenance. However, protective devices can help you to use the motor to its optimum limits.

Types of Motor Failure and Protective Features

Table 1. Breakdown causes, effects and possible motor damage

Causes	Effect	Possible damage
Thermal overload: Extreme starting condition Locked rotor High overload Under-voltage Intermittent operation	Over-current and Thus unacceptable heating-up of windings	Soldered joint damage rotor cage burnt windings stator windings
Cooling problems: Restricted cooling Ambient temperature too high	unacceptable heating-up	burnt windings stator windings
Electrical causes: Single phase condition Unbalanced voltage	 Unbalance over-current of windings heating-up	 Individual windings Or parts burnt

Earth fault Shorted turns Winding short circuit	depending on motor size and bearing damage load	
Mechanical causes: Imbalance Mis-alignment Improperly installed drive(e.g. bearing load of V-belts too high)	uneven wear of bearings	Bearing damage

Necessity for Motor Protection

It could be accepted that legitimately arranged, dimensioned, introduced, worked and kept up drives ought not to separate. In actually, be that as it may, these conditions are barely ever perfect. The recurrence of diverse engine harm varies since it relies on upon distinctive.

Particular working conditions. Measurements demonstrate that yearly down times of 0.5…4% must be normal. Most breakdowns are brought on by an over-burden. Protection shortcomings prompting earth issues, swing to-turn or twisting short – circuits are brought on by overabundance voltage or pollution by sogginess, oil, oil, dust or chemicals.

The Approximate percentages of by these individual faults are :

- ✓ Overload 30%
- ✓ Insulation damage 20 %
- ✓ Phase failure 14 %
- ✓ Bearing Damage 13 %
- ✓ Ageing 10 %
- ✓ Rotor damage 5 %
- ✓ Other 8 %

Hardware design and working:

This system of protection of 3 phase Induction motor can be implemented using 8051 Microcontroller, Current transfer, Potential transformer, relay, and LCD display. Circuit gets activates when it gets the supply voltage. Motor will continue running until critical condition occurs. Voltage supply to the MC is provided through transformer, diode rectifier and 7805 voltage regulator. Current transformer with rating of 5 A provide current equivelent to the supply current to micro controller.

The voltage transformer will provide supply voltage equvue of 12 V Whenever measured value of current exceeds the set value then controller will send signal to relay to turn off motor.

Main Component Used in Circuit

1.Microcontroller 8051
2. Bridge rectifier
3. Induction Motor
4. Relay 12
5. LCD Display (16 x 2)
6. Current Transformer
7. Voltage Transformer.

Description of above component:

Microcontroller 8051

Microcontroller receives data from current transformer then convert it from Analog to Digital signal and then compare with the pre programmed valves.

Salient features of 8051 microcontroller are given below.

·Eight bit CPU
·On chip clock oscillator
·4Kbytes of internal program memory (code memory) [ROM]
·128 bytes of internal data memory [RAM]

·64 Kbytes of external program memory address space.
·64 Kbytes of external data memory address space.
·32 bi directional I/O lines (can be used as four 8 bit ports or 32 individually addressable I/O lines)
·Two 16 Bit Timer/Counter :T0, T1
·Full Duplex serial data receiver/transmitter
·Four Register banks with 8 registers in each bank.
·Sixteen bit Program counter (PC) and a data pointer (DPTR)
·8 Bit Program Status Word (PSW)
·8 Bit Stack Pointer
·Five vector interrupt structure (RESET not considered as an interrupt.)
·8051 CPU consists of 8 bit ALU with associated registers like accumulator 'A' , B register,
PSW, SP, 16 bit program counter, stack pointer.
·ALU can perform arithmetic and logic functions on 8 bit variables.
·8051 has 128 bytes of internal RAM which is divided into Working registers [00 –1F]oBit addressable memory area [20 –2F]o
General purpose memory area (Scratch pad memory) [30-7F]

Bridge Rectifier

We use bridge to get pure DC signal. Bridge rectifier is highly efficient than others. It consists of 4 diodes D1, D2, D3 and D4. When we gives AC supply to the circuit in positive half cycle D1 and D2 become forward biased and it will start conduction at the same time D3 and D4 are reverse biased hence it does not conduct. In negative half cycle D3 and D4 become forward biased and start conduction and D1, D2 become reverse biased and stop conduction.

Induction Motor

An electrical motor is such an electromechanical device which converts electrical energy into mechanical energy.

Specification: 3 phase squirrel cage induction motor,415v, 0.5HP, 50 HZ,4 pole, speed upto 1500 rpm, Insulation class E

Relay

A relay is an electricity operated switch. Many relays use an electromagnet to mechanically operate a switch , but other operating principles are also used, such as solid – state relays. Relays are used where it is necessary to control a circuit by a separate low-power signal, or where several circuits must be controlled by one signal. In this project we use high precision neumerical relay for protecting the motor from earth fault.

LCD Display

Liquid Crystal Display is used for display the measured reading and if fault it also show on LCD.16x2 LCD is used in circuit. It having 16 character and 2 rows.

II. BLOCK DIAGRAM AND FLOW CHART

Block Diagram

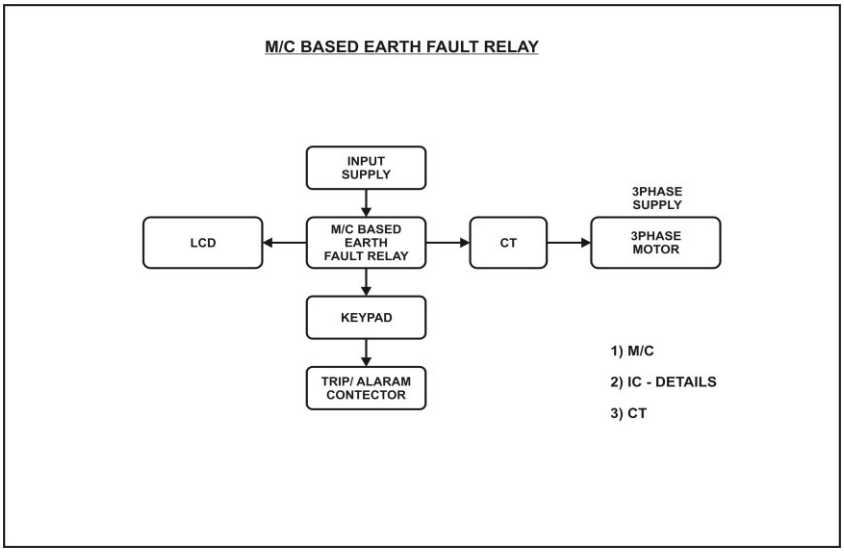

Figure 1

Flow Chart For Over View of Project

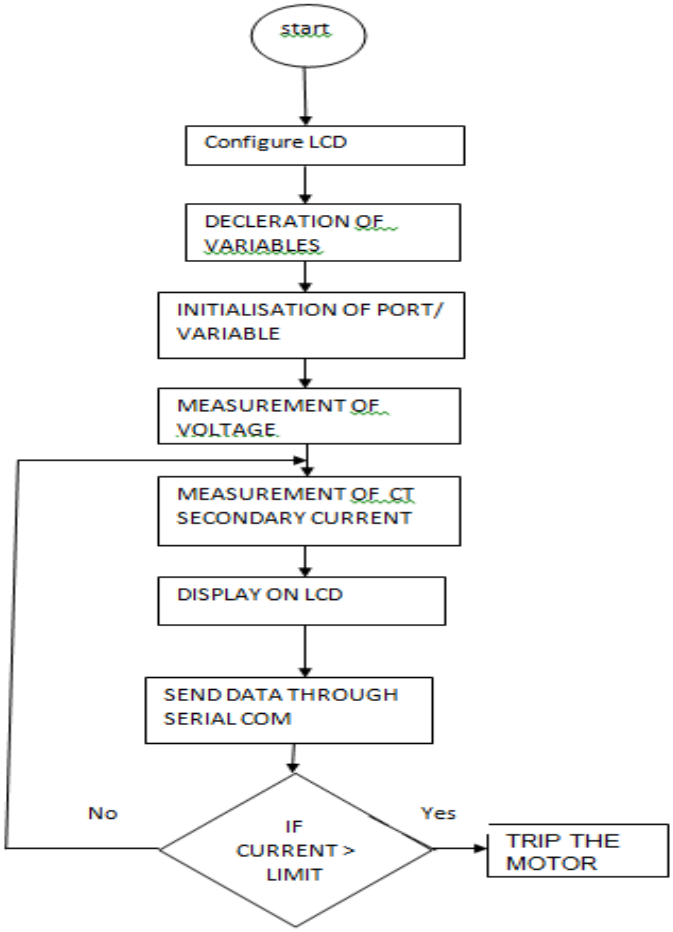

Figure 1

III. CONCLUSIONS

In industries due to over-voltage, Under-voltage, Over-current,moisture and over-temperature motor winding may get damage hence this paper has successfully present reliable, fast and efficient system for induction motor protection from earth fault. This system can be implemented in any industries where the protection of motor is essential requirement. The thesis is based on protection of 3 phase induction motor under faulty condition and it is implemented using microcontroller, relay driver circuit and current transformer.

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Amarapur2 1M.tech Student P.D.A college of Engineering Kalaburgi, India 2Professor, Electrical and Electronics Department, P.D.A College of Engineering, Kalaburgi, India

[4]. International Journal of Research in Computer Science and Information Technology (IJRCSIT) 37 PIC Microcontroller Based Speed Control of Three Phase Induction Motor Using Single Phase Supply B. N. Jamadar1, Dr. S. R. Kumbhar2 & D. S. Sutrave3

[5]. International Advanced Research Journal in Science, Engineering and Technology ISO 3297:2007 Certified Vol. 4, Issue 4, April 2017 Copyright to IARJSET DOI10.17148/IARJSET.2017.4404 22 PIC Based Protection of Single Phase Induction Motor Lata Chavan 1, Prerana Chafekar2, Avnish Bhatt3, Mitesh Patel4, Sarika Kuhikar5 U.G. Student, Department of Electronics Engineering, V.E.S.I.T, Mumbai, India1,2,3,4 Assistant Professor, Department of Electronics Engineering, V.E.S.I.T, Mumbai, India.

National Conference on 'Innovative Research on Robotics, Circuits and Technology' (IRCT 2018)
Organized By : CIrcuit Branches of SCSVMV, (EEE, ECE, EIE & Mechatronics) , Kanchipuram, Tamil Nadu, India
In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Management of Effluents in Industries

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ABSTRACT

Water pollution has become a higher priority task to handle these days and the Industries are keeping major part on water pollution. The polluted water is commonly called as Effluent. So, the effluent management among industries is a vital process and that should contain the effluent Monitoring, Data Acquiring and control over the effluent. When talking about Effluent, the unnecessary water wastage is also considered as water pollution. Because of this type of pollution, the ground water level is decreased and which could lead to the water crisis in future. So, considering all these factors we created a system which can monitor, acquire data and store for future, and do control over the intake pure water of an industry as well as the outlet effluent. Our project limits the intake water and outlet effluent based on the size of industry and if any abnormal activities of the industry is observed to their corresponding limits, then this system will ensure the responsive control activities against them.

Keywords: Industrial Automation, SCADA, PLC and KepServer.

I. INTRODUCTION

Effluent Management system helps in monitoring the total ground water taken and total amount of effluent produced by the industry. This data for each instance is stored in server for remote access. In addition to that this system sets limitations for taking ground water and also for the effluent production. If there are any deviations made by the industry on limits, control actions can be provided in order to make the industries to intake and release effluents as per the limits.

What is an Effluent?

Effluent is defined by the United States Environmental Protection Agency as "wastewater - treated or untreated - that flows out of a treatment plant, sewer, or industrial outfall. Generally, refers to wastes discharged into surface waters". The Compact Oxford English Dictionary defines effluent as "liquid waste or sewage discharged into a river or the sea".

Effluent in the artificial sense is in general considered to be water pollution, such as the outflow from a sewage treatment facility or the wastewater discharge from industrial facilities. An effluent sump pump, for instance, pumps waste from toilets installed below a main sewage line.

Primary Objective

- To monitor the inlet ground water and outlet effluent production of every industries.
- To acquire data and store them in a server for remote access.
- To control the industries ground water usage

and effluent production with some reasonable limits.

- To treat the effluent for the reuse of water and collect the treatment charges from the corresponding industries.

Our proposing method consists of a fully developed SCADA screen for the Management of the effluents in the industries. This screen is developed such that, it is interfaced with the programmable logic controller using the software named as KEP server. The values are collected and stored using trends and historical trends functions of the SCADA screen and the controls are made by the switching operation performed by the PLCs. For continuous monitoring of values from long distances, a methodology known as port forwarding is used to accumulate data's and use it for control purposes.

The earlier methodologies were just used to accumulate data over short distances, monitor them and perform controls based on the values accumulated. But our system provides a long-range process control from a single screen to a number of systems inter connected.

II. SOFTWARES & COMPONENTS USED

2.1. Wonderware InTouch V10.10 (SCADA)

The combination of telemetry and data acquisition is referred as SCADA (Supervisory Control and Data Acquisition system) [1]. Wonderware InTouch delivers truly transformational value. By improving real-time visibility into your processes, InTouch greatly improves operator effectiveness and increases control of your processes to simplify and enforce standardization and change management. InTouch includes numerous new visual enhancements to improve the ability to identify and address abnormal situations before they impact operations. The powerful tools in InTouch go beyond the simplistic graphics provided by other vendors and enable application builders to focus on creating valuable content and to easily assemble effective HMI applications for simplicity, agility and performance.

Application of In-touch in Management of Effluents in Industries.

Effluent Management uses Wonderware In-touch to develop three unique windows.

1. Front Window.
2. Login Window.
3. Industry Window.

FRONT WINDOW

Front window presents data in an organized table shown below and which includes the following data. The variables in InTouch are called TAGS. The data are:

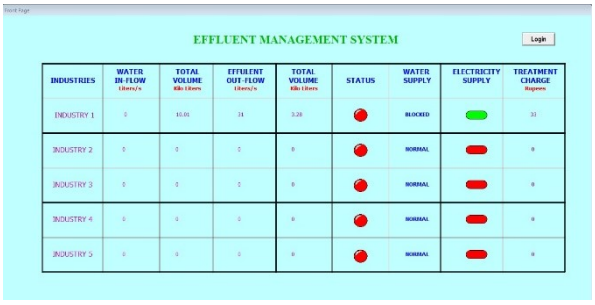

Figure 1. Front Window

Table 1

S.no	Tag	Type
1	IFS#	I/O Real
2	ITV#	Memory Discrete
3	OFS #	I/O Real
4	OTV#	Memory Discrete
5	I#	Memory Discrete
6	P#	Memory Discrete
7	Logout	Memory Discrete

LOGIN WINDOW

Login window serves as a security authorization window which is the only gateway to gain access to change the parameters, values and control limits. Which also provides manual control at any critical strategies.

Figure 2. Login Window

Login window has three tags

1. For the username there is a textbox is used with the tag name "User".
2. For the Password another text box is used with the tag name "Pwd".
3. For the login purpose there is a detend button is used with the tag name "Logon". The Login button will work only if the username and password is a match and it leads to the Front window.

Table 2. Login Tags

S.no	Tag	Type
1	User	Memory Message
2	Pwd	Memory Message
3	Logon	Memory Discrete

INDUSTRY WINDOW

The Industry window monitors and controls a single industry 24*7. Based on the number of industries this window can be added and by doing which all the industries can be monitored and controlled efficiently.

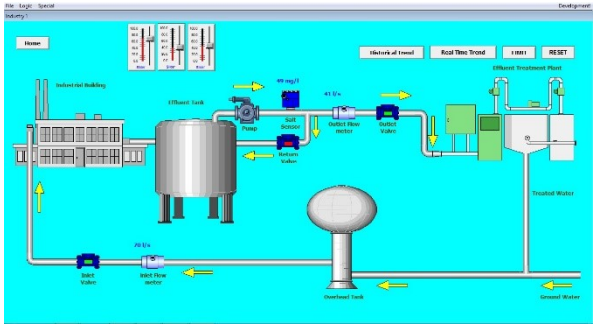

Figure 3. Industry Window.

Industry window consists of the following components

Detend Buttons

Home

When this home button is pressed it navigates to the user to the Front window.

Reset

Reset button resets the Inlet total volume and outlet total volume to zero.

Limit

Limit button opens a pop-up window which allows the user to modify the limits and login information.

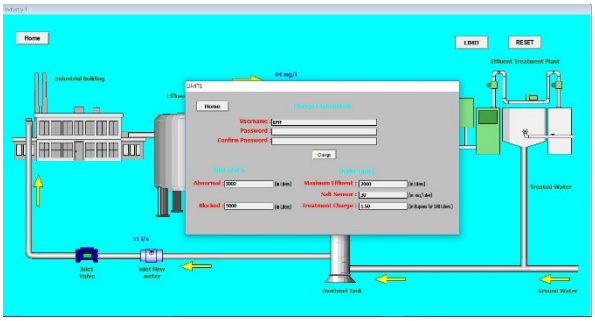

Figure 4. Limit Window

Real time trend

Real time trend button opens a window which contains the graphical monitor of real time variables. (E.g. A graph show the current values of inlet flow meter, outlet flow meter and salt sensor)

Historical trend

Historical trend button opens a window which contains the graphical monitor of the variables and which allows us to set the time period. Because of this reason it can be used to see the values of the variables in the past at a particular time.

Tags used for Industry window.

Table 3. Tags for Industry Window.

S.no	Tag	Type
1	IFS#	I/O Real
2	IV#	I/O Discrete
3	OFS #	I/O Real
4	OV#	I/O Discrete
5	SS#	I/O Real
6	RETV#	I/O Discrete
7	Limit1	Memory Discrete
8	Reset	Memory Discrete

9	Username	Memory Message
10	Password	Memory Message
11	Confirm Password	Memory Message
12	Change	Memory Discrete
13	Abnormalstate	Memory Real
14	Blockedstate	Memory Real
15	Maxeffluent	Memory Real
16	Saltsensor	Memory Real
17	Treatmentcharge	Memory Real

All of the tags are used and initiated using the window script feature of Intouch Software. Scripts are not included in this document.

2.2 WPLSoft (Delta PLC)

WPLSoft is a software for PLC (Programmable logic controller). When PLC is in operation, use WPLSoft to monitor the set value or temporarily saved value in timer (T), counter ©, and register (D) and force On/Off of output contacts. PLC is a control system using electronic operations.

WPLSoft Programmable Logic Controller or programmable controller software is a digital computer interface used for automation of typical industrial electromechanical processes, such as control of machinery on factory assembly lines, amusement rides, or light fixtures using Delta PLC's. PLCs are used in many industries and machines. PLCs are designed for multiple analogue and digital inputs and output arrangements, extended temperature ranges, immunity to electrical noise, and resistance to vibration and impact. Programs to control machine operation are typically stored in battery-backed-up or non-volatile memory. The functionality of the PLC has evolved over the years to include sequential relay control, motion control, process control, distributed control systems and networking. The data handling, storage, processing power and communication capabilities of some modern PLCs are approximately equivalent to desktop computers.

Application of WPLSoft in Management of Effluents in Industries.

WPLSoft is the main controlling software of the DELTA PLC. We used the DVP28 SV for the controlling. In addition to that DVP 04AD is an analog extention module which is also added to read the flow meter reading.

The WPLSoft is used for reading the Analog value of the flowmeter and scaling it for our convinience.

There are two main instruction is used for interfacing the analog module with the PLC.

1.FROM 2.SCLP

1.From instruction is used for reading the data from the extension module.

2.SCLP instruction is used for scaling the read data to our convinience.

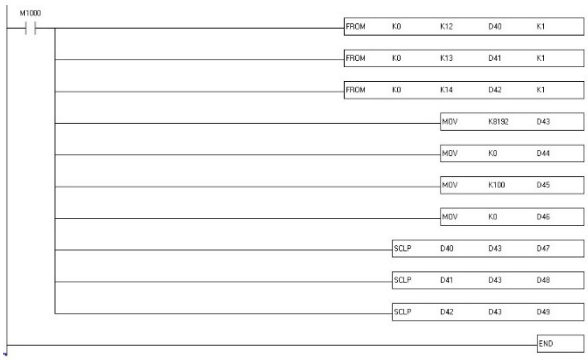

Figure 5. PLC Program

2.3 KEPServer

KEPServerEx falls under the category of a "Server" application. It is very common to hear the term "client/server application" in use across many software disciplines and business segments. In the industrial market, it has usually come to mean the sharing of manufacturing or production data between a variety of applications ranging from human machine interface software and data historians, to large MES and ERP applications.

Application of KEP server in Effluent Management system

KEP server is used in Effluent Management system as the interface between PLC and SCADA. And all the major communications settings and the interface between all the major components are provided using this application.

III. WORKING

MONITORING

For the data monitoring purposes, we use our SCADA screen developed for the project. SCADA (supervisory control and data acquisition) is a type of control system in software. Most of the control systems in industries are computer-controlled systems that monitor and control the real time processes in industries that exists in the physical world. SCADA systems steadily differentiate themselves from other control systems by being large scale processes that can include many numbers of sites and cover much distance. The type of PLC chosen here is Delta DVP 28 series SV.

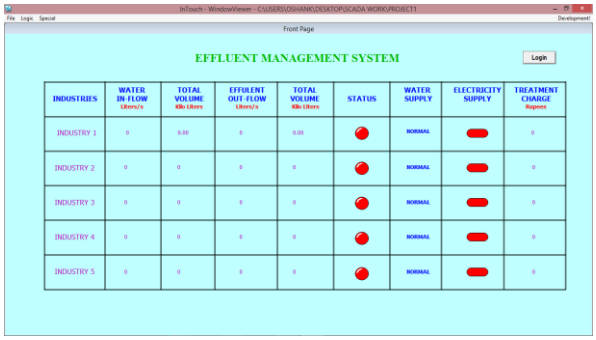

Figure 6. Data Monitoring Screen

The Figure 6 provides all the information about the water intake, outlet and Effluent across various industries. In our screen there are five industries whose water intake and outlet, monitoring has to be performed.

The monitoring of the industries is performed based on the input parameters predefined earlier. The screen shows the continuous intake of the water in terms of its flow and the whole of the water intake done by the industries. Which basically means the total quantity of water intake by the industries in kilo liter's. Now for the outlet, the screen shows the details of the flow of effluent and amount of effluent sent to the treatment plant in kilo liter's.

The status column indicates, whether the industry is functional or dormant. The red light indicates that the industry is not functional and whereas the green light indicates that the industry is functional.

The water supply status provides the information on how the industry is consuming the water. If the water supply status NORMAL, then the industry is consuming the water as per the limit provided to them. When the status of the industry turns to ABNORMAL, then it indicates that the industry is consuming water more that its limit. But this consumption of water is under tolerated level.

That is, an industry is provided with a limit to consume the water and a little more than that limit is tolerated. When the industry starts to consume even more than the tolerated level then the water supply status turns to BLOCKED.

The electricity column provides the status of industries current electricity supply. When the indication is green, it implies that the industry is provided with the electricity supply. When it turns to red, the electricity supply of the industry has been terminated either due to higher consumption of water or due to irregular electricity supply.

The treatment charge column, provides the information such as the necessary amount of money to be paid by the individual industry for the effluent treatment. The treatment value differs based on the value provided by the effluent treatment plant. The function of the monitoring screen is very simple. It just provides the information as per the data collected. And the changes are made accordingly in the screen. For further control, the concerned person who is responsible for the control must Login.

DATA ACQUISITION AND RESET.

Data acquisition is an essential task performed by the SCADA. In our project, the data acquisition is based on the limits set earlier. In the fig 4.2, we can set the limits for the inlet and outlet of the water. The screen works as follows. The industry can start its water intake at any time. But the outlet of the industry is displayed only after consuming the quantity of 1 Kilo liter's. The water at outlet is measured using outlet flow sensor and the water contamination level is checked using Salt sensor. When the limit of the salt sensor is reached, it represents the water contamination level. Thus, the outlet water doesn't stay in the industry, rather it is transferred to the effluent treatment plant.

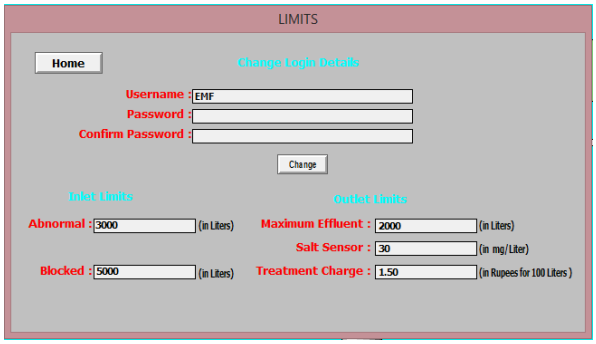

Figure 7. Limits Screen

In real time, the data's will be collected from the actual flow sensors and salt sensors. But in our project, we use potentiometers for representing the changes or to provide some variation. The tag name is allotted with the memory of the register in which the analog value of the potentiometer is obtained. This tag is connected to our PLC and SCADA using an interfacing software known as KEP Server. This software creates a path for accessing the register from both the software.

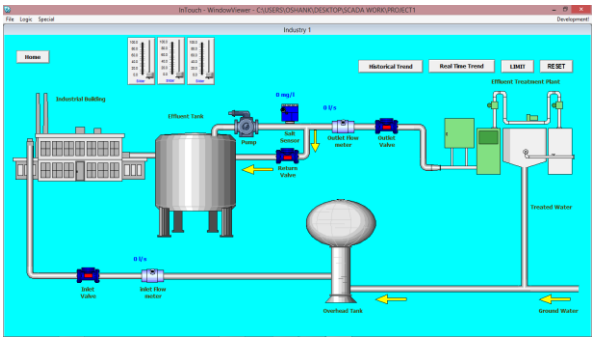

Figure 8. Reset control in INDUSTRY page

Well, the Fig 4.3 provides the details of the process happening in an industry. This screen resets itself for every 24 hours. And so, the industry can start its fresh water intake from the beginning of the next day. The data's such as industry's water intake, outlet, and the treatment charge for the effluent are the values that get reset at the end of every day.

AUTOMATIC AND MANUAL CONTROL

The automatic control is provided based on the limits provided earlier. But the controls can be done manual too. When the industry intakes a large quantity of water, exceeding the tolerated value. Then the electricity supply for the industry is terminated. This termination will only reset at the end of the day. But, when the industry makes a plea then the government has the authority to provide back the electricity to the industry. Thus, we provide a manual control for this purpose. The screen is fully automated and also provided with manual control.

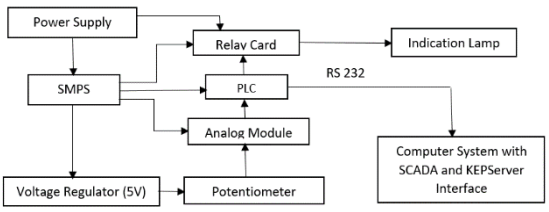

Figure 9. Block Diagram

The Figure 9 represents the block diagram of our system. The limits set once will always be set for further use. As the data are stored in retentive condition. The data's such as maximum effluent outlet, salt sensor value, treatment charge, abnormal state and blocked state are predefined once and the values

don't reset every day. These values can be used until the functioning of the screen. To provide any changes in those values, we can use the limits screen from the Industry page and the limits accordingly. This is manual changing of the limits as per the requirement. The electricity supply and also the excessive effluent flow to the treatment plant can also be provided manually by adjusting the limits. All these works are to be performed by the concerned personnel from the government point of view.

TREND MONITORING

TREND meter is based on standard measurements and data export methods. The TREND meter provides you with easy to read, graphed energy consumption and load information of each measured device. The TREND meter represents the starting point towards a more complex tool able to monitor a network infrastructure and to trigger energy saving techniques when traffic conditions change. Our tool has been developed inside the context of the European project TREND (Towards Real Energy Efficient Network design), which actually supported this work. The main goal of the TREND meter is to collect measurements of power and utilization from a variety of devices located in the Internet. The idea is to build a centralized server which collects the measurements from the devices. As second goal, the TREND meter aims at consolidating these measurements together to study whether there are similarities or not in the patterns of power and utilization of the devices. Additionally, the TREND meter aims at making publicly available the collected data to the community, and to easily show this information with a graphical representation. The design of TREND meter architecture had to face a complex and very heterogeneous scenario. The fig 3.5 shows the real time data monitoring.

Figure 10. Real Time Trend

SCADA is a high-performance trending application that supports real-time trending, historical trending and archival playback. The SCADA system has the ability to trend any real-time, calculated or application generated data value from the system database. The Trend Archiver has the ability to sample and periodically archive data as fast as every two seconds. Efficient compression techniques are used to save data to disk—and data is organized into monthly files which can be permanently archived onto external media for regulatory purposes.

SCADA TRENDS FEATURES

- ✓ Support for horizontal or vertical trending.
- ✓ Support for moveable crosshair for reading data values on a graph
- ✓ Scalable to all industrial manufacturing and infrastructure operations.
- ✓ Supports Business Continuity initiatives.
- ✓ Transforms the time-series process data into actionable information for faster, more accurate decision-making.

Figure 11. Historical Trend

The figure 11 shows the historical trend graphical representation of the overall process for the future

reference. The historical trending supports the storage of trend data for an unlimited period of time. Archived data can also be exported as CSV formatted files for supplementary analysis or for importing data into reports. In real time trending, the values that are monitored consecutively are represented in the form of graph at that particular instance. Whereas in historical trends features, it shows the range of values at a given instance. The real trends are mobile which means that its values change periodically. But for historical trends, it shows the range of values at particular instances for our referral view.

IV. RESULTS AND DISCUSSIONS

CONCLUSION

This project effectively promotes high portability and provides a simple way to monitor the process on the go. The proposed project is completely safe from unauthorized personnel as security username and password are provided to ensure process safety. Practically there would be a time delay in control which could be not more than few milliseconds. The main factor holding the project up straight is the modification and development which could be made possibly with available resources. By using automation based on PLC &SCADA we can increase productivity & also reduce monitoring based on humans done in dangerous environment. Benefit of replacing human for Monitoring and Data Acquisition in plant reduce operation time & increase consistency of output.

FUTURE SCOPE

This project can be modified based on the required condition and control can be made a lot easier. The processes could also be viewed in LabVIEW by making necessary interfacing works with the SCADA. The interfacing with LabVIEW is made to monitor the trends. It is also possible to view the process graphs, data's and desired specific parameters on an android device by developing an application dedicated for the process. With the usage of a GPRS module, this project can be a made lot more useful as it will provide long range data acquisition, data monitoring and process controlling.

APPLICATIONS

- ✓ This screen is used to monitor and control various Plant operations.
- ✓ It can be used by PWD of India for proper monitoring over various industries.
- ✓ It can be used wherever the supervisory control is necessary.
- ✓ It can be used in power plants, industries where data monitoring and control over long range is an absolute necessary.
- ✓ It can be used in Chemical process plants.

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National Conference on 'Innovative Research on Robotics, Circuits and Technology' (IRCT 2018)
Organized By : CIrcuit Branches of SCSVMV, (EEE, ECE, EIE & Mechatronics) , Kanchipuram, Tamil Nadu, India
In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Facial Marks Soft Biometric for Identification of Identical Twins ,Similar Faces, Sibblings in Face Recognition

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ABSTRACT

We propose to utilize micro features, namely facial marks (e.g., freckles, moles, and scars) to improve face recogni-tion and retrieval performance. This Facial marks are used to differentiate the identical twins and similar face and siblings. Facial marks can be used in three ways: i) to supplement the features in an existing face matcher, ii) to enable fast retrieval from a large database us-ing facial mark based queries, and iii) to enable matching or retrieval from a partial or profile face image with marks. We use Active Appearance Model (AAM) to locate and segment the local or primary facial features (e.g., eyes, nose, and mouth). Then, Laplacian-of-Gaussian (LoG) and morphological operators are used to detect facial marks. Experimental results based on FERET and Mugshot databases show that the use of facial marks improves the identification accuracy of a state-of-the-art face recognition system from 92.96% to 93.90% and from 91.88% to 93.14%, respectively.

Keywords: Face Recognition System, Facial Marks, Soft Bio-Metrics, Local Features, Active Appearance Model

I. INTRODUCTION

E2D Face recognition systems typically encode the human face by utilizing either local or global texture features. Local tech-niques first detect the individual components of the human face (viz., eyes, nose, mouth, chin, ears), prior to encoding the textural content of each of these components (e.g., EBGM and LFA) [12] [9]. Global (or holistic) techniques, on the other hand, consider the entire face as a single entity during encoding (e.g., PCA and LDA) [2]. However, both these tech-niques do not explicitly extract micro-features such as wrin-kles, scars, moles, and other distinguishing marks that may be present on the face (see Fig. 1). While many of these features are not permanent, some of them appear to be temporally in-variant, which can be useful for face recognition and index-ing. That is why we define facial marks as a soft biometric; while they cannot uniquely identify an individual, they can narrow down the search for an identity [4].

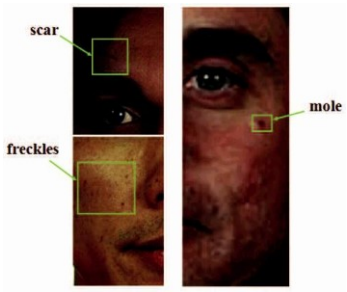


Figure 1. Facial marks: freckles (spots), mole, and scar.

Spaun [11] described the facial examination process car-ried out in the law enforcement agencies. One of

the examination steps involves identifying "class" and "individual" characteristics. The class characteristics include overall fa-cial shape, hair color, presence of facial hair, shape of the nose, presence of freckles, etc. The individual characteris-tics include number and location of freckles, scars, tattoos, chipped teeth, lip creases, number and location of wrinkles, etc. in a face or other body parts. While these examinations are currently performed manually by forensic experts, an au-tomatic procedure will not only reduce the manual labor, but is likely to be more consistent and accurate. This has inspired our work on automatic facial mark detection and matching.

There have been only a few studies reported in the lit-erature on utilizing facial marks. Lin et al. [6] first used the SIFT operator [8] to extract facial irregularities and then fused them with a global face matcher. Facial irregularities and skin texture were used as additional means of distinctiveness to achieve performance improvement. However, the individual types of facial mark were not explicitly defined. Hence, their approach is not suitable for face database indexing. Pierrard et al. [10] proposed a method to extract moles using normal-ized cross correlation method and a morphable model. They claimed that their method is pose and lighting invariant since it uses a 3D morphable model. However, they only explicitly utilized moles - other types of facial marks were ignored or implicitly used. Lee et al. [5] introduced "Scars, Marks, and Tattoos (SMT)" in their tattoo image retrieval system. While tattoos can exist on any body part and are more descriptive, facial marks are defined as marks on the face and they typically show simple morphologies.

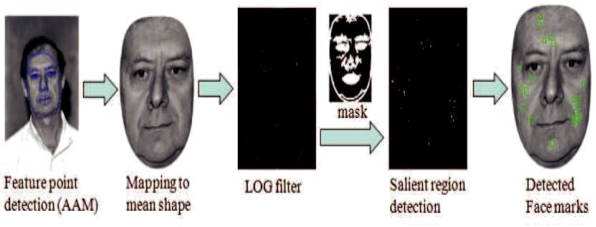


Figure 2. Schematic of automatic facial mark extraction process.

We propose a fully automatic facial mark extraction sys-tem using global and local texture analysis methods. We first apply the Active Appearance Model (AAM) to detect and re-move primary facial features such as eye brows, eyes, nose, and mouth. These primary facial features are subtracted from the face image. Then, the local irregularities are detected us-ing the Laplacian-of-Gaussian (LoG) operator. Finally, we combine these distinguishing marks with a commercial face matcher in order to enhance the face matching accuracy. Our method differs significantly from the previous studies in the following aspects: (a) we extract all types of facial marks that are locally salient and (b) we focus on detecting seman-tically meaningful facial marks rather than extracting texture patterns that implicitly include facial marks. The proposed facial mark extraction system will be useful to forensics and law enforcement agencies because it will (a) supplement ex-isting facial matchers to improve the identification accuracy,(b) enable fast face image retrieval, and (c) enable matching or retrieval from occluded, partial, or severely damaged face images.

II. FACIAL MARK DETECTION SYSTEM

The major categories of facial marks are defined as freckle, mole, scar, pockmark, acne, whitening, dark skin, abrasion, wrinkle, and others. All these facial marks appear as salient lo-calized regions on the face. Therefore, a blob detector based on Difference of Gaussian or Laplacian of Gaussian operator [7] can be used to detect the facial marks. However, a direct application of a blob detector on a face image will result in a large number of false positives because of the pri-mary facial features (e.g., eyes, eye brows, nose, and mouth). Currently, we do not distinguish between the individual mark categories. Instead, our focus is to automatically detect as many of these marks as possible. This facial marks used to distinguish between identical twins .The overall facial mark de-tection process is shown in Figure 2.

2.1. Local Facial Feature Detection

We have used Active Appearance Model (AAM) [3] to au-tomatically detect 133 landmarks that delineate the local or primary facial features: eyes, eye brows, nose, mouth, and face bound-ary (Figure 2). These primary facial features will be disregarded in the subsequent facial mark detection process.

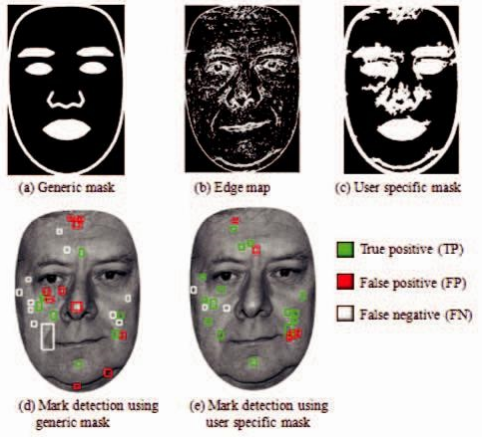


Figure 3. Effects of generic and user specific masks on facial mark detection. Both false negatives and false positives are decreased by using a user specific mask.

2.2. Mapping to Mean Image

Using the landmarks detected by AAM, we tightly crop each face image and map it to the mean shape to sim-plify the mark detection and matching process. Let S_i, i = 1, 2, . . . , N represent the shape of each face image based on the 133 landmarks. Then, the mean shape is simply

$$S_\mu = (1/N) \sum_{i=1}^{N} S_i .$$

Each face image, S_i, is mapped to the mean shape, S_μ, by using Barycentric coordinate based texture mapping process. In this way, all face images are nor-malized in terms of scale and rotation and allows us to use the Euclidean distance based matcher in facial mark matching.

2.3. Mask Construction

We construct a mask from the mean image, S_μ, to suppress false positives due to primary facial features in the blob de-tection process. The blob detection operator is applied to the face image mapped into the mean shape. A mask constructed from S_μ is used to suppress blob detection on the primary fa-cial features. Let the mask constructed from the mean shape be M_g, namely, a generic mask. Since the generic mask does not cover the user specific facial features such as beards or small winkles around eyes or mouth that increase the false positives, we build a user specific mask, M_s, using the edge image. The user specific mask M_s is constructed as a sum of M_g and edges that are connected to M_g. The effect of generic mask and user specific mask on mark detection is shown in Fig. 3. The user specific mask helps in removing most of the false positives appearing around the beard or small wrinkles around eyes or mouth.

2.4. Blob Detection Method

Facial marks mostly appear as isolated blobs. Therefore, we use the well-known blob detector, LoG operator, to detect fa-cial mark candidates. A 3×3 LoG kernel with $\sigma = \sqrt{2}$ is used. The LoG operator is usually applied at multiple scales to detect blobs of different sizes. However, we used a sin-gle scale LoG filter followed by a morphological operator (e.g., closing) to reduce the computation time. The LoG fil-tered image subtracted with the user specific mask un-dergoes a binarization process with a series of threshold values c_i, i = 1, . . . , K in a decreasing order. The threshold value c_0 is selected such that the resulting number of connected com-ponents is larger than n_0. A brightness constraint ($\geq b_0$) is also applied on each of the connected components to suppress false positives from weak blob responses. When the user spe-cific mask does not effectively remove sources of false pos-itives, true marks with lower contrast will be missed in the mark detection process. The overall procedure of facial mark detection is enumerated below.[1]

1. Facial landmark detection (AAM)
2. Mapping to the mean shape, S_μ
3. Construct user specific mask M_s
4. Apply LoG operator

5. Using threshold c_i , $i = 1, \ldots, K$, binarize and detect blobs (m_j) such that m_j does not overlap with M_s and the average brightness of $m_j \geq b_0$; stop if total #blobs$\geq n_0$
6. Encode each mark with a bounding box

2.5. Facial Mark Based MatchingTechnique

Given the facial marks, we compare their (x, y) coordinates in the mean shape space. A pair of marks, m_1 and m_2, is considered to match when $d(m_1, m_2) \leq t_0$, where $d(.,.)$ is the Euclidean distance. The number of matching marks is used as the matching score between two face images.

III. EXPERIMENTAL RESULTS

We used FERET and a Mugshot face database for evaluat-ing the proposed mark based matcher. FERET (Mugshot) database consists of 426 (1,225) images belonging to 213(671) different subjects, where 213 (554) of the subjects in the database have duplicate images[1]. The image size varies from 215×323 to 384×480 (width×height) for Mugshot and 512×768 for FERET both with 96 dpi resolution. We manu-ally labeled the ten facial mark types as defined in Sec. 2 in all the images to create the ground truth. This allows us to evaluate the proposed facial mark extraction method.

For the mark based matching, three different matching schemes are tested based on whether the ground truth or auto-matic method was used to extract the marks in the probe and gallery: i) ground truth (probe) to ground truth (gallery), ii) automatic (probe) to automatic (gallery), and iii) ground truth (probe) to automatic (gallery). Constructing ground truth for a large gallery database with millions of images is very time consuming and not feasible in practice. Therefore, using au-tomatically detected marks on the gallery database and the automatic or manually labeled marks on the individual probe image is more practical. The score-level fusion of a commer-cial face matcher, FaceVACS [1] and mark-based matcher is carried out using the weighted sum technique after min-max normalization of scores. The weights of the two matchers were selected empirically as 0.6 for FaceVACS and 0.4 for facial mark matcher.

Table 1. Face recognition accuracy using FaceVACS matcher, proposed facial mark matcher and their fusion.

Matcher	FERET (Rank-1)	Mugshot (Rank-1)
FaceVACS only	92.96%	91.88%
FaceVACS + Ground truth mark	93.90%	93.14%
FaceVACS + Automatic mark	93.43%	92.78%
FaceVACS + Ground truth (probe) & Automatic mark (gallery)	93.43%	93.14%

The precision and recall values for the mark detector with a range of brightness contrast thresholds b_0 (see Sec. 2.4) varies from (32%, 41%) to (38%, 16%) and from (30%, 60%) to (54%, 16%) for FERET and Mugshot, respectively. The rank-1 identification accuracies from FaceVACS only and the fusion of FaceVACS and marks are shown in Table 1 using b_0=200 and t_0=30. The range of parameter values tried are 200, 400, 600, 800, and 1,000 for b_0 and 10, 30, and 50 for t_0 to obtain the best recognition accuracy. Among the 213 (554) probe images, there are 15 (45) cases that fail to match at rank-1 using FaceVACS for FERET (Mugshot). Af-ter fusion, three (seven) out of

these 15 (45) failed probes are correctly matched at rank-1 for the ground truth (probe) to ground truth (gallery) matching in FERET (Mugshot). There is one case that was successfully matched before fusion but failed after fusion. Only one out of the 15 failed probes are correctly matched at rank-1 for the ground truth (probe) to automatic marks (gallery) matching. Example matching re-sults for FERET database are shown in Fig. 5. The 15 image pairs where FaceVACS failed to match at rank-1 contain rela-tively large pose variations. The examples in Fig. 5 that failed before fusion but succeeded after fusion contain at least four matching marks, which increases the final matching score af-ter fusion to successfully match the true image pairs at rank-1.The proposed mark extraction method is implemented in Matlab and takes about 15 sec. per face image. Mark based matching time is negligible.

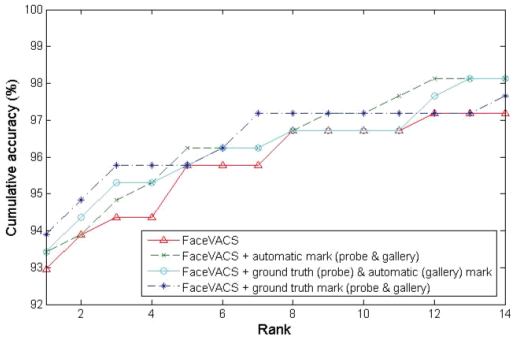
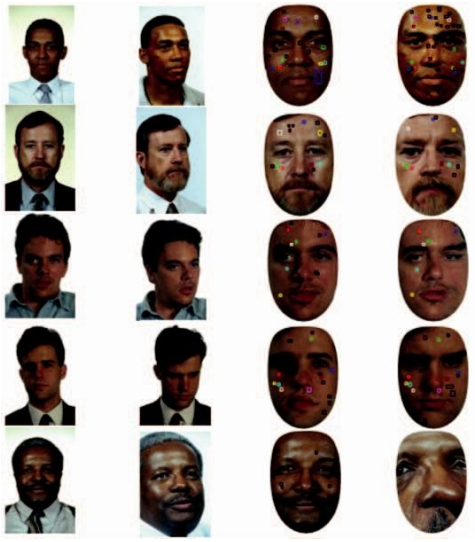


Figure 4. Cumulative Characteristic Matching Curve for FERET database



(a) probe (b) gallery (c) probe (mean shape) (d) gallery (mean shape)

Figure 5. First four rows shows example face image pairs that did not match correctly using FaceVACS but matched correctly after fusion with mark based matcher. Col-ored (black) boxes represent matched (unmatched) marks. The fifth row shows an example that matched correctly with FaceVACS but failed to match after fusion due to errors in facial landmark detection.

IV. SUMMARY AND FUTURE WORK

Facial marks (e.g., freckles, moles and scars) are salient lo-calized regions appearing on the face that have been shown to be useful in face recognition. An automatic facial mark extraction method has been developed that shows promising performance in terms of recall and precision. The fusion of facial marks with a state-of-the-art face matcher (FaceVACS) improves the face recognition performance on a public domain as well as an operational database. This demonstrates that micro-level features such as facial marks do offer some discriminating information. Most of the facial marks detected are semantically meaningful, so users can issue queries to re-trieve images of interest from a large database Future work includes (i) improving the facial mark detection accuracy to enable the face mark based image retrieval, ii) improving the mark based matching accuracy (iii) extending the mark detection process to partial or damaged face images.(iv)improving the distinguish between identical twins and similar faces and siblings

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

A Study of Face Recognition Performance Under Aging

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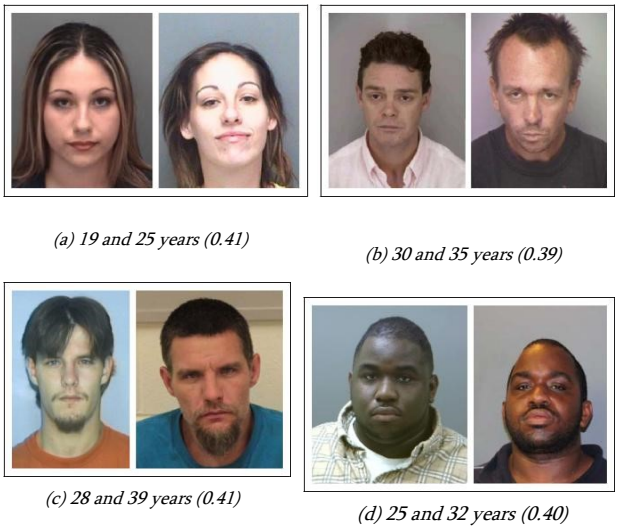
ABSTRACT

In the face recognition technology into important identity applications, it is imperative that the ef-fects of facial aging on face recognition performance are thoroughly understood. As face recognition systems evolve and improve, they should be periodically re-evaluated on large-scale face datasets. In our study, we evaluate the performance of two state-of-the-art commer-cial off the shelf (COTS) face recognition systems on two large-scale longitudinal datasets of mugshots of repeat of-fenders. We fit multi-level statistical models to genuine comparison scores (simi-larity between images of the same face) from the two COTS face matchers. In Accuracy of

Face recognition performance due to elapsed time between a probe (query) and its enrollment (gallery) image. We ac-count for face image quality to obtain a better estimate of trends due to aging, and analyze whether longitudinal trends in genuine scores differ by subject gender and race. Based on the results of our statistical model, we infer that the state-of-the-art COTS matchers can verify 99% of the subjects at a false accept rate (FAR) of 0.01% for up to 10.5 and 8.5 years of elapsed time. Beyond this time lapse of 8.5 years, there is a significant loss in face recognition accu-racy.



(a) 19 and 25 years (0.41) *(b) 30 and 35 years (0.39)*

(c) 28 and 39 years (0.41) *(d) 25 and 32 years (0.40)*

Figure 1: Examples of low-scoring genuine face image pairs of four sub-jects from (a), (b) PCSO and (c), (d) MSP longitudinal mugshot datasets. Ages at image acquisitions are given along with similarity scores from COTS-A for each pair. The thresholds for COTS-A at 0.1% and 0.01% false accept rate (FAR) are 0.42 and 0.49, respectively, for both PCSO and MSP datasets. Each of the genuine pairs would be falsely rejected at 0.1% and 0.01% FARs.

facial hair, etc. Figure 1 shows that large time lapse between two genuine face images can result in false reject errors. Therefore, it is critical to systematically evaluate face recognition technology on longitudinal face datasets to determine state-of-the-art accuracy with respect to time lapse between a probe and its enrollment image in the gallery.

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

1. Introduction

It is now well established that accuracies of face recog-nition systems are adversely affected by factors including facial pose, illumination, expression and aging, collectively known as PIE-A. While image acquisition conditions and subject cooperation can accommodate for PIE variations in controlled capture scenarios, facial aging factors are intrin-sic and cannot be controlled. A face undergoes various temporal changes across time, including wrinkles, weight,

A considerable amount of research has been performed and reported on age-invariant face recognition [6],[7], syn-thetic aging [8],[9], automatic age estimation from face im-ages [10], aging analysis [11], and appearance prediction across ages [12]. In this study, we focus on quantifying the impact of aging on the performance of face recognition sys-tems. Studies within this realm traditionally have followed a methodology of dividing a given population into discrete age groups and then reporting recognition performance (*e.g.* TAR or EER) for each age group independently. Two major conclusions have been drawn based on this cross-sectional analysis: (i) Face recognition performance decreases as the elapsed time between two images of the same subject in-creases [1], [3], [4], and (ii) faces of younger individuals are more difficult to recognize than faces of older individ-uals [4],[5]. Studies, where arbitrary age group assignment are considered, make it difficult to compare results from dif-ferent studies. Additionally, the primary concern with facial aging is a decrease in *genuine* similarity scores over time lapse, which causes an increase in false non-match rates. Reporting summary performance measures for subsets of a facial aging dataset does not provide any insight into how the genuine similarity scores of individuals are changing over time. Previous facial aging studies [19] primarily used FG-NET [17] and MORPH [18] face datasets, which are both limited in terms of the number of subjects and number of images per subject. FG-NET contains only 1,002 images from 82 subjects and MORPH contains only 317 subjects that have at least 5 images over at least 5 years time lapse. Due to their small size, both in terms of number of subjects and number of images per subject over time, FG-NET and MORPH are not suitable for statistical modeling for longi-tudinal study. For this study, we obtained two large-scale longitudinal face datasets, denoted as PCSO and MSP (see Table 1) and report our inference based on these datasets. While these two datasets, due to privacy issues, are not available in the public domain, there is no way to carry out a meaningful longitudinal study without such large-scale data that is only available from government agencies.

Multilevel statistical models have been adopted for large-scale longitudinal study of iris [13], fingerprint [16], and face [2] recognition. Grother *et al.* analyzed a large-scale longitudinal dataset of 7,876 subjects to quantify the iris ag-ing effect on recognition over time in a study called IREX VI [13]. They concluded that an increase in Hamming distance due to elapsed time between enrolled and query images has no significant effect on iris recognition fail-ures. Some limitations of the IREX VI study were iden-tified [14], [15]. Yoon and Jain analyzed a longitudinal fingerprint dataset of 15,597 subjects and found a decreas-ing trend in genuine match scores; however, the recog-nition accuracy, at operational FARs between 0.01% and 0.00001%, remained stable up to 12 years (the maximum time span in the dataset) [16]. Best-Rowden and Jain per-formed a subject-specific analysis using two longitudinal face datasets: PCSO dataset containing 147,784 images of 18,007 subjects and LEO dataset[1] containing 31,852 images of 5,636 subjects [2]. Best-Rowden and Jain concluded:
(i) while genuine scores declined significantly over time, scores for 99% of the population remained above the thresh-old at FAR of 0.01% (0.1%) until 6.5 (8.5) and 5.5 (8.0) years of elapsed time for PCSO and LEO datasets, respec-tively, and (ii) subject demographics had marginal effects on the rates of change in genuine scores over time. Because these results are tied to the particular COTS face matchers used in [2], it is imperative to periodically repeat the lon-gitudinal study utilizing new and improved face matchers as they evolve, as well as additional large-scale longitudinal datasets.

This paper repeats and expands on the longitudinal face study in [2]. The contributions of this paper are as follows:

- Evaluate the performance of two state-of-the-art COTS face matchers (COTS-A and COTS-B)[2] on two longi-tudinal mugshot datasets (PCSO and MSP)[3] from two different law enforcement sources. COTS-A is a new version from the same vendor of the COTS-A face matcher used in [2].
- PCSO and MSP datasets used in this study are the largest longitudinal face datasets studied to date. See Table 1 for details on PCSO and MSP datasets.
- Analyze the rate of change in genuine scores due to the elapsed time between enrollment and probe images, as well as covariates such as gender, race, and the quality of the gallery and probe images.

The key differences between this study and [2] are:

- A newer version of the COTS-A face matcher is uti-lized with significantly improved face recognition per-formance.
- Evaluation of COTS-A on both PCSO and MSP datasets, and evaluation of COTS-A and COTS-B on

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MSP. In contrast, [2] evaluated two matchers, each on only a single dataset.

- While [2] used inter-pupillary distance (IPD) and face frontalness as quality measures, we utilize an over-all face quality measure, namely, Rank-based Quality Score (RQS) proposed by Chen *et al*. [20].

The organization of the paper is as follows. Section 2 de-scribes the two large-scale longitudinal datasets (PCSO and MSP) used in this study. In Section 3, we revisit the multi-level statistical models from [2]. Section 4 makes inferences from fitting the models on genuine scores from COTS-A and COTS-B. Section 5 summarizes and concludes our pa-per.

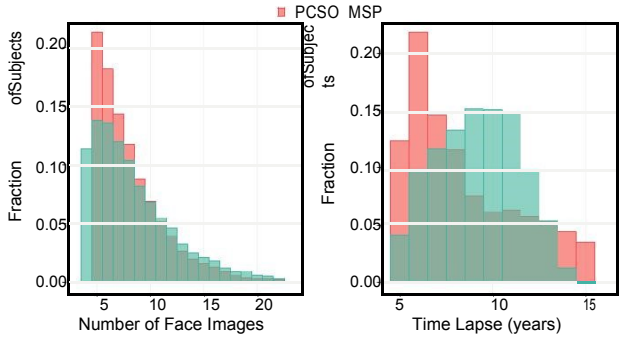

Figure 2: Statistics of the two longitudinal face datasets used in this study (PCSO and MSP). Histograms denote the number of face images per sub-ject, and show the time lapse between the enrollment and the latest probe image of a subject. PCSO dataset contains 147,784 face images of 18,007 subjects and MSP dataset contains 82,450 images of 9,572 subjects.

2. Multilevel Statistical Model

The large-scale longitudinal datasets described in Section 2 contain repeated observations (face acquisitions and, consequently, genuine scores) for each subject over time. Additionally, the datasets are both time-unstructured ($T_{i,k} = T_{j,k}$) and unbalanced ($N_i = N_j$). To study such hierarchical data, multilevel (or mixed-effects) statistical models have been widely used to evaluate the correlation of within-subject response variables across time in many important fields of research including epidemiology, soci-ology, psychology, etc.

Table 1: Statistics of PCSO and MSP datasets.

	PCSO	MSP
Number of Images	147,784	82,450
Number of Subjects	18,007	9,572
Average no. of images/subject	8	9
Max no. of images/subject	60	48
Average time lapse (years)	8.5	9.0
Max time span (years)	16	14
Average age of subjects (years)	31	33
Youngest age of subject (years)	18	18
Oldest age of subject (years)	83	78
Male/Female ratio (%)	83/17	88/12
Black/White ratio (%)	61/39	52/48
Average IPD (pixels)	113	126

The models used in this work contain two levels, simi-lar to those used in [2]. The Level-1 model describes the changes in genuine scores, Y_{ij} , for each subject over time (within-subject variation), whereas the Level-2 model de-scribes how these changes differ across subjects (between-subject variation). Genuine scores are standardized using z-score normalization so that coefficients obtained from the models are interpreted as the change in standard deviations of the genuine distribution per year (e.g. for elapsed time covariate). The genuine score distributions for COTS-A on PCSO and MSP and COTS-B on MSP datasets are shown in Figure 3. We model changes in genuine scores over time, $Y_{i,j}$, as a linear function of various covariates, $X_{i,j}$,

$$Y_{i,j} = \pi_{0i} + \pi_{1i} X_{i,j} + \varepsilon_{i,j} , \quad (1)$$

where π_{0i} and π_{1i} are subject i's intercept and slope, re-spectively. Equation 1 is the Level-1 model which corre-sponds to within-subject changes in face comparison scores over time. The Level-1 residual variation, $\varepsilon_{i,j}$, represents the variance in each individual's comparison scores from his/her linear longitudinal trend. The slope and intercept parameters, π_{0i} and π_{1i}, are modeled as a combination of fixed and random effects. Fixed effects, γ_{00} and γ_{10}, are the overall means of the population intercepts and slopes, whereas random effects, b_{0i} and b_{1i}, are subject i's devia-tion from the population means. Therefore, subject i's slope and intercept parameters can be written as,

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Table 2: Multilevel models with different covariates

Model	Level-1 Model	Level-2 Model	Covariates
Model B_T	$Y_{ij} = \pi_{0i} + \pi_{1i} T_{i,j} + \varepsilon_{i,j}$	$\pi_{0i} = \gamma_{00} + b_{0i}$, $\pi_{1i} = \gamma_{10} + b_{1i}$	Time lapse
Model C_{GR}	$Y_{ij} = \pi_{0i} + \pi_{1i} T_{i,j} + \varepsilon_{i,j}$	$\pi_{0i} = \gamma_{00} + \gamma_{01}Gend_i + \gamma_{02}Race_i + b_{0i}$ $\pi_{1i} = \gamma_{10} + \gamma_{11}Gend_i + \gamma_{12}Race_i + b_{1i}$	Time lapse, gender, and race
Model Q_T	$Y_{ij} = \pi_{0i} + \pi_{1i} T_{i,j} + \pi_{2i} Qual_{i,jj=1} + \pi_{3i} T_{i,j} Qual_{i,jj=1} + \varepsilon_{i,j}$	$\pi_{0i} = \gamma_{00} + \gamma_{01}Qual_{i,1} + b_{0i}$ $\pi_{1i} = \gamma_{10} + \gamma_{11}Qual_{i,1} + b_{1i}$ $\pi_{2i} = \gamma_{20} + \gamma_{21}Qual_{i,1}$ $\pi_{3i} = \gamma_{30} + \gamma_{31}Qual_{i,1}$	Time lapse, quality

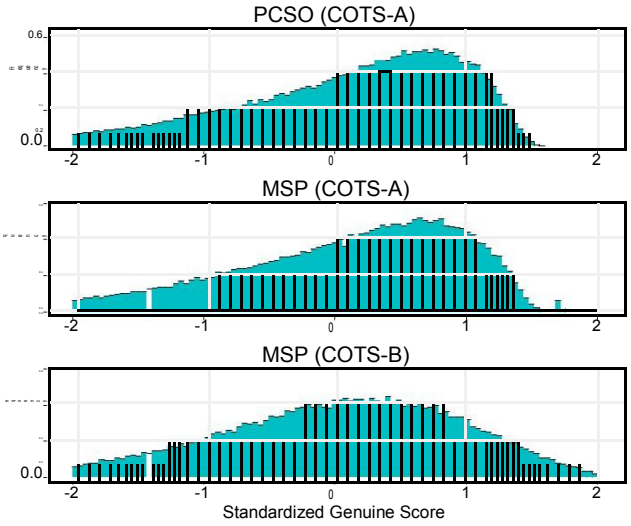
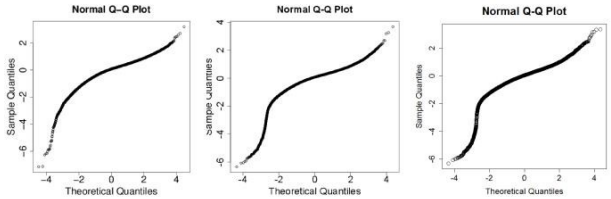


Figure 3: Genuine score distributions for (top to bottom) COTS-A on PCSO, COTS-A on MSP, and COTS-B on MSP datasets.



(a) COTS-A (PCSO dataset) (b) COTS-A (MSP dataset) (c) COTS-B (MSP dataset)

Figure 4: Normal probability plots for level-1 residuals ε_{ij} from Model B_T fit to COTS-A on (a) PCSO and (b) MSP and COTS-B on (c) MSP genuine scores.

$$\pi_{0i} = \gamma_{00} + b_{0i}, \quad (2a)$$

$$\pi_{1i} = \gamma_{10} + b_{1i}. \quad (2b)$$

Equations 2a and 2b constitute the Level-2 model which models changes in face comparison scores across subjects. Equations 1 and 2 can be combined to get,

$$Y_{ij} = [\gamma_{00} + b_{0i}] + [\gamma_{10} + b_{1i}] X_{i,j} + \varepsilon_{i,j}. \quad (3)$$

If the random effects and residual variation are equal to their expected means of zero, then Equation 3 reduces to the population-mean trend $Y_{ij} = \gamma_{00} + \gamma_{10} X_{i,j}$.

The different covariates incorporated in the models are as follows:

- $T_{i,j}$: time lapse between the jth image acquisition and the enrollment face image of subject i
- $Gend_i$: gender of subject i (0 for female, 1 for male)
- $Race_i$: race of subject i (0 for black, 1 for white)
- $Qual_{i,j}$: face quality metric for jth mugshot image of subject i. Face quality values used here are obtained from the methodology proposed by Chen *et al*. [20]. $Qual_{i,1}$ is the face quality value for enrollment image and $Qual_{i,jj=1}$ is the quality value for the jth probe image of subject i.

Note that $T_{i,j}$ and $Qual_{i,j}$ $_{j=1}$ are time-varying covariates and affect within-subject variation in genuine scores (Level-1). On the other hand, $Age_{i,1}$, $Gend_i$, $Race_i$, and $Qual_{i,1}$ are time-invariant covariates and affect between-subject variation in genuine scores (Level-2). Table 2 describes all models and covariates used in this study.

- $Age_{i,1}$: age at enrollment of subject i

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Table 3: Bootstrap parameter estimates of fixed-effects and variance components for COTS-A on PCSO and MSP datasets and COTS-B on MSP dataset. Estimates where the 95% bootstrap confidence intervals contained zero are highlighted in bold

	PCSO (COTS-A)			MSP (COTS-A)			MSP (COTS-B)		
	B_T	$\breve{}_{GR}$	Q_T	B_T	$\breve{}_{GR}$	Q_T	B_T	$\breve{}_{GR}$	Q_T
γ_{00}	0.7233	0.3958	0.6889	0.5858	0.4914	0.5059	0.5599	0.6847	0.4647
γ_{10}	-0.1429	-0.1170	-0.1399	-0.1076	-0.1006	-0.0945	-0.1036	(-0.0849)	-0.0899
γ_{01}		0.4286	0.0595		0.1665	0.1173		0.0424	0.1762
γ_{11}		-0.0087	0.0067		(0.0078)	-0.0029		(-0.0084)	-0.0058
γ_{02}		-0.0433	0.0858		-0.0929	0.1900		-0.3128	0.2408
γ_{12}		-0.0308	0.0069		-0.0291	0.0104		-0.0251	0.0056
γ_{20}			0.0605			0.0833			0.1380
γ_{21}			(-0.0002)			(-0.0001)			-0.0064
σ^2	0.2951	0.2955	0.2587	0.5300	0.5230	0.3878	0.5218	0.5065	0.4034
σ_0^2	0.2465	0.2202	0.2322	0.4338	0.4232	0.3878	0.5878	0.5547	0.5258
σ^2_1	0.0036	0.0033	0.0032	0.0081	0.0077	0.0067	0.0080	0.0072	0.0068
σ_{01}	-0.0020	-0.0017	-0.0026	-0.0367	-0.0356	-0.0305	-0.0470	-0.0447	-0.0425
AIC	254659	252696	246185	178710	177435	162928	177703	174684	163758
BIC	254717	252794	246371	178765	177527	163103	177758	174776	163932
Deviance	254647	252676	246147	178699	177415	162890	177691	174664	163720

3. Experimental Results

Genuine scores from COTS-A and COTS-B were obtained by comparing each subject's enrollment image (youngest acquisition) to his/her subsequent face images. Hence, for subject i, there are $(N_i - 1)$ genuine compar-isons. For PCSO dataset, there are a total of 130,878 gen-uine and 11.1 billion impostor comparison scores, whereas, for MSP da

taset, there are 82,150 genuine and 4.1 billion impostor comparison scores. Increasingly complex mod-els (Table 2) are successively fit to evaluate the variation in genuine scores over time and the impact of additional co-variates. Models were fit using the LME4 package in R using maximum likelihood estimation. Thresholds at dif-ferent FAR values are calculated from the full impostor dis-tributions in order to evaluate how the longitudinal trends in genuine scores affect the recognition accuracies of COTS-A and COTS-B.

Inferences from multilevel models are based on the assumption that the residual errors are normally distributed. Figure 4 shows the normal probability plots (Q-Q plots) of the residuals, $\varepsilon_{i,j}$, from fitting Model B_T to genuine scores. For both datasets, linearity is violated, indicating that the validity of normality assumption does not hold. When parametric model assumptions are violated, non-parametric bootstrap can be performed to obtain confidence intervals for the parameter estimates [16]. Therefore, non-parametric bootstrapping is conducted with 1,000 bootstrap sets, obtained by sampling 18,007 and 9,572 subjects with replacement from PCSO and MSP, respectively. The multilevel models are then fit to each bootstrap set, and the mean parameter estimates over all 1,000 bootstraps are reported. Table 3 gives parameter estimates and variances obtained from the models after bootstrapping; 95% bootstrap confidence intervals have been omitted due to space, but parameters for which confidence intervals contained zero are indicated in bold. These parameters are statistically zero and the null hypothesis of the parameter equal to 0 cannot be rejected at significance level of 0.05.

Model B_T contains a single covariate, namely the time lapse between a subject's enrollment image and probe images ($T_{i,j}$). The population-mean trend for Model B_T , given by γ_{00} and γ_{10}, estimates that COTS-A genuine scores decrease by γ_{10} = 0.1429 and 0.1076 standard deviations per year for PCSO and MSP datasets, respectively. Similar to COTS-A on MSP, Model B_T estimates that COTS-B genuine scores from MSP decrease by 0.1036 standard deviations per year. In other words, this implies that COTS-A genuine scores decrease by one full stan-dard deviation of the PCSO (MSP) score distribution after $1/\gamma_{10}$ = 7.0 (9.3) years of elapsed time. Again, similar to COTS-A on MSP, COTS-B genuine scores decrease by one full standard deviation of the MSP score distribution after $1/\gamma_{10}$ = 9.7 years of elapsed time.

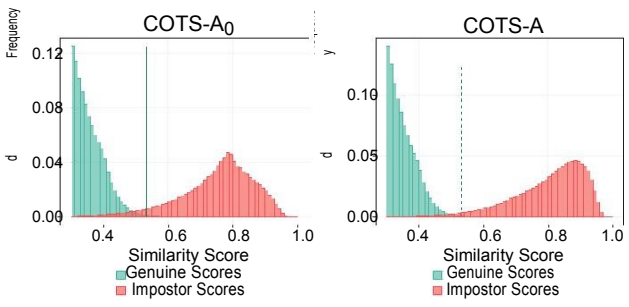

Figure 5: Genuine score distributions for (a) COTS-A_0 and (b) COTS-A face matchers. Thresholds at 0.01% FAR for COTS-A_0 and COTS-A face matchers are 0.53 and 0.49, respectively. The thresholds are shown with dashed lines.

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Table 4: Bootstrap parameter estimates of fixed-effects and variance components from Model B_T for COTS-A_0 and COTS-A on PCSO dataset

		COTS-A_0 [2]	COTS-A
intercept	γ_{00}	0.6734	0.7233
slope	γ_{01}	-0.1364	-0.1429
	σ^2	0.3912	0.2951
	σ_0^2	0.3243	0.2465
	σ_1^2	0.0028	0.0036
	σ_{01}	-0.0039	-0.0020

† COTS-A_0 is the older version of COTS-A face matcher used by Best-Rowden and Jain [2].

Table 4 compares the longitudinal performance on PCSO of the COTS-A face matcher with the previous version of

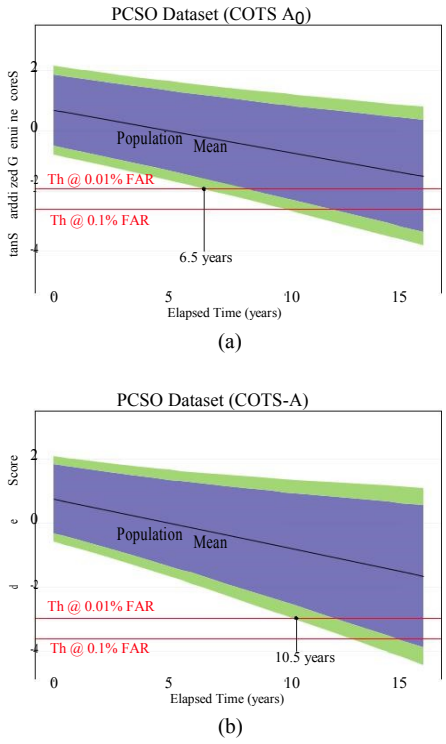

Figure 6: Results from Model B_T on (a) COTS-A_0 and (b) COTS-A match scores on PCSO dataset. The blue and green bands plot regions of 95% and 99% confidence for subject-specific variations around the population-mean trend. Hence, Model B_T estimates that 95% and 99% of the subject trends fall within the blue and green bands. Thresholds at 0.01% and 0.1% FAR for COTS-A_0 and COTS-A are shown as red lines.

COTS-A, denoted as COTS-A_0, used in [2]. The estimated slopes from Model B_T for COTS-A_0 and COTS-A indi-cate that genuine scores decrease by one standard deviation of their respective genuine distributions after 7.3 and 6.9 years of elapsed time, respectively. These two estimates are fairly close for the two versions of COTS-A, but suggest that COTS-A_0 may be slightly more robust to aging.

Following [2], using estimated variation in slope and intercept parameters (σ_0^2, σ_1^2, and σ_{01}), we plot regions that contain the longitudinal trends for 95% and 99% of the population. The regions are then used to determine when genuine scores for 95% and 99% of the population begin to drop below thresholds for FARs of 0.01% and 0.1%. In other words, we estimate the elapsed time in years which is tolerated by the COTS matchers before the decrease in genuine scores begins to cause errors at different FARs. Best-Rowden and Jain reported that genuine scores for 99% of the population remained above the threshold at 0.01% FAR until 6.5 years for COTS-A_0 on the PCSO dataset, whereas, from Figure 6, we estimate this time lapse to be 10.5 years for COTS-A. Figure 5 shows that the score distribution for COTS-A face matcher has a better separation between impostor and genuine score distributions, compared to COTS-

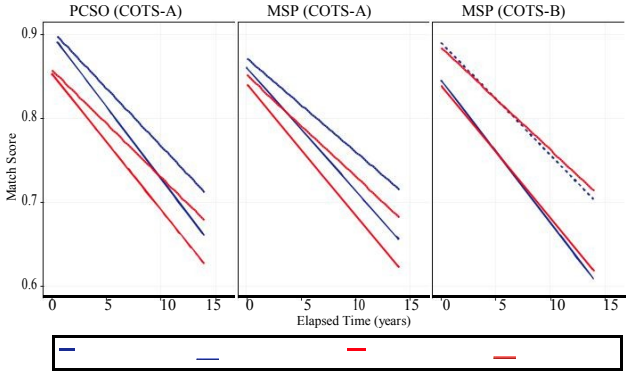

Figure 7: Population-mean trends in COTS-A and COTS-B genuine scores on PCSO dataset and MSP dataset for the four demographic groups in the datasets. Trends were obtained from Model C_{GR}.

A_0, due to lower thresholds at different FARs and a shift in the entire genuine distribution, which can accommodate more for decreasing genuine scores. This may explain the improved longitudinal performance of COTS-A compared to COTS A_0.

From Figure 6, we find a significant amount of variability in subject-specific longitudinal trends in COTS-A genuine scores on PCSO dataset over time. We observed that large subject-specific variability exists for COTS-A and COTS-B on MSP dataset as well. Therefore, we consider other covariates such as gender and race, and face image quality to further explain this variability and to obtain a better estimate of longitudinal trends due to face aging.

4. Conclusions

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In this paper performance accuracy of f face recognition, using two operational large face datasets of mugshot images, PCSO (147,784 mugshots of 18,007 sub-jects, 8 images per subject on average over an average time lapse of 8 years) and MSP (82,450 images of 9,572 sub-jects, 9 images per subject on average over an average time lapse of 9 years). Each subject has at least 5 and 4 im-ages for PCSO and MSP, respectively, acquired over a time lapse of at least 5 years. Multilevel statistical models were used to analyze variations in genuine scores due to covari-ates such as time lapse, gender, race, and face quality. Face similarity scores were obtained from state-of-the-art face matcher, COTS-A, for both PCSO and MSP dataset and another state-of-the-art face matcher, deep-network based COTS-B, on MSP dataset. Based on the results of our statistical model, we infer that the state-of-the-art COTS matchers can verify 99% of the subjects at a false accept rate (FAR) of 0.01% for up to 10.5 and 8.5 years of elapsed time. Beyond this time lapse of 8.5 years, there is a significant loss in face recognition accu-racy.

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Statistical Ratio Analysis and Overview of Growth in Power Energy System in India

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ABSTRACT

An analysis of statistical ratio, overview of growth in power energy system in India is done here. An installed capacity of 330.86 GW as on 2017 in utility electricity sector has one National Grid. In power generation of the country has various aspects using coal, gas and diesel in thermal power plant. The renewable energy system has been generated using the power of hydro, solar and wind sources. Using the source of uranium the nuclear power generation system is also produced. By applying the five year plan customized in the country a new power generating system are installed. The generated power was consumed for various purposes such as domestic, commercial, industrial, traction, agriculture and others. An average statistical study of increase in power system in the last few decades is represented by the graphical form.

Keywords: Power Sector, Energy Audit, Restructuring, Deregulation, Distributed Generation, Non conventional renewable energy, Central Electricity Authority (CEA).

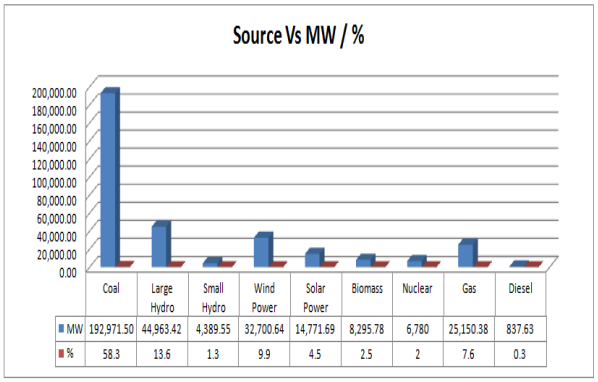
I. INTRODUCTION

The total capacity of power plant installed can be categorized as non- renewable energy and renewable energy. The power plant of renewable energy contributes 32% in the generation of total power system. Recently renewable energy systems are gradually used for electricity generation. A renewable energy technology does not demand any fossil fuel. Their action is only based on the utilizing of natural resources such as wind, solar, hydro power, biomass and geothermal. The consumption and generation of the energy using renewable sources are applied in many places such as industries, home and offices. The generation of renewable energy mainly depends on the nature resources availability of the country. The need of generation of power supply using renewable energy system is an emergency growth to reduce the environmentally pollution done by non-renewable power system.

The progress in power generation sector of the country is extraordinary after independence. At present the whole capacity of the generated power system is about 1,236.39 TWh were it was only 1362 MW at the time of independence. A rapid increase in the generation of the power system due to increase in the consumption of the power source. The development of the country also depends on the production of power sources so as to satisfy the total consumption of the population. The following various corporations sectors were involved in the power system generation as State Electricity Boards (SEB), National Thermal Power Corporation (NTPC),

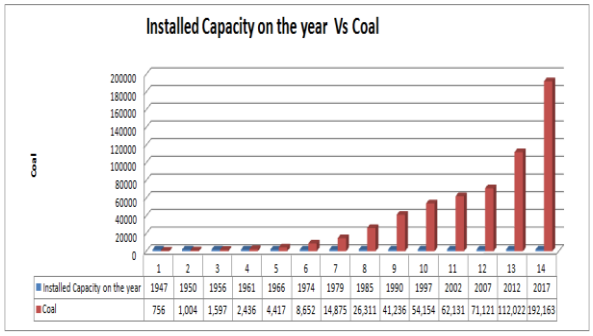
National Hydro-Electric Power Corporation (NHPC) and Power Grid Corporation Limited (PGCL) etc.

The installed Capacity by source as on 31st November 2017 as shown in Figure 1



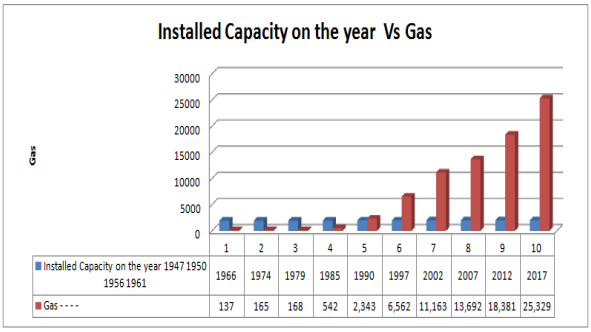
	Coal	Large Hydro	Small Hydro	Wind Power	Solar Power	Biomass	Nuclear	Gas	Diesel
MW	192,971.50	44,963.42	4,389.55	32,700.64	14,771.69	8,295.78	6,780	25,150.38	837.63
%	58.3	13.6	1.3	9.9	4.5	2.5	2	7.6	0.3

Figure 1. Source Vs Mega Watts and Percentage of source



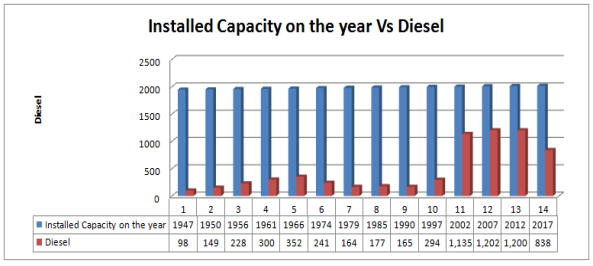
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Installed Capacity on the year	1947	1950	1956	1961	1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Coal	756	1,004	1,597	2,436	4,417	8,652	14,875	26,311	41,236	54,154	62,131	71,121	112,022	192,163

Figure 2. Installed Capacity on the year Vs Coal



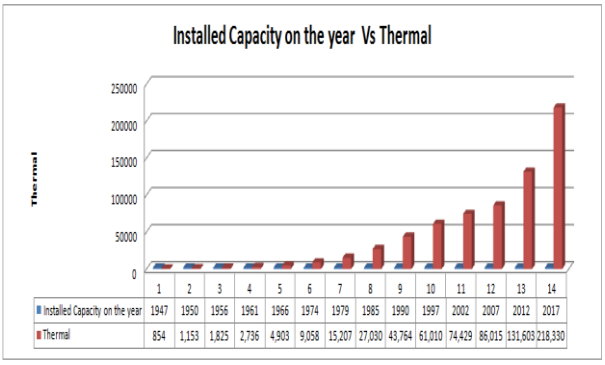
	1	2	3	4	5	6	7	8	9	10
Installed Capacity on the year 1947 1950 1956 1961	1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Gas	137	165	168	542	2,343	6,562	11,163	13,692	18,381	25,329

Figure 3. Installed Capacity on the year Vs Gas



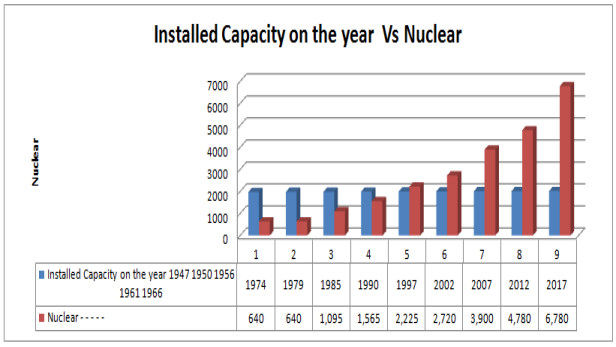
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Installed Capacity on the year	1947	1950	1956	1961	1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Diesel	98	149	228	300	352	241	164	177	165	294	1,135	1,202	1,200	838

Figure 4. Installed Capacity on the year Vs Diesel



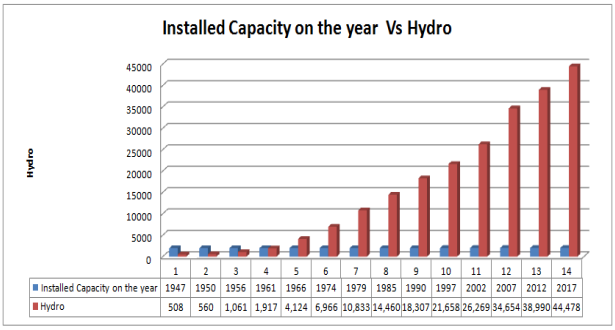
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Installed Capacity on the year	1947	1950	1956	1961	1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Thermal	854	1,153	1,825	2,736	4,903	9,058	15,207	27,030	43,764	61,010	74,429	86,015	131,603	218,330

Figure 5. Installed Capacity on the year Vs Thermal



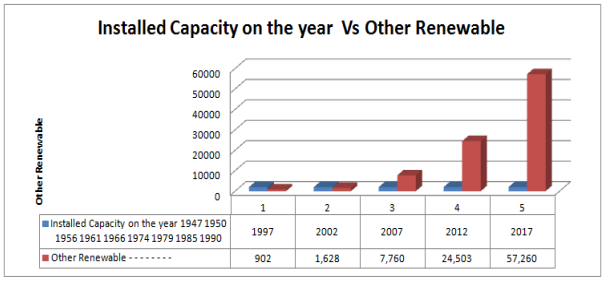
	1	2	3	4	5	6	7	8	9
Installed Capacity on the year 1947 1950 1956 1961 1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Nuclear	640	640	1,095	1,565	2,225	2,720	3,900	4,780	6,780

Figure 6. Installed Capacity on the year Vs Nuclear



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Installed Capacity on the year	1947	1950	1956	1961	1966	1974	1979	1985	1990	1997	2002	2007	2012	2017
Hydro	508	560	1,061	1,917	4,124	6,966	10,833	14,460	18,307	21,658	26,269	34,654	38,990	44,478

Figure 7. Installed Capacity on the year Vs Hydro



	1	2	3	4	5
Installed Capacity on the year 1947 1950 1956 1961 1966 1974 1979 1985 1990	1997	2002	2007	2012	2017
Other Renewable	902	1,628	7,760	24,503	57,260

Figure 8. Installed Capacity on the year Vs Other Renewable

The Table 1 is shows the growth of installed capacity in our country.

Table 1. Growth of Installed Capacity in our country

Installed Capacity as on	Thermal (MW)				Nuclear (MW)	Renewable (MW)			Total (MW)	% Growth (on yearly basis)
	Coal	Gas	Diesel	Sub – Total Thermal		Hydro	Other Renewable	Sub-Total Renewable		
31-Dec-1947	756	-	98	854	-	508	-	508	1,362	-
31-Dec-1950	1,004	-	149	1,153	-	560	-	560	1,713	8.59%
31-Mar-1956	1,597	-	228	1,825	-	1,061	-	1,061	2,886	13.04%
31-Mar-1961	2,436	-	300	2,736	-	1,917	-	1,917	4,653	12.25%
31-Mar-1966	4,417	137	352	4,903	-	4,124	-	4,124	9,027	18.80%
31-Mar-1974	8,652	165	241	9,058	640	6,966	-	6,966	16,664	10.58%
31-Mar-1979	14,875	168	164	15,207	640	10,833	-	10,833	26,680	12.02%
31-Mar-1985	26,311	542	177	27,030	1,095	14,460	-	14,460	42,585	9.94%
31-Mar-1990	41,236	2,343	165	43,764	1,565	18,307	-	18,307	63,636	9.89%

The Table –II is shown the Total installed utility power generation capacity as on 2017 with sector wise & type wise break up

Table 2. (Total installed utility power generation capacity as on 2017 with sector wise & type wise break up)

Sector	Thermal (MW)				Nuclear (MW)	Renewable (MW)		Total (MW)	%
	Coal	Gas	Diesel	Sub-Total Thermal		Hydro	Other Renewable		
Central	55,245.00	7,490.83	0.00	62,735.83	6,780.00	11,651.42	0.00	81,167.25	25
State	65,145.50	7,257.95	363.93	72,767.38	0.00	29,703.00	1,963.80	104,447.28	32
Private	74,012.38	10,580.60	473.70	85,066.68	0.00	3,240.00	55,283.33	143,590.01	43
All India	194,402.88	25,329.38	837.63	220,569.88	6,780.00	44,594.42	57,260.23	329,204.53	100

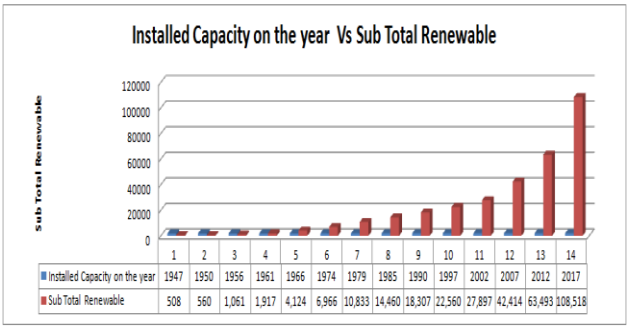


Figure 9. Installed Capacity on the year Vs Sub Total Renewable

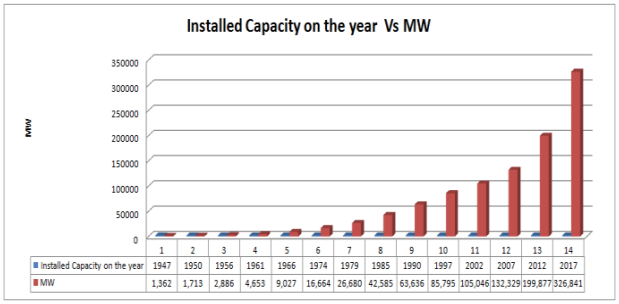


Figure 10. Installed Capacity on the year Vs MW

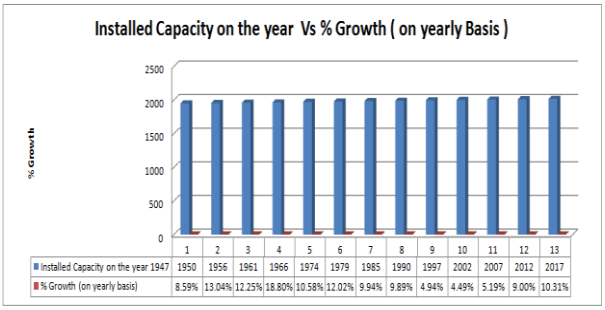


Figure 11. Installed Capacity on the year Vs % Growth (on yearly basis)

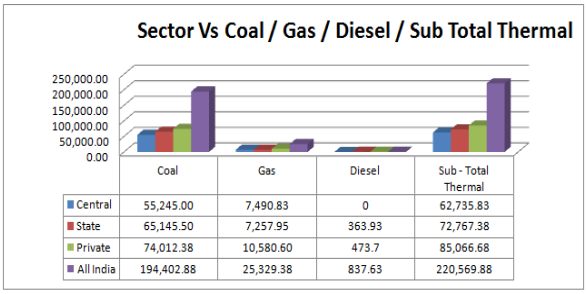


Figure 12. Sector Vs Coal / Gas / Diesel / Sub Total Thermal

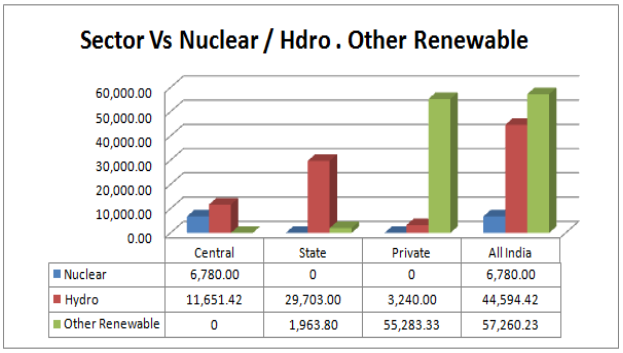


Figure 13. Sector Vs Nuclear / Hydro / Other Renewable

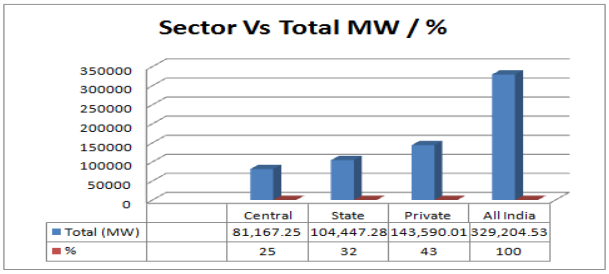


Figure 14. Sector Vs Total MW / Percentage (%)

II. CONCLUSION

A discussion of power system generation are tabulated and represented in the graphical form starting from the year of independence till 2017. By analyzing the graphical representation we can infer that there is a rapid and extraordinary growth in generation of power system in the country. But there is the shortage still present in consumption of power system produced in the country. The main motivation is to increase the generation of the power system so as to satisfy the need of the consumption. In future the needed power supply can be produced by using renewable energy system. Since the renewable energy systems reduced the pollution.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Study of Jtag-Tap Controller for Board Level Testing

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ABSTRACT

This paper gives the detailed study of Test Access Port (TAP) and its functions associated with boundary scan testing for various Unit under Test (UUT).It also explain the boundary scan instructions and the signals through the TAP controller. Supports the applications of testing the devices on various factor using JTAG standard.

I. INTRODUCTION

Boundary scan testing is one of the Design for Testability (DFT) which is special method for system level testing. Boundary scan method is formally called as JTAG, is the standard given by the association IEEE. Boundary scan method can test both the digital and the memory blocks and also supports components and the system level. In these paper, the study of JTAG is discussed for different UUT for board level testing.

Table 1. Required Instruction for JTAG

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE/PRELOAD	Mandatory
USERCODE	Optional

Testing of UUT

The standard IEEE 1149.1 is tested for various UUT under the constraint like cluster test, interconnection test, infrastructure test and memory test. Fig 1 explains the mechanism of testing different UUT through the signals from TAP controller.

The infrastructure tests checks the connections between Boundary Scan circuitry and test bus as well as the most important registers within the Boundary Scan circuitry

The interconnection test checks the connections between Boundary Scan pins. This test considers transparent buffers and disables other buses.

The cluster test checks a non-Boundary Scan cluster by means of the surrounding BScan pins.

The completely-automated cluster test permits you to test combinatorial non-Boundary Scan clusters without much effort.

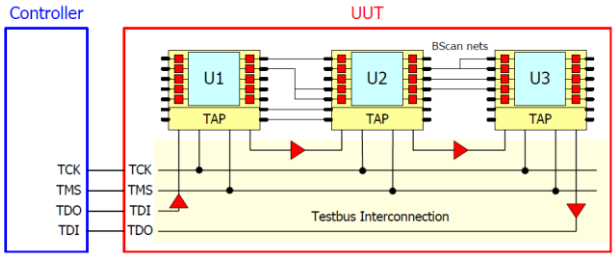

Figure 1. Block of testing different UUT

The TAP state diagram has two main branches and two idle states. Shift IR and Shift DR states are used to insert instructions and test data into the BS device. These are the most important states. TMS signal is used to move through the states While the TAP controller is the heart of any 1149.1 implementation, the instruct-ion register and instruction register decoder can be thought of as the brains. The instruction register stores information concerning which test register or test circuitry is active. Fig 2 shows the state diagram of controller for any boundary scan instructions.

For any instruction code selected, an associated register and/or test circuit is also selected. This is one of the requirements stated in the 1149.1 standard.

Instructions are shifted into the instruction register when the TAP controller is in the SHIFT-IR state and become active when the controller enters the UDPATE-IR state.

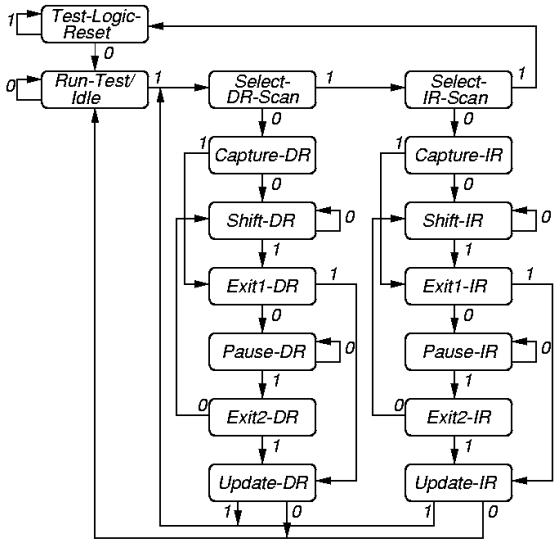

Figure 2. TAP Controller state Diagram

- Capture—DR: Each instruction must identify one or more test data registers that are enabled to operate in test mode when the instruction is selected. In this controller state, data are loaded from the parallel input of these selected test data registers into their shift-register paths on the rising edge of TCK.
- Shift-DR: Each instruction must identify a single test data register that is to be used to shift data between TDI and TDO in the Shift-DR controller state. Shifting allows the previously captured data to be examined and new test input data to be entered. Shifting occurs on the rising edge of TCK in this controller state. In the
- Shift-DR controller state, the TDO output is active (it is inactive in all other controller states except the Shift—IR state).
- Update-DR: This controller state marks the completion of the shifting process. Some test data registers may be provided with a latched parallel output to prevent signals applied to the system logic, or through the chip's system pins, from rippling while new data are shifted into the register. Where such test data registers are selected by the current instruction, the new data is transferred to their parallel outputs on the falling edge of TCK in this controller state.

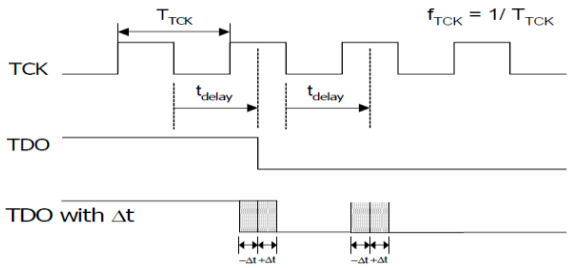

Figure 3. Timing diagram for TAP signals

The delay time (tdelay) to be entered is the time between the falling TCK edge at the controller's connector until the respective TDO signal edge from the UUT arrives at the controller's connector.

- ✓ tdelay includes the delay of **Distance POD** and/or testbus cable and UUT.
- ✓ Δt is the delay time tolerance. It is used to compensate inaccuracies of delay time and TCK frequency.
- ✓ If the exact value of tdelay is known, a value of 5 ns should be entered as Δt.

- ✓ The higher the desired test frequency is, the more accurately Δt has to be defined. The TCK frequency is set by the software according to the condition: **FTCK <= 1/ (4 x (Δt + 2 ns))**

Figure 3 shows that +Δt and –Δt form an undefined area where TDO is not exactly predicted.

However, it is important for the Boundary Scan technique that a rising edge of TCK may only occur after this undefined area to ensure a safe value for TDO. The distance between two undefined areas has to be at least as wide as an undefined area to achieve independence of the delay time.

Test Access Port (TAP) includes these signals:

Test Clock Input (*TCK*) -- Clock for test logic Can run at different rate from system clock

Test Mode Select (TMS) -- Switches system from functional to test mode

Test Data Input (TDI) -- Accepts serial test data and instructions -- used to shift in vectors or one of many test instructions

Test Data Output (TDO) -- Serially shifts out test results captured in boundary scan chain (or device ID or other internal registers)

Test Reset (TRST) -- Optional asynchronous TAP controller reset

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

A Review of Identification of Flood Location from Remotely Sensed SAR Images of Floods

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ABSTRACT

Probabilistic hail mapping offers weather managers, decision makers, protection agencies, and magnanimous relief organizations a complacent characterization of shot in the dark in flood mapping delineation. This study introduces a review of probabilistic hail mapping matter of form based on atrocious aperture radar (SAR) data.

I. INTRODUCTION

FLOOD events pose a major threat to human life and property. Worldwide, almost one billion people are estimated to be exposed to flooding with an annual probability above 0.01[1].Global financial losses due to flooding are expected to increase fromUS$6billion per annum in 2005toUS$52billion per annum by 2050, due to socioeconomic change alone[2]. As space assets are continuously improving there is a growing pressure on the scientific community to find new ways to use the increased volume and accuracy of remote sensing data for disaster risk reduction. The introduction of products and services based on Earth observation (EO) into the working practices of flood managers represents an opportunity to improve our society's capacity to respond to threats posed by large flood events. Insurance companies and flood managers require disaster impact databases, to better identify areas vulnerable to flood losses. Understanding the uncertainties in the flood maps can help identify locations where the provided classification might be highly uncertain. These locations are often critical from an infrastructure and human life perspective. Flood extent observations are also used by emergency response services to target their limited resources on the most risk-prone areas. However, risk assessment and optimal decision making in emergency situations would benefit for man appropriate communication of areas whose classification is uncertain. The most efficient way of mapping flood extents in near real time and over large areas is to exploit EO satellite images. These images represent a globally coherent and consistent source of flooding-related information, both spatially and temporally. In the growing collections of available EO data, data sets derived from synthetic aperture radar (SAR) are often considered as the most promising resource due to their almost all-weather day/night image acquisition capabilities [3]. Flat surfaces such as calm water appear as dark areas in a radar image, since most of the incident radar pulses are specularly reflected away from the antenna [4].As a result the mapping of water bodies in SAR images is often relatively straightforward, with notable exceptions being built environments, vegetated canopies, deep valley bottoms, and various surface water like response areas. As a consequence of the side-looking nature of SAR sensors, areas of a ground surface may not be visible to the satellite due to radar shadowing and layover caused by buildings or taller vegetation.

Non-flooded areas, such as tarmac, paved roads, and parking lots which appear smooth and water surface like at radar wavelengths, produce very low signal returns and are not easily distinguishable from flooded areas

Detection of flooded urban areas in high resolution Synthetic Aperture Radar images using double scattering BY D.C. Mason, L. Giustarini

A difficulty with using SAR for urban flood detection is that, due to its side-looking nature, substantial areas of urban ground surface may not be visible to the SAR due to radar layover and shadow caused by buildings and taller vegetation. This paper investigates whether urban flooding can be detected in layover regions (where flooding may not normally be apparent) using double scattering between the (possibly flooded) ground surface and the walls of adjacent buildings. The method estimates double scattering strengths using a SAR image in conjunction with a high resolution LiDAR (Light Detection and Ranging) height map of the urban area. A SAR simulator is applied to the LiDAR data to generate maps of layover and shadow, and estimate the positions of double scattering curves in the SAR image.

Water Level Estimation and Reduction of Hydraulic Model Calibration Uncertainties Using Satellite SAR Images of Floods BY Renaud Hostache, Patrick Matgen

Exploitation of river inundation satellite images, particularly for operational applications, is mostly restricted to flood extent mapping. However, there lies significant potential for improvement in a 3-D characterization of floods (i.e., flood depth maps) and an integration of the remote-sensing-derived (RSD) characteristics in hydraulic models. This paper aims at developing synthetic aperture radar (SAR) image analysis methods that go beyond flood extent mapping to assess the potential of these images in the spatiotemporal characterization of flood events. To meet this aim, two research issues were addressed. The first issue relates to water level estimation. The proposed method, which is an adaptation to SAR images of the method developed by [1] and [2] for water level estimation using flood aerial photographs, is composed of three steps: 1) extraction of flood extent limits that are relevant for water level estimation; 2) water level estimation by merging relevant limits with a Digital Elevation Model; and 3) constraining of the water level estimates using hydraulic coherence concepts. Applied to an ENVISAT image of an Alzette River flood (2003, Grand Duchy of Luxembourg), this provides ±54-cm average vertical uncertainty water levels that were validatedusing a sample of ground surveyed high water marks. The second issue aims at better constraining hydraulic models using these RSD water levels. To meet this aim, a "traditional" calibration using recorded hydrographs is completed via comparison between simulated and RSD water levels. This integration of the RSD characteristics proves to better constrain the model (i.e., the number of parameter sets providing acceptable results with respect to observations has been reduced).

Monitoring Flood Evolution in Vegetated Areas Using COSMO-SkyMed Data: The Tuscany 2009 Case Study BY Luca Pulvirenti

Synthetic Aperture Radar (SAR) systems represent a powerful tool to monitor floods because of their all-weather capability, the very high spatial resolution of the new generation of instruments and the short revisit time of the present and future satellite constellations. To exploit these technological advances, an accurate interpretation of the multitemporal radar signature of the flooded areas is required. Mapping flooded vegetation is a task in which the interpretation of SAR data is not straightforward and should rely on the knowledge about the radar scattering phenomena in the volume between canopy, trunks and floodwater. This paper presents a methodology aiming at mapping flooded areas with a focus on flooded vegetation; the algorithm is based on an image segmentation technique and a fuzzy logic classifier. The tuning of

the parameters of the fuzzy algorithm, based on the outputs of a theoretical backscattering model, is described in detail. Ancillary data giving accurate information on land cover are also used to set the input parameters of the model. The methodology is tested on a case study regarding a flood occurred in Tuscany (Central Italy) on December 2009 monitored using COSMO-SkyMed data. The multitemporal radar signatures observed during the event are discussed;

Discrimination of Water Surfaces, Heavy Rainfall, and Wet Snow Using COSMO-SkyMed Observations of Severe Weather Events BY Luca Pulvirenti

An automatic method to distinguish water surfaces (either flooded or permanent water bodies) from artifacts caused by heavy precipitation and wet snow is designed to improve flood detection accuracy in X-band synthetic aperture radar (SAR) images. The algorithm implementing the proposed method, mainly based on image segmentation techniques and on the fuzzy logic, consists of two principal steps: 1) detection of regions (or segments) of low-radar backscatter that appear dark in a SAR image, and 2) classification of each detected segment. Ancillary data, such as a local incidence angle map, a land cover map, and an optical image (helpful to detect wet snow), are also used. Through the fuzzy logic, the algorithm integrates different rules for the detection of dark areas, as well as for their classification based on radiometric, geometrical and shape features extracted from the segmented SAR image and on the ancillary data.

Conditioning Water Stages From Satellite Imagery on Uncertain Data Points BY Guy Schumann

Observed spatially distributed water stages with uncertainty are of considerable importance for flood modeling and management purposes but are difficult to collect in the field during a flood event. Synthetic aperture radar (SAR) remote sensing offers an inviting alternative to provide this kind of data. A straightforward technique to derive water stages from a single SAR flood image is to extract heights from a digital elevation model at the flood boundaries. Schumann et al. have presented a regression modeling approach as an improvement to this simple technique. However, regression modeling associated with their model may restrict output to mapping purposes rather than extend it to integration with other data or models. This letter introduces an inviting alternative that conducts statistical analysis on river cross-sectional data points, thereby allowing uncertainty assessment of remote-sensing-derived water stages without any regression modeling constraint.

Worldwide, almost one billion people are estimated to be exposed to flooding with an annual probability above, due to socioeconomic change alone. Insurance companies and flood managers require disaster impact databases, to better identify areas vulnerable to flood losses. Understanding the uncertainties in the flood maps can help identify locations where the provided classification might be highly uncertain.

These locations are often critical from an infrastructure and human life perspective. Flood extent observations are also used by emergency response services to target their limited resources on the most risk-prone areas. However, risk assessment and optimal decision making in emergency situations would benefit from an appropriate communication of areas whose classification is uncertain.

SYNTHETIC aperture radar (SAR) sensors are particularly useful for data acquisition during flood events due to their all-weather as well as day and night capabilities, and given the rapid recession of floods in smaller catchments, SAR is currently the most promising possibility to monitor floods from space. Despite the fact that many authors have shown since the mid-1980s that remote-sensing images of water bodies can be merged with topographical data to derive water stage, volume, and depth (e.g., [1]–[6]), a SAR flood image is, most of the time, limited to a simple wet–dry thresholding [6]. Schumann et al. [1] presented a (steady-state) SAR-based model that uses

regression analysis to account for most of the "noise" in water heights extracted from a LiDAR digital elevation model (DEM) at the SAR-derived flood boundaries. They developed the Regression- and Elevation-based Flood Information eXtraction (REFIX) model on a reach of the River Alzette north of Luxembourg City (G.D. of Luxembourg) for which they proposed a linear regression model to estimate spatially distributed water stages for the 2003 flood event. The methodology allows for rapid mapping and prepares the observed data in a consistent way with the SAR extractions. It is worth noting that the regression coefficients are not set by any field data butare conditioned on the SAR waters tag extracted at the flood boundaries of river cross sections drawn perpendicular to the direction of flow. In the presence of a hydraulic structure influencing the water surface gradient and therefore extent, piecewise or nonlinear regression can be applied to the SAR data to adapt the regression to localized flow behavior. The water stages estimated with the REFIX regression model can be used in a Geographic Information System to create a Triangular Irregular Network (TIN) mesh of the water surface, from which the actual flood plain DEM is subtracted to generate a 3-D flood depth and area map [1].

Block Diagram of Proposed Approach

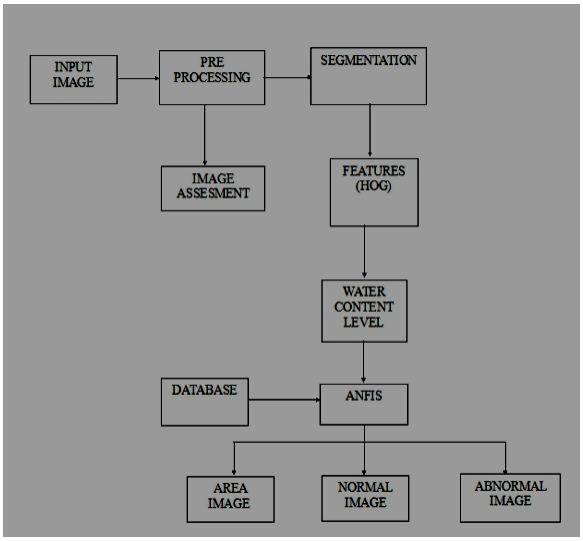

Figure 1

II. CONCLUSION

We have proposed a Bayesian approach for generating probabilistic flood maps from remotely sensed SAR images of floods. The probability of a particular pixel being flooded is derived from the histogram of back scatter values, the latter being modelled as a mixture of two populations of back scatter values, corresponding to flooded and non-flooded pixels, respectively. In addition to the SAR maps, the probabilistic flood mapping approach only requires the specification of the prior probability of a given pixel being flooded. With the help of K means segmentation we can identify the histogram of gradient. With ANFIS classifiers the output image are building, normal image and abnormal image can be determined. Based on the flood levels the voice board gives announcements.

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Performance Analysis in Vehicular Ad Hoc Network Architecture

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ABSTRACT

The Vehicular Ad hoc Network is a collection of portable hubs framing a brief system on variable topology, working without a base station and without an incorporated organization. VANETs generally established as reliable networks in that vehicles use for communication reason on expressways or urban conditions. Due to limitation streets and rapid of vehicles directing is an issue in VANET. VANET transforms each vehicle into a remote hub, permitting vehicles about 100 to 300 meters of each other to associate and, make a system with a wide range. Be that as it may, in circumstances where hubs are mobile or when hubs frequently turn on and off, the nearby topology stays settled. Subsequently, it is important that every hub communicates its refreshed hub data to the greater part of its neighbour updates from the nodes known as beacons. Signals are communicated occasionally to maintain a precise neighbour list. In this paper performance evaluation is done based on distance, speed, throughput based beaconing schemes using network simulator.

Keywords: VANET, performance evaluation, throughput, packets, locations

I. INTRODUCTION

VANET is the subclass of Mobile Ad Hoc Networks (MANETs). VANET recognizes MANET as far as the accompanying highlights: -, for example, the fast mobility of the system element or vehicles, to a great degree vast measure of system elements, exceptionally powerful topology of the system, substantial scale systems, irregular development example of vehicles, half and half correspondence design, self-sorting out nature of the system. It does now not rely upon any predictable group framework. Vehicular Ad Hoc frameworks are conceivable to pass on a broad scope of mobility related applications that range from development prepared spread and dynamic course proposing to aware of context advertisement and record sharing. VANET empowers communication between the vehicle to vehicle communication and the road side foundation.

The basic objective of VANET is to build security of road clients and help of travelers. Every hub inside VANET work as the switch and member of the system as the hubs conveys through various transitional hub that exists in their own transmission. The goal of Vehicular Ad Hoc Networks (VANETs) is to enhance vehicle traveler safety by methods for inter vehicle communication. For instance, if there should be an occurrence of a mishap, VANET communication can be utilized to caution different vehicles moving toward the site. VANET framework composed and is executed under the accompanying rigidity: availability and attribute of administrations, security and isolation. Recently car makers and media transmission organizations have been gearing to

furnish every vehicle with innovation that enables travelers and drivers to speak with each different and with the roadside framework that might be arranged in some basic areas of the street, for example, at each activity light or any crossing point to enhance the driving background and make driving more secure.

Today, a vehicle isn't only a thermo mechanical motor with couple of electronic gadgets. Or maybe, most recent headway in remote correspondence innovation has brought a chief change of vehicles from a straightforward moving motor to an intelligent framework transporter. The paper is arranged as follows: we have given related work in Section 2, and problem statement in Section 3 took after by the proposed work and results given in the section 4. Section 5 gives the conclusion of the paper.

II. PROPOSED WORK

A. PROBLEM STATEMENT

Upon introduction, every hub communicates a reference point advising its neighbours about its quality and its present area and speed and vitality. Following this, in most geographic routing conventions, for example, GPSR, every hub occasionally communicates its present area data. The position data got from neighbouring signals is put away at every hub. In light of the position refreshes got from its neighbours, every hub ceaselessly refreshes its nearby topology, which is spoken to as a neighbour list. Just those hubs from the neighbour list are considered as possible candidates for information sending. Along these lines, the reference points have a vital impact in keeping up a precise portrayal of the nearby topology. The signal interval affects network availability and expanded the system vitality utilization.

B. PREVIOUS WORK

In the previous paper DCIP-WAVE mechanism is proposed for IP addressing and one-hop communications using WAVE protocol. the quality of VANETs improved by providing internet access with distance-based reduction in power consumption in vehicle's RSU Units. The RSU provides Distance Cautious Internet Protocol (DCIP) to the OBU for internet access. The WAVE standard and its support of IP based applications is analysed and a Distance Cautious Internet Protocol in WAVE (DCIP-WAVE) is analysed.

III. RESULTS AND ANALYSIS

Simulation based performance comparison done using the parameters of distance, location, speed throughput using Network simulator. A scenario is setup to simulate 80 vehicles driving towards the same direction on two lanes with the inter-vehicle distance of 60m. in the distance-based execution examination, a hub transmits a reference point when it has moved a given separation d. The hub removes an outdated neighbour if the hub does not hear any reference points from the neighbour while the hub has moved more than k-times the distance d, or after a greatest time out of 5s. This approach along these lines is versatile to the hub portability, e.g., a quicker moving hub sends reference points all the more every now and again and the other way around. Figure 2 gives the distance measurement.

In the speed-based execution investigation, the beacon is reliant on the hub speed. A hub decides its signal interval from a predefined run with the correct esteem picked being conversely relative to its speed. Figure 3 gives the speed estimation when the distance varied.

In the throughput-based execution investigation the base and greatest delay are considered for the for the vitality utilization and to compute the life time of the Ad Hoc Networks. Figure 1 gives the throughput estimation investigation.

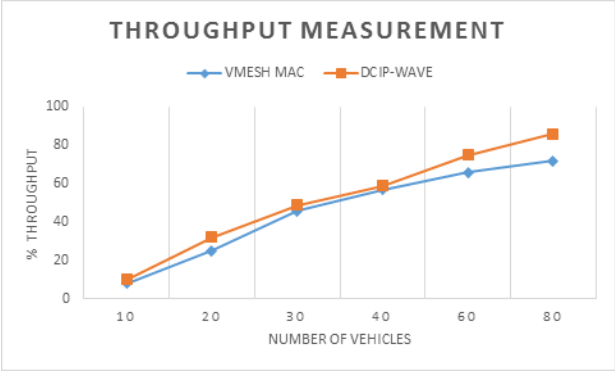

Figure 1. shows throughput measurement when increased number of vehicles = 80

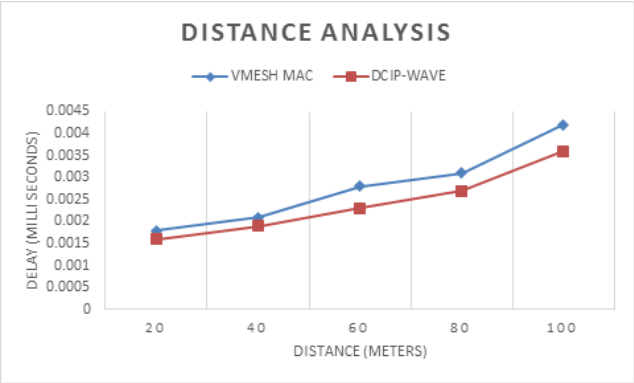

Figure 2. shows distance measurement when the distance varied between 20m to 100m

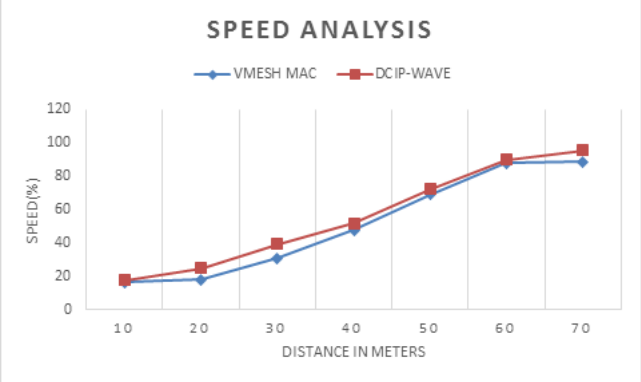

Figure 3. shows speed measurement when the distance is varied between 10m to 70 meters

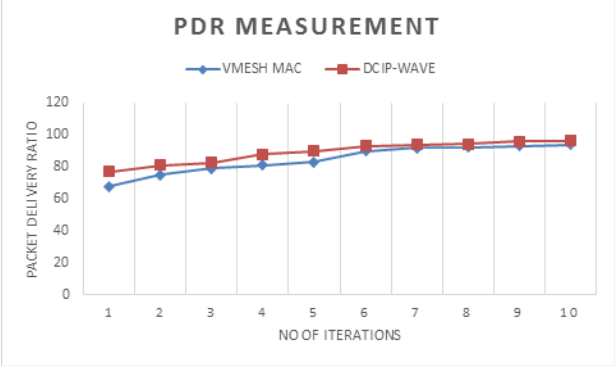

Figure 4. shows packet delivery ration for the number of iterations

The throughput and defer exhibitions of uplinks, i.e. from OBUs to RSUs when OBUs and RSUs are in communication scope of each other, are appeared in Figure 3 for both VMESH MAC protocol and DCIP WAVE protocol. It can be seen that under low traffic load, the throughput accomplished by the two protocols are very comparative, while the defer execution of DCIP WAVE is superior than the VMESH protocol. This is on the grounds that under light activity conditions, the probability of having impact in WAVE MAC is generally low. The outcomes show the advantage of crash free access protocol in ensuring the steady throughput and additionally the limited packet delay.

IV. CONCLUSION

In this work, we evaluated a portion of the fundamental regions that specialists have concentrated on over the most recent couple of years and these incorporate security, steering, QoS, and broadcasting strategies and we featured the most striking outcomes accomplished to date. We exhibited investigation intensive of NS2 recreation device appropriate for VANET condition. In this paper execution performance is done on distance based and speed based beaconing plans, considering the execution measurements in view of throughput, for example, normal delay, speed, throughput based aggregate packets dropped, least delay. The outcomes demonstrate that the proposed framework superior to anything the current framework regarding speed, distance and throughput. Theoretical investigation and simulation examinations demonstrate that the novel convention has focal points over the current WAVE MAC regarding framework all through.

In the following stage, we will research the execution streamlining of the DCIP WAVE convention utilizing topology data got through beaconing.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Mathematical Model for Modulation Detection in Adaptive Modulation System

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ABSTRACT

Modulation detection is the one the main process in Adaptive Modulation Systems. In this paper, propose the seven parameters to identify the best modulation. Modulation selection based on Amplitude, Phase, Frequency and Environment. The Seven Parameters are absEnv (Abstract environment), absPhase, rEnv (Environment), absEnv2 (Environment 2), absFreq, absFreq2, absPhase2. These modulation selections improve the Quality of Services and avoid the Multipath fading, Delay in Transmission/Receiving, Bandwidth limitation.

Keywords: Adaptive Modulation, QOS, Multipath Fading, Delay

I. INTRODUCTION

The mathematic distribution is related to the logistic distribution in an identical fashion to how the log-normal and normal distributions are related with each other. It is related to work towards Environment, Phase and frequency. A logarithmic transformation on the logistic distribution generates the log-logistic distribution. The probability density function (pdf) of the log-logistic distribution is f (x | α, β). where $\alpha > 0$ is the scale parameter, and is the median of this distribution; $\beta > 0$ is the shape parameter, which controls the shape of the distribution observe that this distribution has radically different shapes, as the distribution can be strictly decreasing, right-skewed, or unimodal. As β increases this distribution becomes more symmetric. Because of its flexible shapes, the log-logistic distribution has been illustrated to provide useful fits to data from many different fields, including engineering, economics, hydrology, and survival analysis. For instance, adopted this distribution in modeling economic data. Superior performance on fitting precipitation data from various Canadian regions. [3] applied this distribution to maximum annual stream flow data. For further topics related to the log-logistic distribution.

The estimating the unknown parameters of the log-logistic distribution. It is well-known the maximum likelihood method is a common choice to estimate the unknown parameters. This is due to its various attractive properties, such as being asymptotically consistent, unbiased, and normal as the sample tends to infinity. However, these attractive properties may not be valid when the sample size of the data is small or moderate, as is encountered in many practical applications. For instance, the maximum likelihood estimators (MLEs) may be severely biased to a certain order for a small sample size among others. It deserves mentioning that [1] recently considered Bayesian estimation of the log-logistic distribution using objective priors. They showed the performances of the Bayesian estimators and the

MLEs are quite similar with the various sample sizes, indicating the bias of the Bayesian estimators for small and moderate sample sizes. This motivates a study for obtaining unbiased or nearly unbiased estimators of the unknown parameters for the log-logistic distribution. First consider a certain 'corrective' approach developed in part by [7], which can correct the bias to the second order of magnitude. The main idea of this 'corrective' approach is to adjust the bias by subtracting it from the original MLEs, and so the obtained estimators are often referred to as bias-corrected MLEs. It is bias-corrected MLEs of the log-logistic distribution not only have explicit expressions in terms of a convenient matrix notation, but also simultaneously reduce the biases and the root mean square errors (RMSEs) of the parameters. Then consider Efron's bootstrap resampling method [8] which can also reduce the bias to the second order. However, this estimator may accomplish this with an expense of increased variance. As a comparison, we also consider the generalized moments (GM) method, a method commonly used in Hydrology. Monte Carlo simulation studies and real-data applications are provided to compare the performances of the various estimators under consideration. Numerical evidence shows that the proposed bias-corrected MLEs should be recommended for use in practical applications, especially when the sample size is small or moderate.

II. ESTIMATION METHODS

Automatic modulation detection extracts seven parameters (Features based on amplitude, frequency and phase) for identification of different modulation techniques, namely: ASK, FSK, PSK, QAM16 and QAM64. The thresholds of different parameters have been calculated from the classification during training in real time situation. The parameters are carefully chosen based on signal statistics. The parameters selected area The methods are based on the environment, Phase and frequency equations. This equation gives the best modulation identification in real time environments. Maximum Likelihood Estimation Suppose that we have n observations from the log-logistic distribution, denoted by X1 , · · · , Xn . The log-likelihood function of α and β can be written as

$$\log L = n\log(\beta) - n\beta\log(\alpha) + (\beta-1)\sum_{i=1}^{n}\log(X_i) - 2\sum_{i=1}^{n}\log\left[1+\left(\frac{X_i}{\alpha}\right)^{\beta}\right].$$

Differentiating the above function with respect to α and β, we have

$$\frac{\partial \log L}{\partial \alpha} = -\frac{n\beta}{\alpha} + \frac{2\beta}{\alpha}\sum_{i=1}^{n}\left(\frac{X_i}{\alpha}\right)^{\beta}\left[1+\left(\frac{X_i}{\alpha}\right)^{\beta}\right]^{-1},$$

Table 1

Parameter Name	Mathematical Model
AbsEnv	$absEnv = \frac{1}{N}\sum_{i=1}^{N}\lvert A_{cn}[i]\rvert$
AbsPhase	$absPhase = \frac{1}{C}\sum_{A_n[i]>a_t}\lvert\phi_c[i]\rvert$ $\phi_c[i] = \phi[i] - \frac{1}{N}\sum_{j=1}^{N}\phi[j]$
rEnv	$rEnv = \frac{1}{N}\sum_{i=1}^{N}\lvert A[i] - m_a\rvert \Big/ m_a$

absEnv2	$rEnv2 = \frac{1}{N}\sum_{i=1}^{N}\left\|B_{cn}[i]-m_b\right\|$ $B_{cn}[i] = \left\|A_{cn}[i]\right\|$ $m_b = \frac{1}{N}\sum_{i=1}^{N}B_{cn}[i]$
absFreq	$absFreq = \frac{1}{C}\sum_{A_n[i]>a_t}\left\|\frac{f[i]-f_a}{Fsym}\right\|$ $f_a = \frac{1}{C}\sum_{A_n[i]>a_t} f[i]$
absFreq2	$absFreq2 = \frac{1}{C}\sum_{A_n[i]>a_t}\left\|f_2[i]-\frac{1}{C}\sum_{A_n[j]>a_t} f_2[j]\right\|$ $f_2[i] = \left\|\frac{f[i]-f_a}{Fsym}\right\|$
absPhase2	$absPhase2 = \frac{1}{C}\sum_{A_n[i]>a_t}\left\|\phi_2[i]-\frac{1}{C}\sum_{A_n[j]>a_t}\phi_2[j]\right\|$ $\phi_2[i] = \left\|\phi_c[i]\right\|$

The MLEs can be obtained by setting the above two equations to zero. Due to the lack of explicit solutions to the above Equations, numerically estimate the MLEs using the logic MLE function from the R STAR package, created. It is well- known that the MLEs are biased with small sample sizes and the bias of an estimator may lead to misleading interpretations of phenomena in practical applications. This motivates a study for obtaining unbiased or nearly unbiased estimators to reduce the bias of the MLEs of the log-logistic distribution.

$$\frac{\partial \log L}{\partial \beta} = \frac{n}{\beta} - n\log(\alpha) + \sum_{i=1}^{n}\log(X_i) - 2\sum_{i=1}^{n}\left(\frac{X_i}{\alpha}\right)^{\beta}\log\left(\frac{X_i}{\alpha}\right)\left[1+\left(\frac{X_i}{\alpha}\right)^{\beta}\right]^{-1}$$

The corrective approach Suppose that based on 'n' randomly selected observations, we are interested in estimating the 'p' unknown parameters, expressed as θ = (θ1, · · · , θp) The joint cumulates of the derivatives of the log-likelihood function L(θ) are given by

$$k_{ij} = \mathbb{E}\left[\frac{\partial^2 L}{\partial\theta_i\partial\theta_j}\right], \quad k_{ijl} = \mathbb{E}\left[\frac{\partial^3 L}{\partial\theta_i\partial\theta_j\partial\theta_l}\right], \quad k_{ij,l} = \mathbb{E}\left[\left(\frac{\partial^2 L}{\partial\theta_i\partial\theta_j}\right)\left(\frac{\partial l}{\partial\theta_l}\right)\right],$$

where i, j, l = 1, 2, · · · , p. The derivatives of the joint cumulates

Here, assume that L(θ) is regular with respect to all derivatives up to the third order, inclusively. Also assume that all expressions in are of order O(n). Then bias can be writer as,

$$\mathrm{Bias}(\hat{\theta}_s) = \sum_{i=1}^{p}\sum_{j=1}^{p}\sum_{l=1}^{p} k^{si}k^{jl}\left[\frac{1}{2}k_{ijl} + k_{ij,l}\right] + O(n^{-2}), \quad s = 1, 2, \cdots, p,$$

Correcting Bias Using the Bootstrap will consider Efron's bootstrap resampling method, which was introduced by [8]. The main idea of this method is to generate pseudo-samples from the original sample to estimate the bias of the MLEs. Then subtract the estimated bias from the original MLEs to obtain bias-corrected MLEs. Let x = (x1, · · ·, xn)0 be a sample of n randomly selected observations from the random variable X with its cumulative distribution function

(cdf) given by F . Let the parameter υ be some function of F , denoted by υ = t(F). Let υˆ be some estimator of υ. We obtain pseudo-samples x∗ = (x∗, · · ·, x∗)0 from the original sample x by resampling observations with replacement. We compute the bootstrap replicates of υˆ from these pseudo samples, denoted by υˆ∗ = s(x∗). Use the empirical cdf (ecdf) of υˆ∗ to estimate the cdf of υˆ, Fυˆ . We obtain a parametric estimate for F by using a consistent estimator for Fυˆ , provided F belongs to a parametric family which is known and has a finite dimension, Fυ . The bias of the estimator υˆ = s(x) can be estimated by using BF (υˆ, υ) = EF [υˆ] – υ(F). Generalized Moments As a comparison, consider another commonly used method, the generalized moments (GM) method, which utilizes moments of the form E[X k] = Mk , where k can take on a diverse range of values, being positive or negative. In general, the values of k can be chosen to suit the user's needs, and the GM method can thus provide differing weights to the data values [4] have implemented the GM method for the log-logistic distribution based on similar techniques as are used for the generalized probability weighted moments (GPWM) method, introduced by [12]. For our problem, we consider probability weighted moments (PWMs) of the form

$$M_{k,h} = \mathbb{E}[X^k F^h] = \int_{-\infty}^{\infty} x^k F^h(x) f(x) dx$$
$$= \alpha^k B\left(h + 1 + \frac{k}{\beta}, 1 - \frac{k}{\beta}\right),$$

III. RESULTS AND DISCUSSION

The conduct Monte Carlo simulations to evaluate the performances of the various considered estimators of the log-logistic distribution. The data were simulated using the rllogis function in the STAR package created.

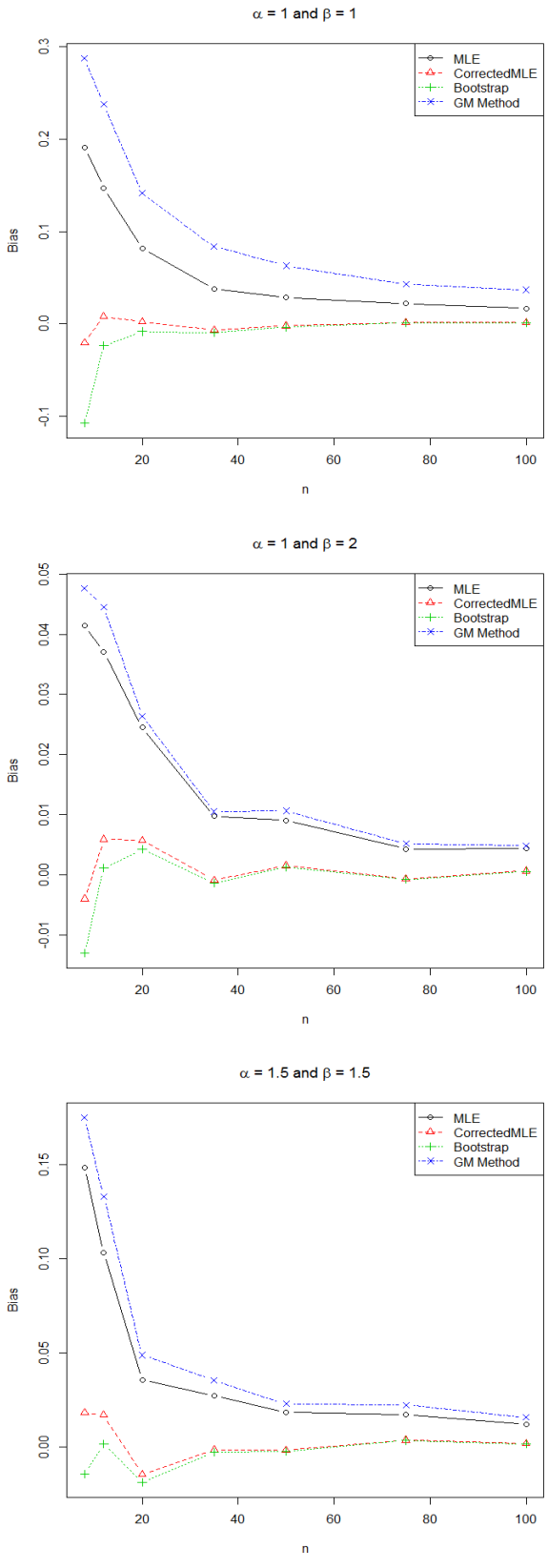

Figure 1. Comparison of the average biases of the four different estimation methods for

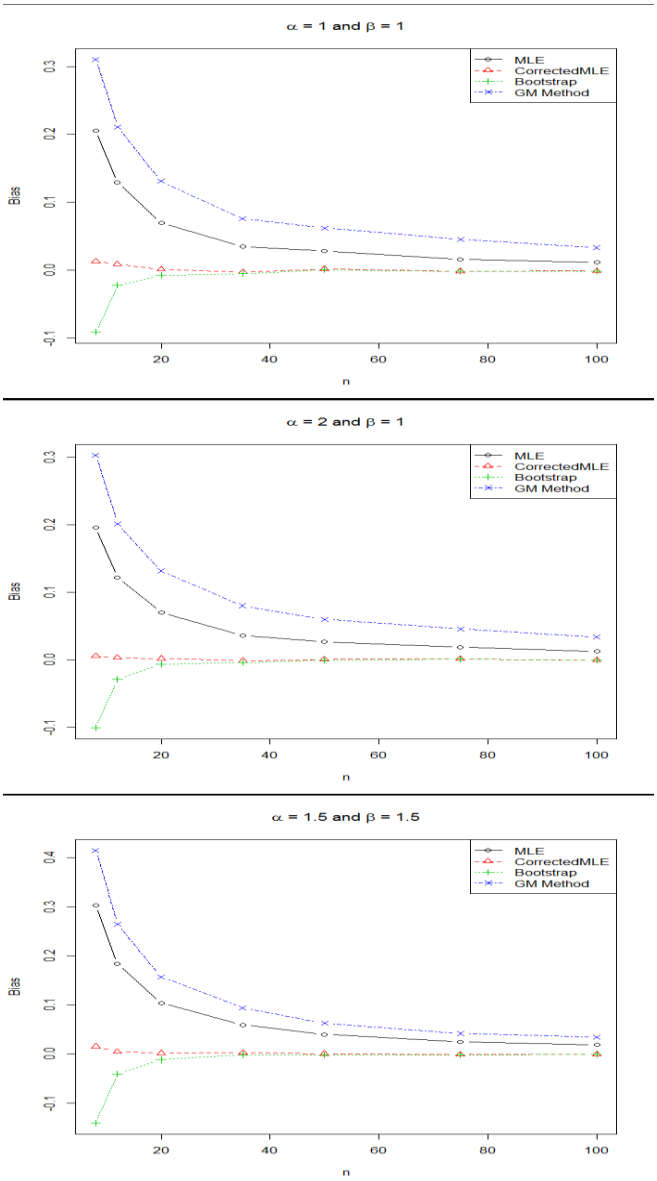

Figure 2. Comparison of the average biases of the four different estimation methods for β.

IV. CONCLUSION

The mathematical analysis can have performed with several parameters. Those parameters are analyzed with several conditions. Result show the best modulation identification based on the value of the α and β. Calculation are based the values represent in the graph MLE, Corrected MLE, Bootstrap and GM method. In future the work focused on the simply the calculations and increase the complexity also improve the security the modulation schemes.

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© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Scalable Transaction Management with Snapshot Isolation For NOSQL Data Storage System

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ABSTRACT

Cloud computing system refers to the demand delivery of IT resources via the internet with pay as you go pricing. A cloud offers many services to the end users such as software, infrastructure and platform go on. Develop scalable techniques for transaction management utilizing the snapshot isolation (SI) model. Because the SI model can lead to non-serializable transaction executions, investigate two conflict detection techniques for ensuring serializability. To support scalability, investigate system architectures and mechanisms in which the transaction management functions are decoupled from the storage system and integrated with the application-level processes. present two system architectures and demonstrate their scalability under the scale-out model of cloud computing platforms. In the first system architecture all transaction management functions are executed in a fully decentralized manner by the application processes. The second architecture is based on a hybrid approach in which the conflict detection functions are performed by a dedicated service. Perform a comparative evaluation of these architectures using the TPC-C benchmark and demonstrate their scalability.

Keywords: Scalable Transaction, key-value store, snapshot isolation

I. INTRODUCTION

The cloud computing platforms enable building scalable services through the scale-out model by utilizing the elastic pool of computing resources provided by such platforms. Typically, such services require scalable management of large volumes of data. It has been widely recognized that the traditional database systems based on the relational model and SQL do not scale well. The NoSQL databases based on the key-value model such as Bigtable and HBase. Have been shown to be scalable in large scale applications. Unlike traditional relational databases, these systems typically do not provide multi-row serializable transactions, or provide such transactions with certain limitations. For example, HBase and Bigtable provide only single-row transactions, whereas systems such as Google Megastore and G-store provide transactions only over a particular group of entities. These two classes of systems, relational and No SQL based systems. Represent two opposite points in the scalability versus functionality space. We present here scalable architecture models for supporting multi-row serializable transactions for key value based No SQL data storage systems. The widespread popularity of Cloud computing as a preferred platform for the deployment of web applications has resulted in an enormous number of applications moving to the cloud, and the huge success of cloud service providers. Due to the increasing number of web applications being hosted in the cloud, and the growing scale of data which these applications store, process, and serve – scalable data management systems form a critical part of cloud infrastructures.

This design is suitable for applications that require transactional access to groups of keys that are transient in nature, but live long enough to amortize the cost of group formation. Our assumption is that the number of keys in a group is small enough to be owned by a single node. Considering the size and capacity of present commodity hardware, groups with thousands to hundreds of thousands of keys can be efficiently supported. Furthermore, the system can scale-out from tens to hundreds of commodity nodes to support millions of Key Groups. G-Store inherits the data model as well as the set of operations from the underlying Key-Value store; the only addition being that the notions of atomicity and consistency are extended from a single key to a group of keys.

II. OVERVIEW OF EXISTING SYSTEMS

Present here scalable architecture models for supporting multi-row serializable transactions for keyvalue based NoSQL data storage systems. Our approach is based on decentralized and decoupled transaction management where transaction management functions are decoupled from the storage system and performed by the application-level processes themselves, in decentralized manner. In this approach the multi row transaction on SQL will be facing many issues like hanging or some kind of update error and so on. So that in this proposed system will be used for NoSQL method that will contain Some kind of issues like serializability to overcome this issues implement that Snapshot isolation method will helpful for to conform serializability. A new replica contacts all other existing replicas in the group and obtains information regarding the pending requests for which it was either a coordinator or a participant and the lock status for the items involved in these requests cycle detection approach requires tracking all dependencies among transactions. Anti-dependencies (both incoming and outgoing) among concurrent transactions, and write-read and write-write dependencies among non concurring transactions. We maintain this information in the form of a dependency serialization graph (DSG), in the global storage. Since an active transaction may form dependencies with a certain committed transaction, we need to retain information about such transactions in the DSG.

III. PROPOSED APPROACH

The approaches the focus was on evaluating the scalability of different approaches under the scale-out model. A comparison of the service-based model and the decentralized model in terms of transaction throughput and scalability and comparison of the basic SI and the transaction serializability approaches based on the cycle-prevention and the cycle-detection techniques .The approaches the focus was on evaluating the scalability of different approaches under the scale-out model. A comparison of the service-based model and the decentralized model in terms of transaction throughput and scalability and comparison of the basic SI and the transaction serializability approaches based on the cycle-prevention and the cycle-detection techniques .When two concurrent transactions Ti and Tj have anti-dependency, one of them is aborted. This ensures that there can never be a pivot transaction, thus guaranteeing serializability. We implemented and evaluated the above approaches in both the fully decentralized model and the service-based model. The cycle prevention approach can sometimes abort transactions that may not lead to serialization anomalies. Cycle Prevention Approach is a two concurrent transactions Ti and Tj have an anti-dependency, one of them is aborted. This ensures that there can never be a pivot transaction, thus guaranteeing serializability. In the context of RDBMS, this approach was investigated . A transaction is aborted only when a dependency cycle is detected involving that transaction during its commit protocol. The cycle detection approach aborts only the transactions that can cause serialization anomalies but it requires tracking of all dependencies for every

transaction and maintaining a dependency graph to check for cycles. Cycle Prevention Approach is a two concurrent transactions Ti and Tj have an anti-dependency, one of them is aborted.

IV. DESIGN

PNUTS presents a simplified relational data model to the user. Data is organized into tables of records with attributes. In addition to typical data types, "blob" is a valid data type allowing arbitrary structures inside a record, but not neces-sarily large binary objects like images or audio. (We observe that blob fields, which are manipulated entirely in application logic, are used extensively in practice.) Schemas are flexible: new attributes can be added at any time without halting query or update activity, and records are not required to have values for all attributes. The query language of PNUTS supports selection and prjection from a single table. Updates and deletes must specifiy the primary key. While restrictive compared to relational systems, single-table queries in fact provide very flexible access compared to distributed hash [12] or ordered [8] data stores, and present opportunities for future optimization by the system.Consider again our hypo-thetical social networking application: A user may update her own record, resulting in point access. Another user may scan a set of friends in order by name, resulting in range access. PNUTS allows applications to declare tables to be hashed or ordered, supporting both workloads efficently. Our system is designed primarily for online serving work-loads that consist mostly of queries that read and write single records or small groups of records. Thus, we expect most scans to be of just a few tens or hundreds of records, and optimize accordingly. Scans can specify predicates which are evaluated at the server. Similarly, we provide a "multiget" operation which supports retrieving multiple records (from one or more tables) in parallel by specifying a set of primary keys and an optional predicate, but again expect that the number of records retrieved will be a few thousand at most.

Our system, regrettably, also does not enforce constraints such as referential integrity, although this would be very desirable. The implementation challenges in a system with fine-grained asynchrony are significant, and require future work. Another missing feature is complex ad hoc queries (joins, group-by, etc.). While improving query functionality is a topic of future work, it must be accomplished in a way that does not the response-time and availability currently guaranteed to the more "transactional" requests of web applications.

V. CYCLE DETECTION APPROACH

A transaction is aborted only when a dependency cycle is detected involving that transaction during its commit protocol. The cycle detection approach aborts only the transactions that can cause serialization anomalies but it requires tracking of all dependencies for every transaction and maintaining a dependency graph to check for cycles. Cycle Detection Approach: A transaction is aborted only when a dependency cycle is detected involving that transaction during its commit protocol. This approach is conceptually similar to the technique [12] investigated in the context of RDBMS.The conflict dependency checks in the above two ap-proaches are performed in addition to the check for write-write conflicts required for the basic SI model. We implemented and evaluated the above approaches in both the fully decentralized model and the service-based model. The cycle prevention approach can sometimes abort transactions that may not lead to serialization anomalies. The cycle detection approach aborts only the transactions that can cause serialization anomalies but it requires tracking of all dependencies for every transaction and maintaining a dependency graph to check for cycles. When two concurrent transactions Ti and Tj have anti-dependency, one of them is aborted. This ensures that there can never be a pivot transaction, thus guaranteeing serializability. We implemented and evaluated the above approaches in both the fully decentralized model and the service-

based model. The cycle prevention approach can sometimes abort transactions that may not lead to serialization anomalies.

VI. CYCLE PREVENTION APPROACH

The first system architecture all transaction management functions are executed in a fully decentralized manner by the application processes. The second architecture is based on a hybrid approach in which the conflict detection functions are performed by a dedicated service. We perform a comparative evaluation of these architectures using the TPC-C benchmark and demonstrate their scalability. Cycle Prevention Approach is a two concurrent transactions Ti and Tj have an anti-dependency, one of them is aborted. This ensures that there can never be a pivot transaction, thus guaranteeing serializability. In the context of RDBMS, this approach was investigated .The cycle prevention approach requires tracking all dependencies among transactions, i.e., anti-dependencies (both incoming and outgoing) among concurrent transactions, and write-read and write-write dependencies among non concurring transactions. We maintain this information in the form of a dependency serialization graph (DSG), in the global storage. Since an active transaction may form dependencies with a certain committed transaction, we need to retain information about such transactions in the DSG. This raises an issue that a concurrent writer may miss detecting a read-write conflict if it attempts to acquire a write lock after the conflicting reader transaction has committed and its read lock has been released. To avoid this problem, transaction records its commit timestamp, in a column named 'read-ts' in the Storage Table, while releasing read lock acquired on an item. A writer checks whether the timestamp value written in the 'read-ts' column is greater than its snapshot timestamp, which indicates that the writer is concurrent with a committed reader transaction. A reader transaction checks for the presence of a write lock or a newer committed version for an item in its read set to detect read-write conflicts. Otherwise, it acquires a read lock on the item.

VII. TIME STAMP MANAGEMENT

The decentralized model the steps in the commit protocol are executed concurrently by the application processes. Because these steps cannot be performed as a single atomic action, a number of design issues arise as discussed below. There can be situations where several transactions have acquired commit timestamps but their commitment status is not yet known. We also need to make sure that even if a transaction has made its update to the storage system, these updates should not be made visible to other transactions until the transaction is committed. Therefore, we need to maintain two timestamp counters: GTS (global timestamp) which is the latest commit timestamp assigned to a transaction, and STS (stable timestamp), which is the largest timestamp such that all transactions with commit timestamp up to this value are either committed or aborted and all the updates of the committed transactions are written to the global storage. An example shown in Figure illustrates the notion of GTS and STS. In this example, STS is advanced only up to sequence number 16 because the commit status of all the transactions up to sequence number is known, however, the commit status of the transaction with sequence number is not yet known. When a new transaction is started, it uses the current STS value as its snapshot timestamp. We first experimented with using the key-value storage itself to store these counter values. However, we found this approach to be slow, and therefore we use a dedicated service which we refer to as Timestamp Service for maintaining these counter values.

VIII. EXPERIMENT

The SI model requires checking for write-write conflicts among concurrent transactions. This requires a mechanism to detect such conflicts and a method to resolve conflicts by allowing only one of

the conflicting transactions to commit. When two or more concurrent transactions conflict, there are two approaches to decide which transaction should be allowed to commit. The first approach is called first-committer-wins (FCW)[27], in which the transaction with the smallest commit timestamp is allowed to commit. In this approach, conflict checking can only be performed by a transaction after acquiring its commit timestamp. This enforces a sequential ordering on conflict checking based on the commit timestamps. This would force a younger transaction to wait for the progress of all the older transactions, thereby limiting concurrency. In contrast, in the second approach, which is called first-updater-wins , conflict detection is performed by acquiring locks on write-set items and in case of conflicting transactions the one that acquires the locks first is allowed to commit. The FUW approach appears more desirable because the conflict detection and resolution can be performed before acquiring the commit timestamp, there-by reducing any sequential ordering based on commit timestamps and reducing the time required for executing the commit protocol. Therefore, we chose to adopt the FUW approach for conflict detection.

There are two problems that arise due to transaction failures. A failed transaction can block progress of other conflicting transactions. A failure of a transaction after acquiring commit timestamp stalls advancement of the STS counter thereby forcing the new transactions to use old snapshot time, which may likely result in greater aborts due to write-write conflicts. Thus, an appropriate timeout mechanism is needed to detect stalled or failed transactions and initiate their recovery. The cooperative recovery actions for a failed transaction are triggered in two situations.

The conflicting transaction is waiting for the commit of a failed transaction, and the STS advancement has stalled due to a failed transaction that has acquired a commit timestamp. The recovery actions in the first situation are performed by any of the conflicting transactions, whereas the failures of the second kind are detected and recovery actions are performed by any application level process or by a dedicated system level process. If a transaction fails before acquiring a commit timestamp, then it is aborted, otherwise the transaction is committed and rolled-forward to complete its commit protocol.

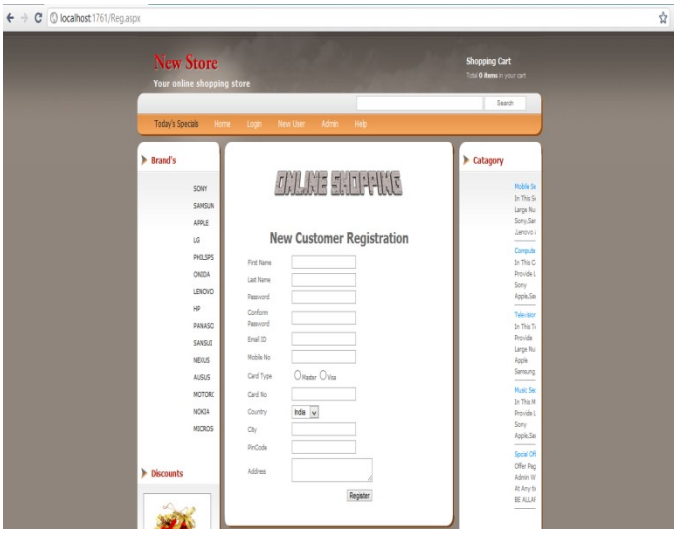

Figure 1. Registration screenshot

We used TPC-C benchmark to perform evaluations under a realistic workload. However, our implementation of the benchmark workload differs from TPC-C specifications in the following ways. Since our primary purpose is to measure the transaction throughput we did not emulate terminal I/O. Since HBase does not support composite primary keys, we created the row-keys as concatenation of the specified primary keys. This eliminated the need of join operations, typically required in SQL-based implementation of TPC-C. Predicate reads were implemented using scan and filtering operations provided by HBase. Since the transactions specified in TPC-C benchmark do not create serialization anomalies under SI, as observed in [9], we implemented the modifications suggested in. In our experiments we observed that on average a TPC-C transaction performed 8 read operations and 6 write operations.

We first identify the features of the key-value data storage system that are required for realizing the transaction management mechanisms presented here. The storage system should provide support for tables and multiple columns per data item (row), and primitives for managing multiple versions of data items with application-defined timestamps. It should provide strong consistency for updates [29], i.e., when a data item is updated, any subsequent reads should see the updated value. Moreover, for the decentralized architecture, we require mechanisms for performing row-level transactions involving any number of columns. Our implementation is based on HBase [3], which meets these requirements.

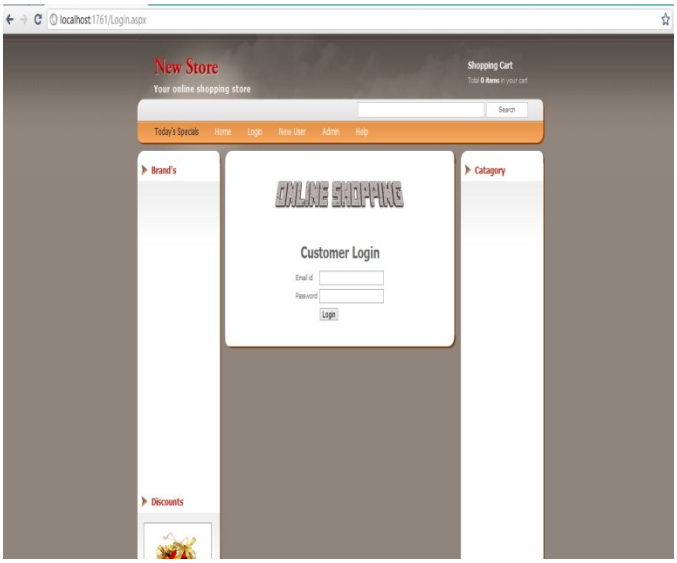

Figure 2. Login screenshot

For each transaction, we maintain in the global storage the following information: transaction, snapshot timestamp, commit time stamps , write-set information, and current status. This information is maintained in a table named Transaction Table in the global storage, as shown in Fig. 5. In this table, tid is the row-key of the table and other items are maintained as columns. The column out-edges' is used to record information related to outgoing dependency edges, which is required only in the cycle detection approach. To ensure that the Transaction Table does not become the bottleneck, we set the table configuration to partition it across all the HBase servers.

The data distribution scheme for HBase is based on sequential range partitioning. Therefore, if we generate transaction ids sequentially it creates a load balancing problem since all the rows in Transaction Table corresponding the currently running transactions will be stored only at one or few HBase servers. Therefore, to avoid this problem we generate transaction ids randomly. For each application data table, hereby referred as Storage Table, we maintain the information related to the committed versions of application data items and lock information, as shown in Fig. 6. An application may have multiple such storage tables. Since we adopt the eager update model, uncommitted versions of data items also need to be maintained in the global storage. A transaction writes a new version of a data item with its tid as the version timestamp. These version timestamps then need to be mapped to the transaction commit timestamp TSc when transaction commits. This mapping is stored by writing tid in a column named committed-version with version timestamp as TSc. The column 'w lock' in the Storage Table is used to detect write-write conflicts, whereas columns 'r lock,' 'read-ts,' and 'readers' are used in detecting read write conflicts for serializability, as discussed in the next section.

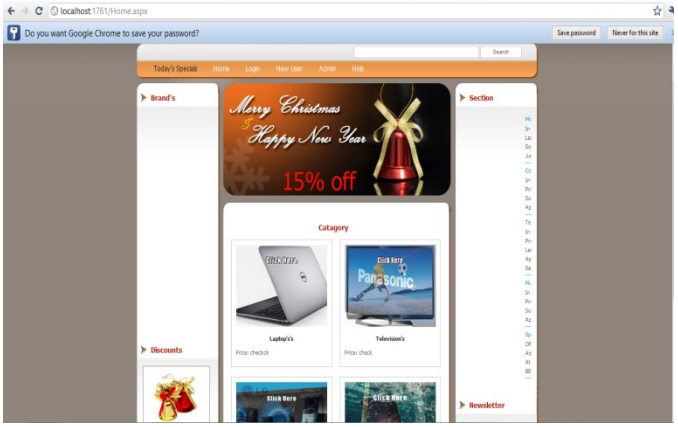

Figure 3. Home Screen Shot

Understanding Snapshot Isolation and Row Versioning. Once snapshot isolation is enabled, updated row versions for each transaction are maintained in tempdb. A unique transaction sequence number identifies each transaction, and these unique

numbers are recorded for each row version.SI is an extension of multiversion concurrency control. A transaction T1 executing with Snapshot Isolation Takes snapshot of committed data at start of T1 called start- timestamp Always reads/modifies data in its own snapshot Updates of concurrent transactions are not visible to T1 T1 is allowed to commit only when another Tx t2 running concurrently has not already written the data item that T1 intends to write.

PNUTS is a hosted, centrally-managed database service shared by multiple applications. To add capacity, we add servers. The system adapts by automatically shifting some load to the new servers. The bottleneck for some applications is the number of disk seeks that can be done concurrently; for others it is the amount of aggregate RAM for caching or CPU cycles for processing queries. In all cases, adding more servers adds more of the bottleneck resource. When servers have a hard failure (such as a burnt out power supply or RAID controller failure), we automatically recover by copying data (from a replica) to other live servers (new or existing), carrying out little or no recovery on the failed server itself. Our goal is to scale to more than ten worldwide replicas, each with 1,000 or more servers. At this scale, auto-mated failover and load balancing is the only way to manage the operations load. This hosted model introduces several complications that must be dealt with. First, different applications have different workloads and requirements, even within our relatively narrow niche of web serving applications. Therefore, the system must support several different workload profiles, and be automatically or easily tunable to different profiles. For example, our master ship migration protocol adapts to the observed write patterns of different applications. Second, we need performance isolation so that one heavyweight application does not negatively impact the performance of other applications. In our current implementation, performance isolation is provided by assigning different applications to different sets of storage units within a region.

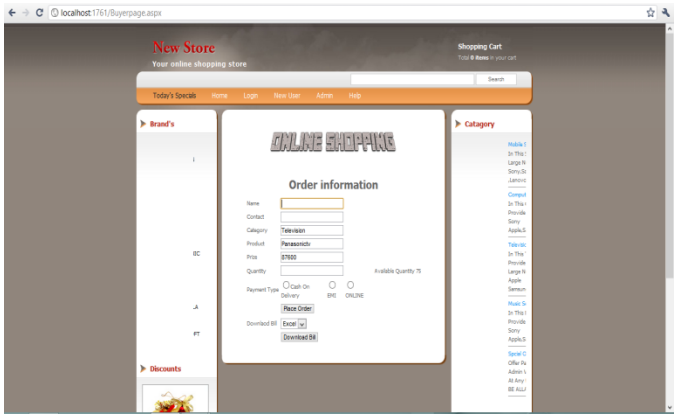

Figure 4. Buyer page Screen shot

Our implementation of Paxos has interesting trade in system behavior. Application servers in multiple datacenters may initiate writes to the same entity group and log position simultaneously. All but one of them will fail and need to retry their transactions. The increased latency imposed by synchronous replication increases the likelihood of conicts for a given per-entity-group commit rate Limiting that rate to a few writes per second per entity group yields insignificant conict rates. For apps whose entities are manipulated by a small number of users at a time this limitation is generally not a concern. Most of our target customers scale write throughput by shading entity groups more only or by ensuring replicas are placed in the same region, decreasing both latency and connect rate. Applications with some server \stickiness" are well positioned to batch user operations into fewer Megastore transactions. Bulk processing of Megastore queue messages is a common batching technique, reducing the conict rate and increasing aggregate throughput. For groups that must regularly exceed a few writes per second, applications can use the _ne-grained advisory locks dispensed by coordinator servers. Sequencing transactions back-to-back avoids the delays associated with retries and the reversion to two-phase Paxos when a convict is detected.

To scale throughput and localize outages, we partition our data into a collection of entity groups, each independently and synchronously replicated over a wide area. The underlying data is stored in a scalable

NoSQL datastore in each datacenter . Entities within an entity group are mutated with single-phase ACID transactions (for which the commit record is replicated via Paxos). Operations across entity groups could rely on expensive two-phase commits, but typically leverage Megastore's e_cient asynchronous messaging. A transaction in a sending entity group places one or more messages in a queue; transactions in receiving entity groups atomically consume those messages and apply ensuing mutations. Note that we use asynchronous messaging between logically distant entity groups, not physically distant replicas .All network transaction between datacenters is from replicated operations, which are synchronous and consistent. Indexes local to an entity group obey ACID semantics those across entity groups have looser consistency. See Figure 2 for the various operations on and between entity groups.

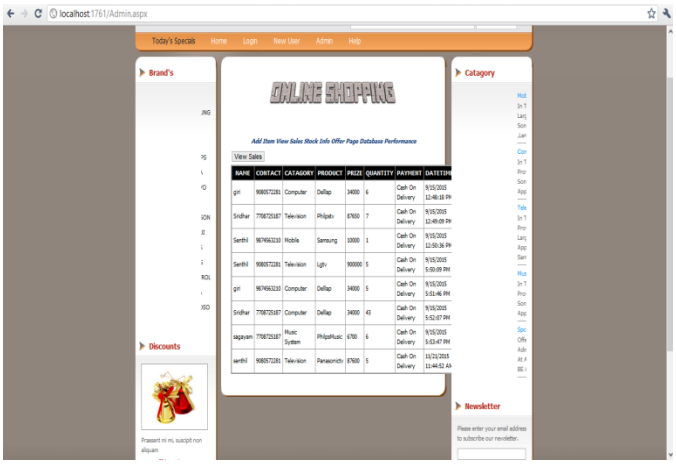

Figure 5. View sale Screen shot

We decided to use Paxos, a proven, optimal, fault-tolerant consensus algorithm with no requirement for a distinguished master. We replicate a write-ahead log over a group of symmetric peers. Any node can initiate reads and writes Each log append blocks on acknowledgments from a majority of replicas, and replicas in the minority catch up as they are able |the algorithm's inherent fault tolerance eliminates the need for distinguished failed" state. A novel extension to Paxos, detailed in Section, allows local reads at any up-to-date replica. Another extension permits single-roundtrip writes. Even with fault tolerance from Paxos, there are limitations to using a single log. With replicas spread over a wide area, communication latencies limit overall through-put. Moreover, progress is impeded when no replica is cur-rent or a majority fail to acknowledge writes. In a traditional SQL database hosting thousands or millions of users, using a synchronously replicated log would risk interruptions of widespread impact . So to improve availability and throughput we use multiple replicated logs, each governing its own partition of the data set.

We evaluated common strategies for wide-area replication Asynchronous Master/Slave A master node replicates write-ahead log entries to at least one slave. Log appends are acknowledged at the master in parallel with transmission to slaves. The master can support fast ACID transactions but risks downtime or data loss during failover to a slave. A consensus protocol is required to mediate master ship. Synchronous Master/Slave a master waits for changes to be mirrored to slaves before acknowledging them, allowing failover without data loss. Master and slave failures need timely detection by an external system. Optimistic Replication Any member of a homogeneous replica group can accept mutations , which are asynchronously propagated through the group. Availability and latency are excellent. However, the global mutation ordering is not known at commit time, so transactions are impossible. We avoided strategies which could lose data on failures, which are common in large-scale systems. We also discarded strategies that do not permit ACID transactions. Despite the operational advantages of eventually consistent systems, it is currently too dificult to give up the read-modify-write idiom in rapid application development. We also discarded options with a heavyweight master. Failover requires a series of high-latency stages often causing a user-visible outage, and there is still a huge amount of complexity. Why build a fault-tolerant system to

arbitrate mastership and failover work ows if we could avoid distinguished masters altogether.

Replicating data across hosts within a single data center improves availability by overcoming host-specific failures but with diminishing returns. We still must confront the networks that connect them to the outside world and the infrastructure that powers, cools, and houses them. Economically constructed sites risk some level of facility-wide outages [25] and are vulnerable to regional disasters. For cloud storage to meet availability demands, service providers must replicate data over a wide geographic area. In contrast to our need for a storage platform that is global, reliable, and arbitrarily large in scale, our hardware building blocks are geographically conned, failure-prone, and super limited capacity. We must bind these components into a united ensemble _bring greater throughput and reliability. To do so, we have taken a two-pronged approach for availability, we implemented a synchronous, fault tolerant log replicator optimized for long distance-links for scale, we partitioned data into a vast space of small databases, each with its own replicated log stored in a per-replica NoSQL datastore.

PNUTS presents a simplified relational data model to the user. Data is organized into tables of records with attributes.In addition to typical data types, “blob” is a valid data type, allowing arbitrary structures inside a record, but not neces-sarily large binary objects like images or audio. (We observe that blob fields, which are manipulated entirely in application logic, are used extensively in practice.) Schemas are flexible: new attributes can be added at any time without halting query or update activity, and records are not required to have values for all attributes. The query language of PNUTS supports selection and prjection from a single table. Updates and deletes must specific the primary key. While restrictive compared to relational systems, single-table queries in fact provide very flexible access compared to distributed hash or ordered data stores, and present opportunities for future optimization by the system . Consider again our hypo-thetical social networking application: A user may update her own record, resulting in point access. Another user may scan a set of friends in order by name, resulting in range access. PNUTS allows applications to declare tables to be hashed or ordered, supporting both workloads efficently. The implementation challenges in a system with fine-grained asynchrony are significant, and require future work. Another missing feature is complex ad hoc queries (joins, group-by, etc.). While improving query functionality is a topic of future work, it must be accomplished in a way that does not jeapardize the response-time and availability currently guaranteed to the more “transactional” requests of web applications. In the shorter term, we plan to provide an interface for both Hadoop, an open source implementation of Map Reduce , to pull data out of PNUTS for analysis, much as Map Reduce pulls data out of Big Table .

IX. CONCLUSION

We have presented here a fully decentralized transaction management model and a service-based architecture for supporting snapshot isolation as well as serializable transactions for key-value based cloud storage systems. We investigated here two approaches for ensuring serializability. We find that both the decentralized and service based models achieve throughput scalability under the scale-out model. The service-based model performs better than the decentralized model. To ensure the scalability of the service-based approach we developed a replication based architecture for the conflict detection service. The decentralized model has no centralized component that can become a bottle neck, therefore, its scalability only depends on the underlying storage system. We also observe that the cycle detection approach has significant overhead compared to the cycle prevention approach. We conclude that if serializability of transaction is required then using the cycle prevention approach is desirable. We also demonstrated here the effectiveness of the

cooperative recovery mechanisms used in our approach. In summary, our work demonstrates that serializable transactions can be supported in a scalable manner in NoSQL data storage system.

In this paper we present Megastore, a scalable, highly available datastore designed to meet the storage requirements of interactive Internet services. We use Paxos for synchronous wide area replication, providing lightweight and fast failover of individual operations. The latency penalty of synchronous replication across widely distributed replicas is more than onset by the convenience of a single system image and the operational benefits of carrier-grade availability. We use Bigtable as our scalable datastore while adding richer primitives such as ACID transactions, indexes, and queues. Partitioning the database into entity group sub-databases provides familiar transactional features for most operations while allowing scalability of storage and throughput.

X. FUTURE WORK

In the future, we would like to explore the implications of the Key Grouping protocol in the presence of analytical workloads and index structures built on Key-Value stores. We would also like to explore the feasibility of the design of G-Store using Key-Value stores such a Dynamo and PNUTS where the data store spans multiple data centers and geographical regions, and supports replication and weaker consistency guarantees of reads, and evaluate the ramifications of the weaker consistency guarantees of the data store on the consistency and isolation guarantees of transactions on groups In the concept multi row transaction using DB2 database has been more important one for all the process that scalability process to done the project work. In feature thing is all multi rows. If user at stabel mode means database will be remove the user from DataBase.

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National Conference on 'Innovative Research on Robotics, Circuits and Technology' (IRCT 2018)
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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Session Key for secured ATM Transaction

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ABSTRACT

Personalized identification number (PIN) entry method is highly unsecured due to various threats. To avoid these threats in bank transaction platform, we introduced two methods name STEGNO PIN and SESSION KEY which helps the user for safe bank transactions. In both the methods the main concept is to hide the pin numbers. In stegno pin we going to enter the pin number based on the shuffled position of the numbers in the virtual keypads, while in session key we going to achieve the secured traction by random generated symbols. User as the option to choose any one way of pin entry method through this applications .Once the pin number is entered then the application is redirects to the users banking service.

Keywords: Stegnopin, session key

I. INTRODUCTION

These personalized identification number (PIN) entry applications are increasing due to the development of touch screen which facilitates the implementation of pin entries interface on various commodities such as Automated teller machine (ATM), point of scale POS terminals, debit cards terminals, digital door lock, smart phones and tablet computers.

CONCEPT:

In this paper each ATM card will have separate four digit PIN number. The pin will be initially sent to the people as authentication on the time of their registry through this mobile application. We are going to hide the PIN by using Stegnopin or Session key method for secure transaction of money. Because nowadays transaction of money through mobile application is most popular and also less secure.

Requirements:

A) Hardware:

The software requirements are the specification of the system. It is a set of what the system should do rather than how it should do it. The software requirements provide a basis for creating the software requirements specification. It is useful in estimating cost, planning team activities, performing tasks, tracking the teams, and tracking the team's progress throughout the development activity.

- ✓ Windows 7 and above
- ✓ JDK 1.7
- ✓ Tomcat 6.0
- ✓ My sol. 5.0.

B) Software:

The hardware requirements may serve as the basis for a contract for the implementation of the system and should therefore be a complete and consistent specification of the whole system. They are used by software engineers as the starting point for the system design. It shows what the system does and not how it should be implemented.

- ✓ Hard Disk: 250GB and Above

- ✓ RAM : 4GB and Above
- ✓ Processor: I3 and Above
- ✓ OS: Gingerbread and above.
- ✓ No of Devices : 1.

VARIOUS ATTACKS IN PIN ENTRY:

- Guessing Attack.
- Shoulder Surfing Attack.
- Recording Attack.

A) Guessing Attack:

In guessing attack the attackers predict the user pin number and enter the number at an ATM machine so that they can get access to the banking account without the user's knowledge and the required transaction of money can be done. They can even block their account by entering the wrong pin more than thrice.

Figure 1

B) Shoulder Surfing Attack:

Shoulder surfing is a direct observation techniques to collect the data. This is an effective way to get information in the public places, because it's easy to stand next to someone and watch as they fill out any applications, using credit cards in shopping malls or ATM. Sometimes the vision-enhancing devices are also helps in this shoulder surfing attack, if subject is in far distance.

Figure 2

C) Recording Attack:

In recording attack the attackers use a skimming device or miniature cameras to record and hack the PIN (i.e.) Small cameras are fixed by the intruders inside the ATM to record the particular actions such as PIN entry, and the user gather all the required information even without their presence in that particular area. Such type of attacks is a great threat to society nowadays.

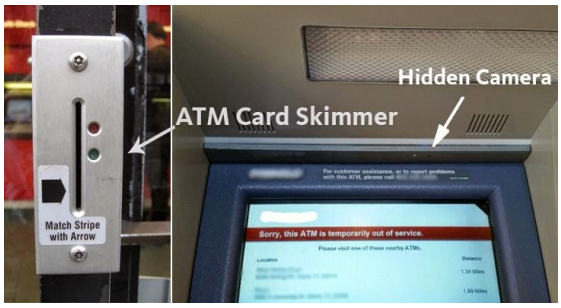

Figure 3

Why Android?

Android is the fast growing environment in which many kinds of applications are running successfully. This development of android is mainly for the easy access to the user with safe UI environments . Lets now learn some basic details about the android open source environment and also its applications.

Android:

Android is a Linux based open source operating system designed for use on cell phones, e-readers, tablet PCs and other mobile devices. For users of smart phones, Android provides easy access to social networking sites like Face book, Twitter and YouTube and smooth integration with Google products like Gmail, Google maps and Google calendar. Android has been adopted by a number of manufactures Motorola, Samsung etc.

II. ANDROID ARCHITECTURE

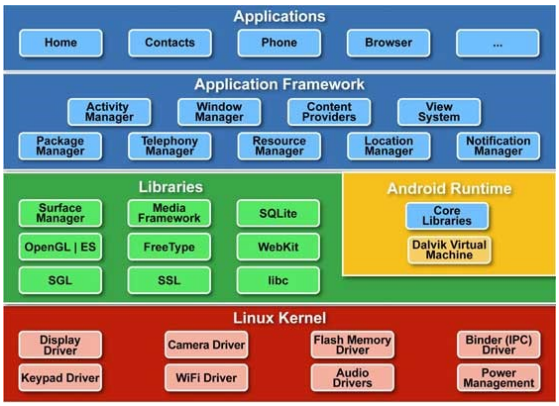

Figure 4

Applications of android:

- Android applications are composed of one or more application components (activities, services, content providers and broadcast receivers.
- Each components performs a different roles in the overall applications behavior and each one can be activated individually (even by othe applications).
- The manifest files must declare all components in the applications and should also declare all applications requirements such as minimum version of android required and any hardware configuration required.
- Non-code application resources (images ,strings, layout flies ,etc)should include alternatives for different devices configuration such as different strings for different languages

Flow chart:

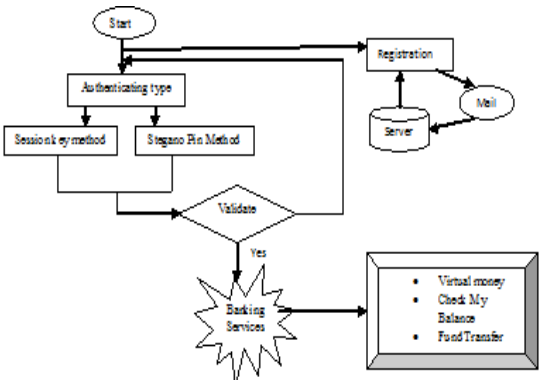

Figure 5

System Architecture:

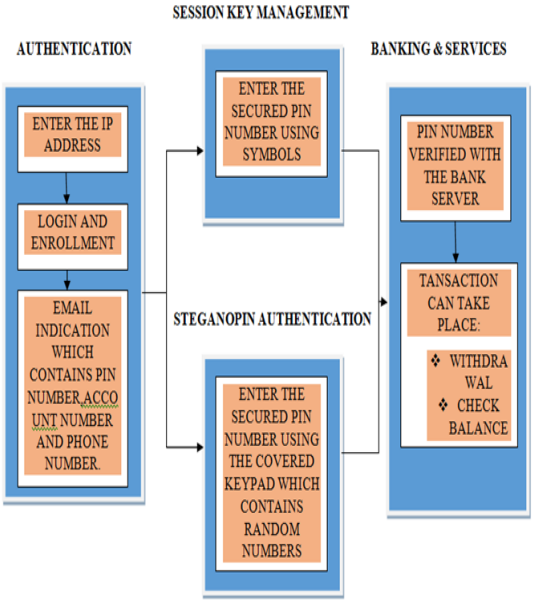

Figure 6

MODULES:

1. Authentication
2. Session Key management
3. SteganoPIN Authentication
4. Banking and Services

AUTHENTICATION:

User Registration is done and after that the user is able to access the ATM application in their mobile phones. Once their Registration is successfully completed, the user will be provided with the unique pin number which is sent to their registered mail Ids as the Mail Alert.

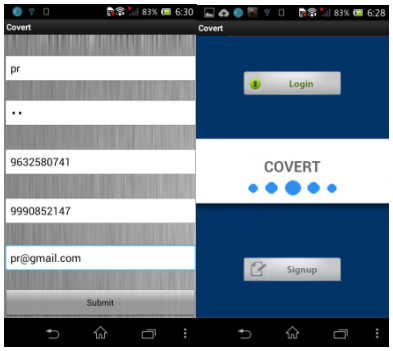

Figure 7

A) Mail Alert:

Mail Alert is just the form of authentication to the user which contain certain details like Account Holder Name, Pin Number, Account Number, and also the Amount present in their account which will helps in transaction

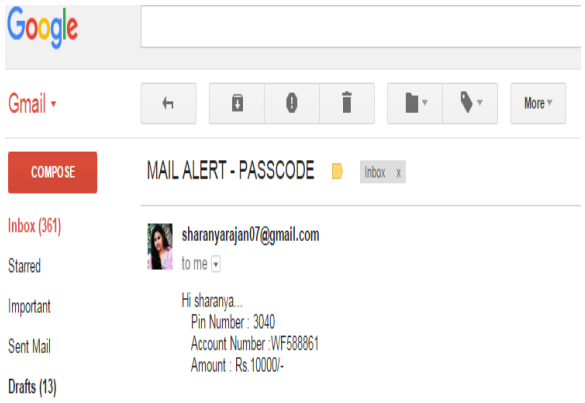

Figure 8

Once we get registered with the application we can use the same username and password for login. The pin number is used to access the services.

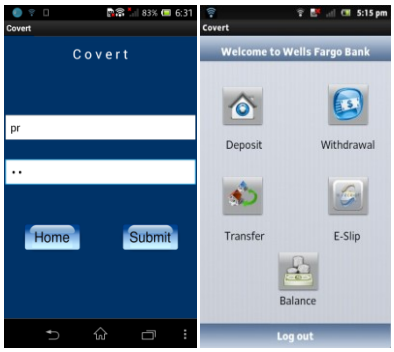

Figure 9

III. MODES OF ENTRY

In this process there is two method of pin transaction as we already mentioned before we can make any one of the mode of selesction as per the users wish. The two modes are as fallows:

- Stegnopin method
- Session key method

Figure 10

IV. SESSION KEY MANAGEMENT

In this session key method we are going to use the randomly generated symbols for the transactions. This method is designed in such a way that 0 to 9 digits arranged in vertical column and next to it another vertical column of ten symbols are arranged. The pin numbers is restricted to four digits which mean four rounds. The first round is session key decision round and the remaining three round are pin entry rounds. In each session key decision round the ten symbols are randomly generated, arranged and displayed so that attackers cannot guess the PIN number. For example, 2894 is the pin number the user selects the symbols next to each of the number 2,8,9,4 and Press "OK". In order to achieve this user is provided with the control buttons such as UP and DOWN, which helps the user to select the exact PIN without any flaws. .

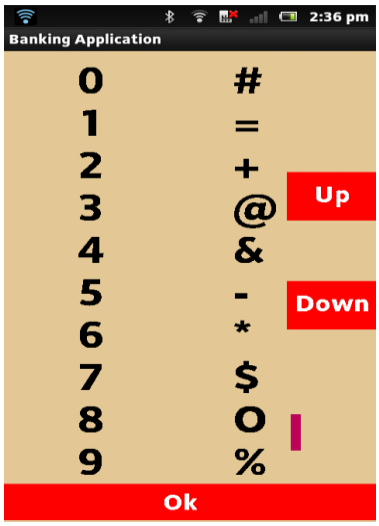

Figure 11

StegnoPIN Authentication:

The stegnopin system is uses two keypads one is the illusion and the other is response keypad. The response keypad appears in front of the user with regular layout and size. The illusion keypad appears in front of the user only when the screens senses the "P" shaped user cups. The illusion keypad help the user to select the position of the pin numbers, the keypad disappears once the "p" shaped user cups are removed. The illusion screen is also called as challenge keypads were the generated OTP by user registration are used. Finally the user enters the pin numbers on the regular keypads or response keypads based on the position of the virtual keys.

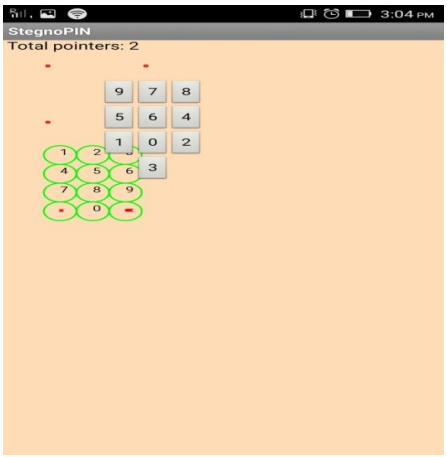

Figure 12

BANKING AND SERVICES:

Once the user has entered the OTP their respective pin number is identified. The pin number will be checked with the local database provided by the Sol. lite in order to continue the transaction, then one way hash method has been generated for the validation of pin entry which has been send to the server in the public channel so that the attacker cannot guess the pin by monitoring the channel .After verification the mobile app will provide a response to redirect the user to the services. In ATM services cash withdrawal and deposit and fund transfer can be done safely.

ADVANTAGES:

- ✓ Transaction of money is Safer.
- ✓ Security of PIN is also achieved.
- ✓ User Friendly Platform.

V. CONCLUSION

Our paper is proposed to minimize the attacks that prevail in ATM transactions. This mobile application will be more useful to this digital world which lacks in security. This is simple to install. Hence leads to the safer transactions of money between the bank and the customer.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Application of LabVIEW in Digital System Design and Image Processing

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ABSTRACT

The main objective of this article is to simulate the experiment of digital logic using LabVIEW. This article explains the application of LabVIEW in digital logic experimental teaching, and completed design of the assembly logic circuit output system and extinguished zero function of 12 digital display system and displayed the result by digital display. The actual experimental results verify the correctness of the simulation system, enrich the digital logic experiment teaching method and means, and enhance the students learning interest and enthusiasm.

Keywords: LabVIEW, Digital Logic Experiment, Seven Segment Display.

I. INTRODUCTION

LabVIEW [1] is a graphical programming language that uses icons instead of lines of text to create applications. In contrast to text-based programming languages, where instructions determine program execution, LabVIEW uses dataflow programming, where the flow of data determines execution order. LabVIEW also includes several wizards to help you quickly configure your DAQ devices and computer-based instruments and build applications. In LabVIEW, you build a user interface by using a set of tools and objects. The user interface is known as the front panel. You then add code using graphical representations of functions to control the front panel objects. The block diagram contains this code. In some ways, the block diagram resembles a flowchart. Users interact with the Front Panel when the program is running. Users can control the program, change inputs, and see data updated in real time. Every front panel control or indicator has a corresponding terminal on the block diagram. When a VI is run, values from controls flow through the block diagram, where they are used in the functions on the diagram, and the results are passed into other functions or indicators through wires.

In the front panel of LabVIEW, under control choose board, Boolean control provided all kinds of Boolean input control, including various button, switch and lamps circuit components, as shown in Fig.1. Boolean transport operator choose board of program diagram function choose provided fully functional logic operator, as shown in Fig.2. To design programs for Indicator light when logic really (“1”) and lights out to show logical false (“0”). LabVIEW also has the function of creating subVI; users can need according to oneself design subVI to realize special function

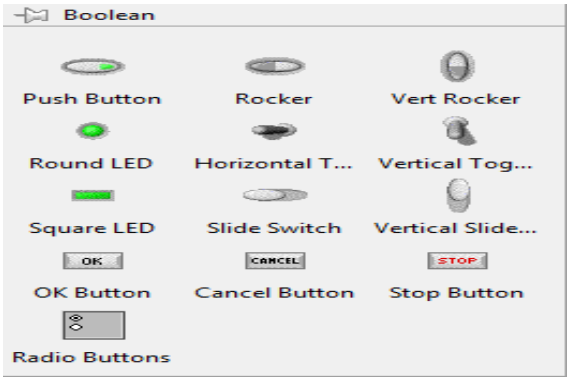


Figure 1. Boolean Control Palette

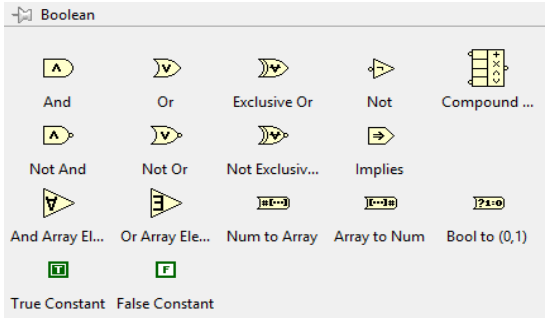


Figure 2. Boolean Functions Palette

II. TYPES OF DIGITAL DISPLAY:

The Common Cathode Display (CCD) – In the common cathode display, all the cathode connections of the LED's are joined together to logic "0" or ground. The individual segments are illuminated by application of a "HIGH", logic "1" signal to the individual Anode terminals.

The Common Anode Display (CAD) – In the common anode display, all the anode connections of the LED's are joined together to logic "1" and the individual segments are illuminated by connecting the individual Cathode terminals to a "LOW", logic "0" signal.

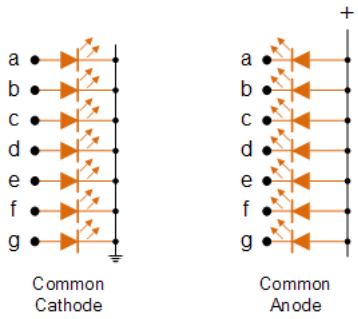


Figure 3. (a) Common cathode display

Figure 3. (b) Common anode display

TRUTH TABLE FOR DISPLAY:

The Segment which is to be glow has given "High" as input.

Table 1. Truth Table for Hexadecimal Display

Individual Segments							Display
a	B	c	D	e	F	g	
1	1	1	1	1	1	0	0
0	1	1	0	0	0	0	1
1	1	0	1	1	0	1	2
1	1	1	1	0	0	1	3
0	1	1	0	0	1	1	4
1	0	1	1	0	1	1	5
1	0	1	1	1	1	1	6
1	1	1	0	0	0	0	7
1	1	1	1	1	1	1	8
1	1	1	1	0	1	1	9
1	1	1	0	1	1	1	A
0	0	1	1	1	1	1	b
1	0	0	1	1	1	0	C
0	1	1	1	1	0	1	d
1	1	0	1	1	1	1	e
1	0	0	0	1	1	1	F

Table 2. Boolean Expression

SEGMENT	EXPRESSION
'a'	$\bar{A}BD + A\bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}C + A\bar{D} + BC$
'b'	$\bar{A}\ (\overline{C \oplus D}) + A(C \oplus D) + \bar{B}\bar{C} + \bar{B}\bar{D}$
'c'	$\bar{B}\bar{C} + \bar{B}D + \bar{C}D + \bar{A}B + A\bar{B}$
'd'	$\bar{B}\bar{C}\bar{D} + \bar{B}CD + \bar{A}C\bar{D} + B\bar{C}D + A\bar{C} + AB\bar{D}$
'e'	$\bar{B}\bar{D} + C\bar{D} + AB + AC$
'f'	$\bar{A}B\bar{C} + \bar{C}\bar{D} + B\bar{D} + AC + A\bar{B}$
'g'	$\bar{A}B\bar{D} + B\bar{C}D + \bar{B}C + AC + A\bar{B}$

III. IMAGE PROCESSING

Digital Image Processing (DIP) is a multidisciplinary science that borrows principles from diverse fields such as optics, surface physics, visual psychophysics, computer science and mathematics. The many

applications of image processing include: astronomy, ultrasonic imaging, remote sensing, video communications and microscopy, among in-numerable others. In this paper, we discuss teaching visualization tools developed for Digital Image Processing. An image may be defined as a two-dimensional function f(x ,y), where x and y are spatial coordinates and the amplitude of f at any pair of coordinates is called the intensity of the image at that point. The term gray level is used often to refer to the intensity of monochrome images. Color images are formed by a combination of individual images. For example, in the RGB color system a color image consists of three individual monochrome images, referred to as the red (R), green (G), and blue (B) primary (or component) images. For this reason, many of the techniques developed for monochrome images can be extended to color images by processing the three component images individually. An image may be continuous with respect to the x and y coordinates, and also in amplitude. Converting such an image to digital form requires that the coordinates as well as the amplitude be digitized. Digitizing the coordinate values is called sampling; digitizing the amplitude values is called quantization. [4][5] Thus when x, y and the amplitude values of f are all finite, discrete quantities, we call the image a digital image.

IV. RESULTS AND SIMULATION

The following are the steps required to design Seven Segment LED Hexadecimal display using NI LabVIEW:

STEP 1: Open LabVIEW and press Ctrl + N followed by Ctrl + T keys to open new Front Panel and Block Diagram Window.

STEP 2: In Front Panel and from the menu select View → Control → Modern → Boolean → Round LED, drag and drop it on the front panel and Label as A (Input A), similarly select 3 more inputs and name it as B, C and D respectively. Arrange them as shown in Figure 4.

STEP 3: Similarly, In Front Panel and from the menu select View → Control → Modern → Boolean → Square LED, drag and drop it on the front panel and arrange them in Seven Segment LED Display and name each as individual segment **"Segment a, Segment b, Segment c, Segment d, Segment e,**

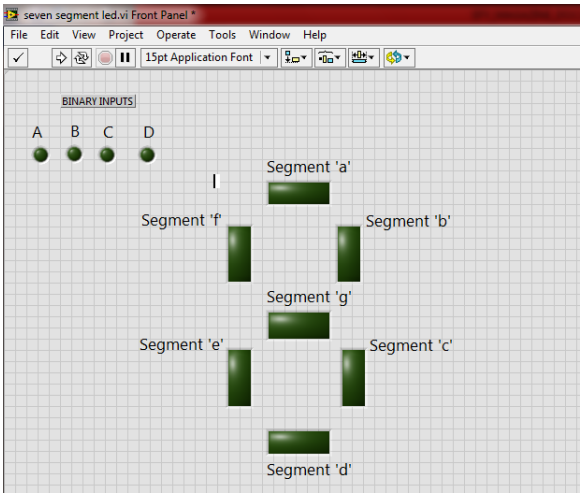
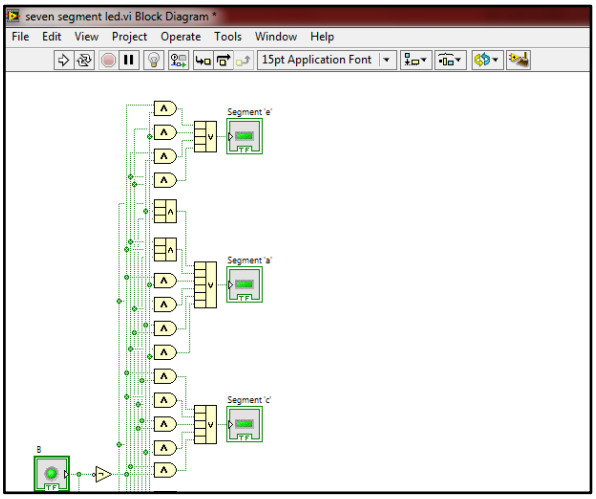


Figure 4. Front Panel



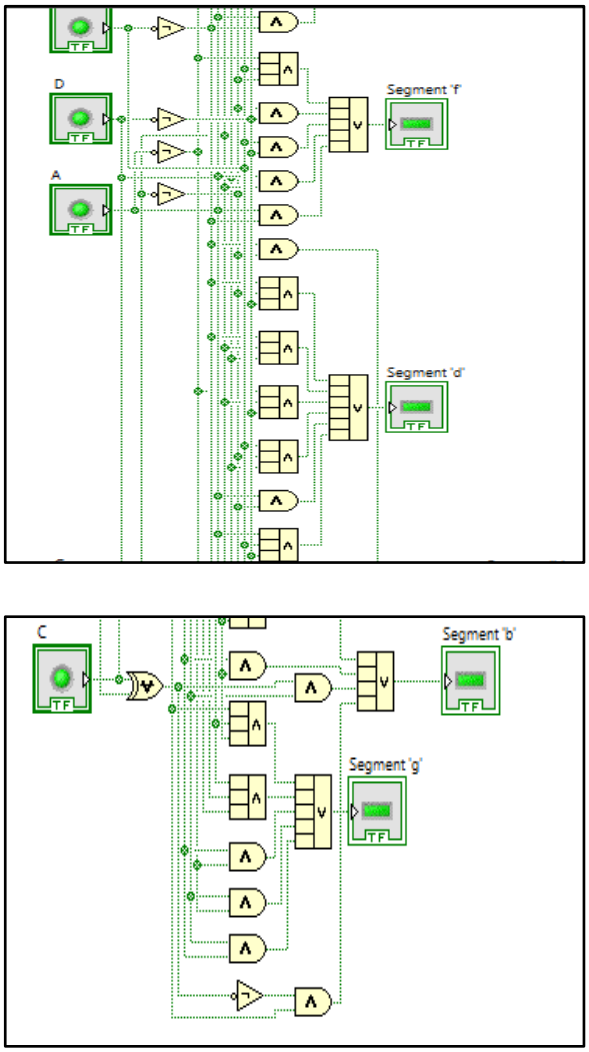


Figure 5. Block Diagram for Display

Segment f, Segment g. Arrange them as shown in Fig. 4.

STEP 4: Go to Block Diagram Workspace (Fig. 2) from the menu select Programming → Boolean → NOT gate, drag and drop it on the workspace for each and every input as shown in Fig. 5

STEP 5: From the menu select Programming → Numeric → Compound Arithmetic, drag and drop it on the workspace. Right Click the Compound Arithmetic, Select the option Change Mode → choose which logic gate operation needed (OR, AND). This compound Arithmetic is used to do Logical and Arithmetic Operations for more than two inputs.

STEP 6: Similarly select the suitable logic gates for the corresponding Boolean Expression for each segment as given in Table.2.

STEP 7: Connect each output of the Boolean expression to each of the indicator (Segments) as shown in Figure 3.

STEP 8: Return to Front Panel. Save the VI and press Run Continuously button to check the operation of seven segment display. Given different Binary Inputs and check the outputs from 0 to f.

Figure 6 shows the result of Seven Segment LED (Hexadecimal Display). The decimal values from 0 to 9 are obtained for the corresponding binary inputs as shown in Table 1. And also hexadecimal outputs such as 'A', 'b', 'C', 'd', 'e', 'F'. Certain characters appear in lowercase because 'B' looks similar to '8' in LED display and 'D' looks similar to '0' in LED display.

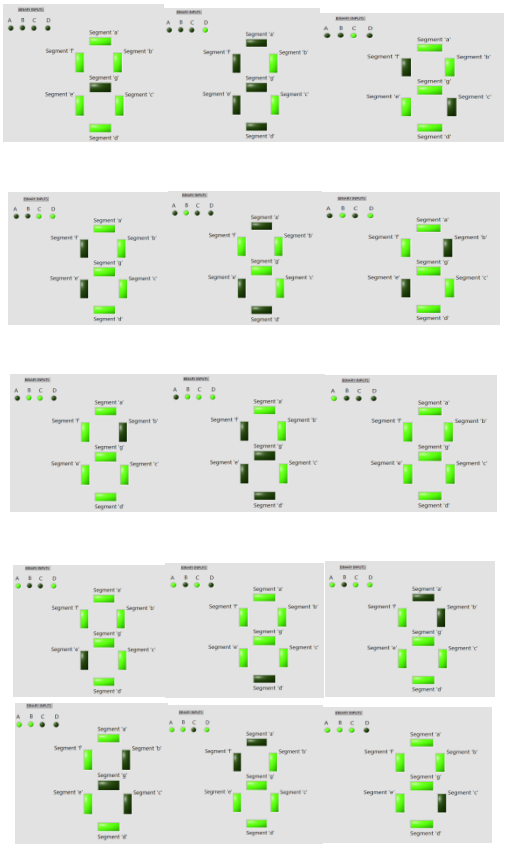


Figure 6. Decimal/Hexadecimal Display from (0 to 9, A, b, C, d, e)

a) IMAGE HISTOGRAM:

The histogram is a graph that contains the number of pixels in an image at different intensity value. In an 8-bit grayscale image a histogram will graphically

display 256 numbers showing the distribution of pixels versus the grayscale values.

b) IMAGE INVERSE:

This function creates a new image that is the inverse of the input image, like the negative of a photo, this function is useful with images generates by absorption of radiation, that is the case of medical image processing. For a gray scale image with values from 0 to 255, this function is defined as: q= 255-p.

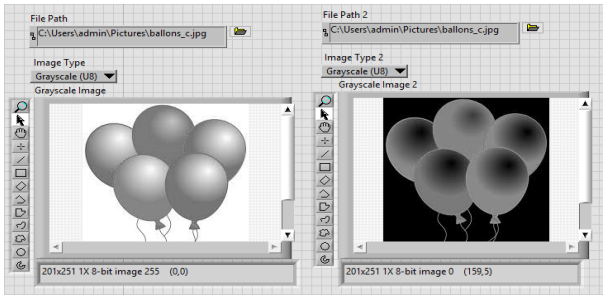


Figure 7. Gray Scale Image and Inverse Gray Scale Image

V. CONCLUSION

LabVIEW software used in digital logic experiment teaching in another field application fields except of in the test of virtual instrument system. The introduction of digital logic experiment teaching LabVIEW software can give full play to visualization and operability of virtual instrument system, which enable the teaching process to become more intuitive and make the experiment process can fully reflect and strengthen the design of practice of self-created experiment. Thus Image processing can be enhanced further by Pattern Matching etc in LABVIEW software. This process of Image Acquisition and Processing can be extended to the real time application of object detection and diagnosis of faulty objects in process industries.

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Microcontrollor Based Over Current Relay for Protection System

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ABSTRACT

Inverse overcurrent is normally associated with the overcur- rent relay types, the operation lime is inversely proportional (in certain degrees) with their overcurrent ratio.

I. INTRODUCTION

E The general equation of the inverse overcurrent relays can be written as In t = constant and is used for the protection Of transmission lines and equipments. The value of index n is chosen to match the specific characteristic required by the system under consideration. This paper describes a proposed scheme of overcurrent relays dealing with programming of a single-board dsp IC-30 F 3011 microcontroller, getting experimental results with better relay characteristic performances and high flexibility for implementing the desired value of ii including non-integer values.

dealing with the following points

1) the introduction of special control features which differ from the standard systems;

2) the implementation of unforeseen operational changes after installation of an equipment;

3) the recent trend to depart from standard substation configurations;

4) successive stages in the development of a substation which may require radical changes in automatic switching facilities.

In such cases relatively high engineering charges and development costs may be incurred [1].

These factors have encouraged the movement towards more flexible approaches; an obvious one is to use programmable sequence controllers which are based on plug board or diode matrix segments [13. While for many applications these provide economic equipment, for applications above a certain order of complexity the equipment may become bulky with many components.

An alternative approach is the use of microcontroller testing aids running either on the microcontroller system itself or on a more powerful large computer [1]. The reliability of such equipment is, of course, of great importance and here again the microcontroller scores well. Firstly, the principle of the system is such that wide use is made of large-scale integrated circuits which means that the number of compo- nents is minimized, resulting in good reliability and small size. Secondly, it is possible to perform a certain amount of self- checking in normal operation.

II. SYSTEM DESCRIPTION AND OPERATION PRINCIPLE

Fig. 1 represents a block diagram of a proposed microcontroller-based overcurrent relay.

The limited dc voltage output of the measuring unit is proportional to the operating current [7], i.e.,

The voltage is fed to a microcomputer [5], whose function is to perform the following jobs sequentially through an appropriate programming (flow chart is shown in Fig. 2):

1) analog-to-digital conversion;

2) fault detection;
3) function generation;
4) automatic variable time delay achievement;
5) pulse generation

The microcomputer first converts the dc analog input voltage into a digital equivalent in terms of the hexadecimal system [3], [4], [7], i.e. ,

$$(X)h = V \cdots$$

This digital value is tested. If there is a fault, this means that tested value exceeds a stored digital pick-up value, then it will be processed through a software function generator, which consequently determines the type of the resulting overcurrent relay, i.e.,

$$\frac{K_2}{g(X)}$$

The operation time of the relay is determined by a specified time delay subroutine [2] depending upon the value *or(Y)h,* i.e.,

$$t—Kg(Y)h\ldots\ldots$$

systems which offer a number of attractions over other approaches. The approach lends itself to software design and

Hence, pulses are generated through an output port of the microcontroller fed to the triggering isolating circuit which triggers the triac and so the tripping circuit is complete and the fault current will be cleared.

If there is no fault, i.e., the digital value of the ADC output is less than the pick-up value, the relay will not operate.

Simple mathematical operations on the above equations give a relation between the operation time I of the relay and the operating current I of the load to be protected as follows [7]:

$$t = \frac{K_2 K_3}{K_1 g(I)}.$$

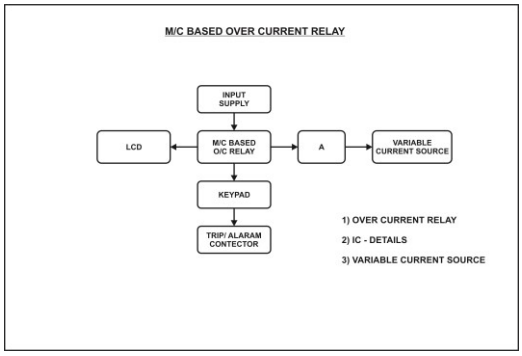

Figure 1

Figrue 2

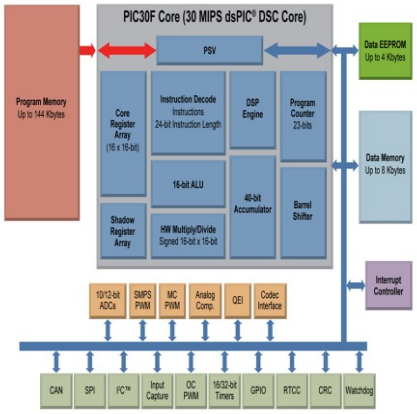

Figure 3

Description

1. Power ON/OFF Switch: Used to ON/OFF the input 230VAC of trainer kit
2. MCB: 20A Used to ON/OFF the Variable current source output
3. S1: START Button used to start the automatic relay tripping time measurement Circuit
4. S2: MANUAL STOP Button used to stop the automatic relay tripping time measurement Circuit
5. Autotransformer (Current adjustments) : Used to adjust the Variable ac current
6. Stop-Clock: Used to measure the relay tripping time

7. RESET Switch: Used to Restart the stop clock
8. Ammeter (Relay current): Used to measure the Applied relay current
9. Banana terminals (NC Contacts 1,2) – Over current relay Output NC Contacts
10. Banana terminals (C1,C2 , CT Input) – Over current relay Current input terminals
11. Banana terminals (C1A,C2A) – current source output terminals
12. Power input Connector (FM14-Back side) – Used for Mains input supply.

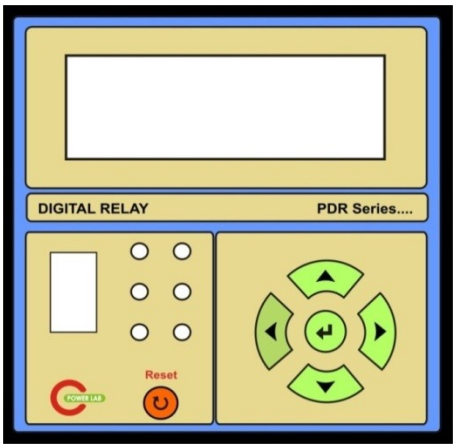

Figure 4

Make - PLI
Current Setting - 0-1A
Contacts 'No' & 'NC'

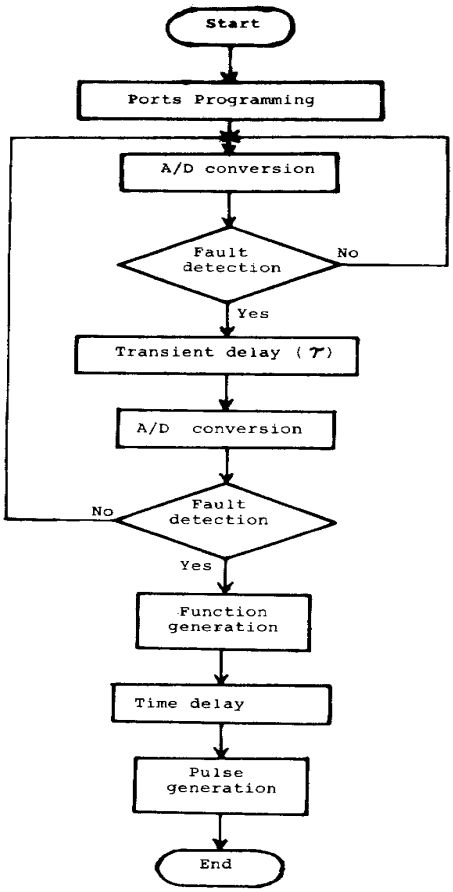

Fig. 2. Flow chart of the software in the microprocessor-based overcurrent relays.

or

$$tI^n = G \cdots \quad (6)$$

where $G = K_2K_3/K_1$ and $I^n = g(I)$.

Now it can be concluded that (6) is similar to the general equation [6] of the inverse time overcurrent relays.

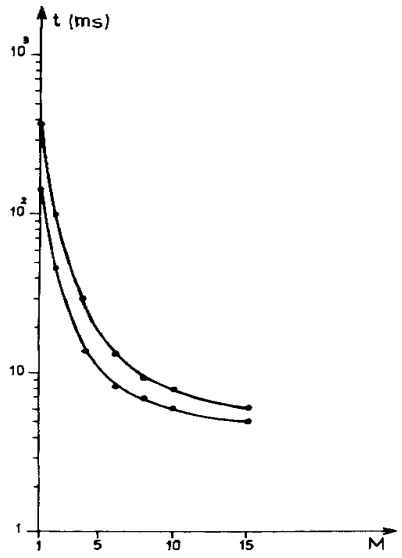

Fig. 3. Time-current characteristics for $n = 2$.

III. Experimental Results

In this proposed relay scheme, function generation is an important task achieved by the microcomputer since it will decide the type of resulting time-current characteristic [7]. Two types of function generation software have been used here.

1) The integer type used mathematical operations through multiplication and division subroutines to obtain characteristics with integer values of n. Fig. 3 shows time-current characteristic for $n = 2$.

2) The flexible type used a look-up table method in order to obtain the desirable value of n whether integer or non-integer as is shown in Fig. 4 for $n = 1.3$, which cannot be obtained in any other type.

Time multiplier settings can be obtained through a change in the time-delay subroutine.

It is useful to mention that the proposed technique cannot be used for instantaneous type overcurrent relay [7].

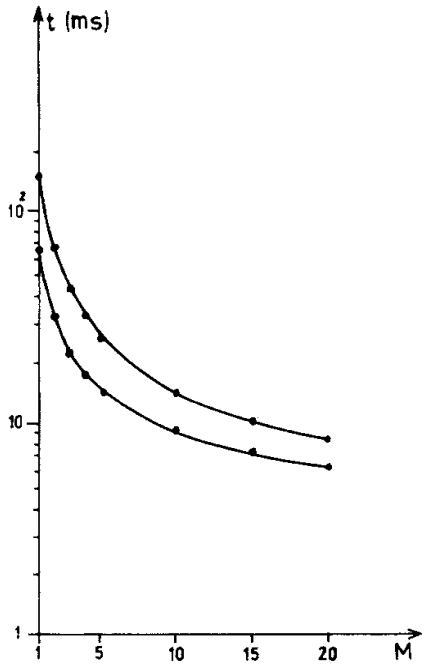

Fig. 4. Time-current characteristics for $n = 1.3$.

IV. Practical Applications

A brief discussion for applications of different types of time-current characteristics can be explained as follows [7]:

1) Definite time ($n = 0$): This is generally employed in cases of wide variation of system generating conditions. Another possible application is the differential protection of transformers. Also, it is used as backup relays for differential and distance protection schemes. Definite time is preferred to instantaneous over-current relay (discussed later) to serve as a check against short-time asymmetrical currents.

2) Inverse time ($n = 1$): This is generally employed in cases where the source impedance is much smaller than the line impedance. Because of the steep nature of the curve, it permits the use of the same-time multiplier setting for several relays in series. This reduces the time errors and overtravel so that the time margin for grading can be reduced.

3) Very inverse time ($n = 2$): Fuse coordination and thermal protection of transformers and induction motors require such characteristic. They are useful to protect against unbalanced operation of generators.

V. Conclusions

The proposed technique for generating inverse time over-current relay characteristics for any desired value of n is an accurate method of approaching theoretical characteristics. The basic design of the relay does not change with the different values of n desired. Only changing the subroutine of the function generation is required. This relay has a great advantage in ease of manfacturing and flexibility for any type of characteristics desired.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Modeling of Three Phase Ac-Ac Matrix Converter on Dfig Based Wind Energy Conversion System

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ABSTRACT

This paper presents a full description of three phase AC-AC matrix converter modeling through the wind energy conversion system (WECS) based on double fed induction generator (DFIG).MC is a proposed drive system used to perform the AC-AC conversion directly without any dc link. So, it may increases the output of the power generation. It controls the MPPT by adjusting the DFIG terminal frequency and the shaft speed. In addition, the MC controls the grid injected current to be in phase with the grid voltage for the unity power factor. Space vector modulation (SVM) is used to generate the pulse width modulation (PWM) signals of the matrix converter switches. Simulation studies of the proposed power generation system were carried out. Results obtained are presented and modeled with good control performance of the system.

Keywords: Wind Energy Conversion System (WECS); Double Feed Induction Generator (DFIG); Matrix Converter (MC); Space Vector Modulation(SVM); Pulse Width Modulation (PWM);Maximum Power Point Tracking .

I. INTRODUCTION

EARTH's fossil energy resources such as oil, gas and coal are limited in production and are expected to use beyond their peak in the next decades, so the price of energy can continue to rise. Ever rising need of energy in future can met by contributing more renewable energy sources. The growing need for electrical energy and they will to preserve the nature justifies the use of renewable energy sources. The use of renewable sources for

Electric power generation has been a huge increase since the past decade. Increased economical and ecological woes have driven researchers to discover newer and better means of generating electrical energy. In this race, the production of electricity by wind turbine is actually the best method in comparison with the energy produced by the solar source conversion and this is due to the price per a kilo watt that is less elevated with respect to the second [1].

Among the most used and available technologies for wind turbines, the doubly fed induction generator (DFIG) is the most accepted because it presents greater benefits for a reduced conversion structure and efficient energy capture due to the variable speed operation of wind turbine based on a conversion (DFIG). The doubly fed induction generator is the most popular option for harnessing energy from the wind because of variable and unpredictable nature of the wind speed. This base structure (DFIG) offers the benefits of improved efficiency, reduced converter, cost and losses are reduced, easy implementation of power factor correction, a variable speed operation,

and the control four quadrants of active and reactive power.

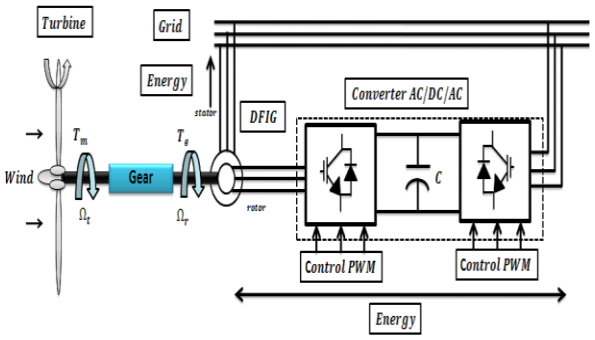

Figure 1. Wind Energy Conversion System's structure

Due to variable speed operation, the total energy production is 20% to 30% higher and therefore capacity utilization factor is improved and the cost per kWh of energy is reduced. In general, the stator windings of the DFIG are directly connected the electrical network and the rotor windings are powered via bidirectional PWM voltage converters (VSC). The control strategy is used to control the rotor and the stator output power supplied to the grid variable speed operation [2]. Decoupled control of active and reactive powers is the used approach based on vector control. Transfer of active power by a wind turbine based on (DFIG) in the distribution network can be carried out by the stator and rotor. The transfer direction of the active power is determined by wind speed and hence the synchronous speed of the generator. When a speed of the generator below the synchronous speed then the transfer of active power flows from the network to the electric rotor machine. The transfer is made by two cascaded converters. The first is linked to the network operates as a rectifier and the second operates as an inverter is connected to the rotor of the generator.

However, an AC-DC-AC converter system requires large DC-link capacitors, making the system bulky and expensive. In addition, its control scheme employs two current-regulated PWM controllers, one for the supply-side converter, the other the generator-side converter [3]. The control algorithms are thus complicated, having potentially a reliability problem. A direct AC-AC matrix converter can offer all the advantages given by its AC-DC-AC counterpart [4, 5]. More importantly it converts AC power in a single stage and eliminates large energy storage components. The work described in talus paper is based on a simulation study of a matrix converter controlled DFIG for wind power generation. For maximum energy capture from the wind, high performance speed control is desired to enable the speed of the generator to track closely the value predicted by the wind turbine power-speed characteristic curve. This is realized by regulating the rotor current using a stator flux, field-oriented scheme and a space-vector modulated matrix converter. The control scheme also enables flexible adjustment of the power factor. The principle of using the space vector modulation technique to control the matrix converter in a closed loop configuration is discussed.

In this paper, the use of a direct matrix converter [5, 6, and 7] for the control of the rotor-side currents of a DFIG system is proposed. Such a configuration offers certain advantages, notably:

1) The power converter requires no bulky an costly energy storage components, like those in the dc-link converter,
2) The control scheme required by a direct AC-AC conversion scheme is simpler than that used by a two-stage power conversion.

For maximum energy capture from the wind, high performance speed control **is** desired to enable the generator speed to closely track the value predicted by the wind turbine power-speed characteristic curve. This is realized by regulating the rotor current using a stator-flux, field-oriented scheme and a space-vector modulated matrix converter. The control scheme also enables flexible adjustment of the power factor. In this paper, the operating principles of this power generation scheme and the control method used are discussed. Simulation studies were carried out using a 7.5kW induction generator. The results under various operating conditions are presented. Features of the system and its modeling performance are scrutinized. The Wind energy conversion system configuration used in this work (DFIG with converters cascade and a capacity energy storage system in the dc link) is shown in Figure 1.

II. DOUBLY FED INDUCTION GENERATORS (DFIG)

The doubly fed induction generators (DFIG) are wound rotor induction generator. The DFIG is based on the concept, which corresponds to a variable speed wind turbine configuration with a wound rotor induction generator (WRIG) and a partial-scale power electronic converter on the rotor circuit, as illustrated. The stator is directly connected to the grid, whereas the rotor is connected through a back to back power electronic converter. The power converter controls the rotor frequency and thus the rotor speed. This concept supports a wide speed range operation, depending on the size of the frequency converter. Typically, the variable speed range is ±30% around the synchronous speed. The rating of the power electronic converter is only 25–30% of the generator capacity, which makes this concept attractive and popular from an economic point of view [3].

There are various advantages of DFIG reported as its controllability of both active and reactive power is better. The large rotor inertia smoothest the variations of wind speed and as a result it has fewer fluctuations in output power. The most important advantage of DFIG is its ability to get ride through fault by its uninterruptable operation. DFIGs connect to grid with selecting a good control; it has uninterruptable operation and can successfully ride through grid faults. The uninterruptable operation can be achieved by properly arranging the operation and control of the converters and using dynamic reactive compensation [4].

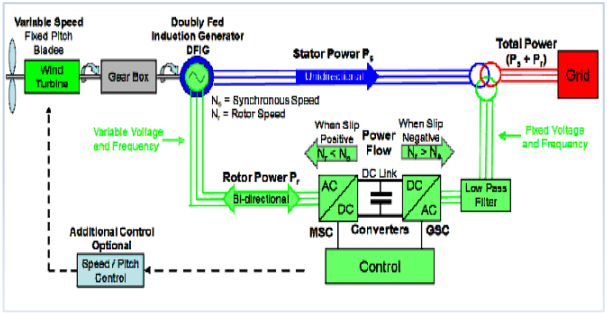

Figure 2. Power flow diagram of DFIG

The stator is directly connected to the AC mains, whilst the wound rotor is fed from the Power Electronics Converter via slip rings to allow DIFG to operate at a muddle of speeds in response to changing wind speed. Indeed, the basic concept is to interpose a frequency converter between the variable frequency induction generator and fixed frequency grid. The DC capacitor linking stator- and rotor-side converters allows the storage of power from induction generator for further generation. [4] To achieve full control of grid current, the DC-link voltage must be boosted to a level 18 higher than the amplitude of grid line-to-line voltage. The slip power can flow in both directions, i.e. to the rotor from the supply and from supply to the rotor and hence the speed of the machine can be controlled from either rotor- or stator-side converter in both super and sub-synchronous speed ranges. As a result, the machine can be controlled as a generator or a motor in both super and sub-synchronous operating modes realizing four operating modes. Below the synchronous speed in the motoring mode and above the synchronous speed in the generating mode, rotor-side converter operates as a rectifier and stator-side converter as an inverter, where slip power is returned to the stator. Below the synchronous speed in the generating mode and above the synchronous speed in the motoring mode, rotor-side converter operates as an inverter and stator side converter as a rectifier, where slip power is supplied to the rotor. At the synchronous speed, slip power is taken from supply to excite the rotor windings and in this case machine behaves as a synchronous machine [3, 4].

The mechanical power and the stator electric power output are computed as follows:

$P_r=T_m*W_r$ & $P_s=T_{em}*W_s$

For a loss less generator the mechanical equation in steady-state at fixed speed for a loss less generator

$T_m=T_{sm}$ and $P_m=P_s+P_r$

where,

S $(W_s-W_r)/W_s$ is defined as the slip of the generator

Generally, the absolute value of slip is much lower than 1 and, consequently, Pr is only a fraction of Ps. Since Tm is positive for power generation and since ωs is positive and constant for a constant frequency grid voltage, the sign of Pr is a function of the slip sign. Pr is positive for negative slip (speed greater than synchronous speed) and it is negative for positive slip (speed lower than synchronous speed). For super-synchronous speed operation, Pr is transmitted to DC bus capacitor and tends to raise the DC voltage. For sub-synchronous speed operation, Pr is taken out of DC bus capacitor and tends to decrease the DC voltage. Cgrid is used to generate or absorb the power Pgc in order to keep the DC voltage constant. In steady-state for a lossless AC/DC/AC

converter Pgc is equal to Pr and the speed of the wind turbine is determined by the power Pr absorbed or generated by Crotor. The phase-sequence of the AC voltage generated by Crotor is positive for sub-synchronous speed and negative for super-synchronous speed. The frequency of this voltage is equal to the product of the grid frequency and the absolute value of the slip. C_{rotor} and C_{grid} have the capability for generating or absorbing reactive power and could be used to control the reactive power or the voltage at the grid terminals.

III. MATRIX CONVERTER CONTROLLED DFIG

The matrix converter is a forced commutated converter which uses an array of controlled bidirectional switches as the main power elements to create a variable output voltage system with unrestricted frequency. It does not have any dc-link circuit and does not need any large energy storage elements.

A. System Configuration

In the generation system, an AC-AC matrix converter may be used to supply the variable-frequency voltages to the rotor terminals of the induction machine. Figure 3 shows schematics of the matrix converter-DFIG configuration and its simplified control scheme. The stator of the generator is connected directly to the utility grid. A matrix converter is inserted in the rotor circuit, giving direct AC-AC power conversion between the rotor circuit and grid.

The grid-side connection is made via a three-phase LC filter to suppress high-order harmonics. A matrix converter provides bidirectional power-flow control thereby enabling the DFIG to operate in either sub synchronous (or<ws) or super synchronous modes (w,>o,). In both modes the stator active power is generated from the DFIG and delivered to the grid. On the other hand, the rotor active power is either supplied to the machine in the sub synchronous mode or delivered to the grid in the super synchronous mode. Now the output power of a wind turbine at a specific wind speed varies with change of the turbine shaft speed.

The control objective is to ensure that the power developed by the turbine is a maximum at any wind speed. The control scheme must also maintain continuous power flow from the DFIG to the grid.[6]. To achieve this, a turbine shaft speed which results in a maximum turbine power must be determined and the DFIG is controlled so as to obtain the desired shaft speed. The desired shaft speed can be determined by an optimal power tracking algorithm which is not fully investigated in this present work.

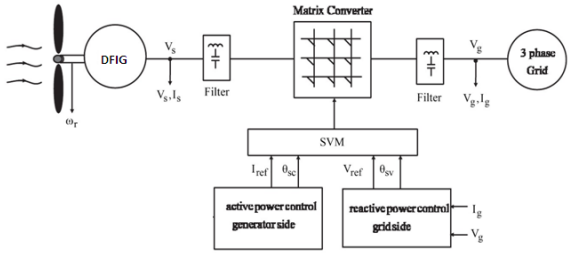

Figure 3. Conventional Matrix Converter in WECS

Instead, the stator active power is controlled directly assuming that a maximum generator developed power is known. The ideal machine stator power, denoted by P_s is used as the reference value for the DFIG power control loop. In the inner current control loop, the stator-flux vector position is used to establish a reference frame that allows the d and q axis components of the rotor current to be controlled independently. Adjustment of the q-axis component of the rotor current. i_{qr} controls either the generator developed-torque or the stator-side active power of the DFIG *(Ps).*Regulating the d-axis component, *jdr,* controls directly the stator-side reactive power flow *(Qs).*

B. Principle of Active and Reactive Power Control

To provide independent control of the stator active power P, and reactive power Qs of the DFIG, by means of rotor current regulation, it is necessary to define the dq components of the rotor currents in the stator-flux oriented reference frame and show that P, and Q, can be represented as functions of the individual current components. Subsequently, the P, and Qs commands can be used to determine the reference rotor currents. Stator-flux oriented control is used to regulate the rotor current. In this scheme the d components of the rotor current vector is aligned with the stator-flux linkage vector λs, hence the active and reactive currents supplied to the power grid become linear functions of the rotor current d and q components, given as

$$i_{qs}^{e} = \frac{Lm}{Ls} i_{qr}^{e} \quad \text{and} \quad i_{ds}^{e} = \frac{Lm}{Ls}(\lfloor i_{ms}^{s} \rfloor - i_{ds}^{e} \quad (1)$$

The magnitude of the stator magnetizing current vector i_{ms} is a constant determined by the supply voltage. The stator active and reactive power components may be given as

$$P_s = \frac{3}{2} V_{ds}^e i_{ds}^e + V_{qs}^e i_{qs}^e = \frac{3}{2} V_{ds}^e i_{ds}^e = -\frac{3}{2} W_e \frac{Lm}{Ls} i_{ms}^e i_{qr}^2 \quad (2)$$

$$Q_s = \frac{3}{2} V_{qs}^e i_{ds}^e + V_{ds}^e i_{qs}^e = \frac{3}{2} V_{qs}^e i_{ds}^e = -\frac{3}{2} W_e \frac{Lm}{Ls} i_{ms}^e i_{dr}^2 \quad (3)$$

Knowing L_{ms} , Ls, and ideal values of p_s^e and Q_s^e, the reference values for i_{dr}^e and j_{ds}^e can be calculated directly from the above equations.

C. Space Vector Modulation Control of the Matrix Converter

Once the input and output voltage values are specified for each sampling period, the space vector modulation (SVM) method can be directly applied to control the matrix converter[5,6,]. The method represents the three-phase input currents and output line-to-line voltages as space vectors. It is based on the concept of approximating a rotating reference voltage vector with those phased realizable on a matrix converter. For nine bidirectional switches, there are 27 valid switch combinations which may be divided into *5* groups [6,8].

The first group consists of six vectors whose angular positions vary with the change of input voltage vector. This group of vectors is not employed in the SVM method. The next three groups of switch combinations have two common features, namely, each of them consists of six vectors which all hold constant angular positions and each of them defines a six sextant hexagon. These, so named stationary vectors, are used to synthesize the desired output voltage vector. The remaining group comprising three zero vectors is also used in the method. The modulation process consists of two procedures: vector selection and vector on-time duration calculation. At a given time instant T , the SVM method selects 4 stationary vectors to approximate a desired reference voltage with the constraint of unity input power factor.

To achieve this. the amplitude and phase angle of the reference rotor voltage vector are calculated and the desired phase angle of the input current vector is determined in advance. The stationary vectors chosen should be adjacent to the sextant where the reference voltage vector locates. Moreover their magnitudes are equivalent to the maximum line-to-line input voltage at the given sampling instant. It is performed at every sampling interval. Note that the maximum achievable output voltage is limited to 86% of the input voltage due to the fact that the peak-to-peak output voltage cannot be greater than the minimum line-to-line input voltage. However, this restriction may not be a significant drawback for this application.

IV. SIMULATION AND RESULTS

A 10 MW wind farm consisting of five wind turbines each of 2 MW connected with a 25 kV distribution system. This grid-tie wind turbine model based on DFIG and three-phase-to-three-phase matrix interface converter has been carried out in Matlab/Simulink environment. The complete Simulink model is shown in figure 4.

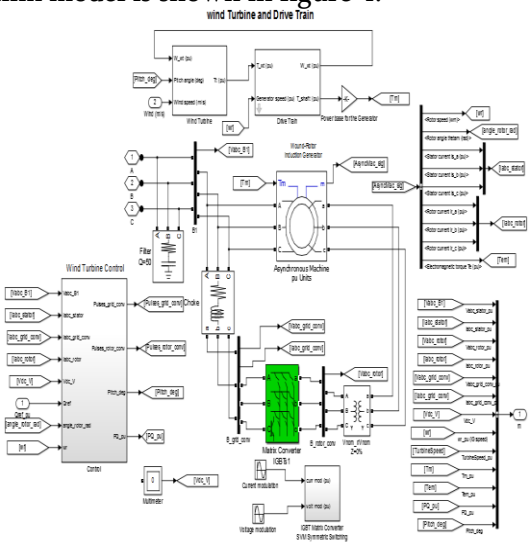

Figure 4. Complete simulink model of wind turbine with Matrix converter

This system consists of a three-phase matrix converter (MC) constructed from 9 back-to-back IGBT switches. The MC is supplied by an ideal 60Hz three-phase source and drives a static resistive load at 60Hz. The switching algorithm is based on an indirect space-vector modulation. Indirect space-vector modulation allows direct control of input current and output voltage and hence allows the power factor of the source to be controlled. The switching algorithm utilizes a symmetric switching sequence. LC filters are also included in this model so that the output waveforms can be seen clearly.

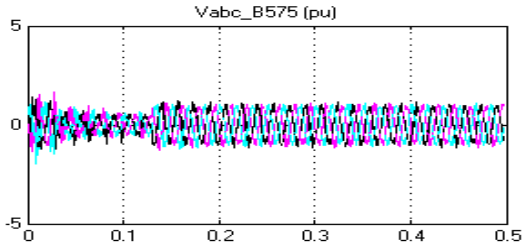

Figure 5 Voltage waveform of Grid connected to wind energy system

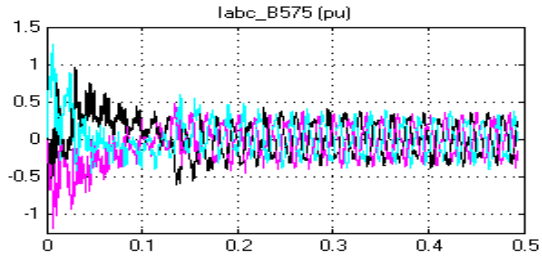

Figure 6. Current waveform of Grid connected to wind energy system

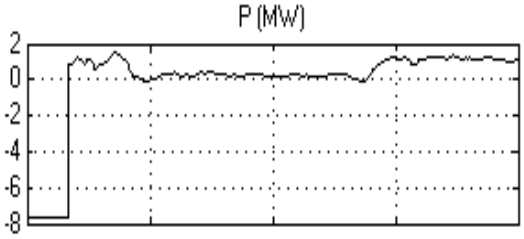

Figure 7. Active power of wind turbine

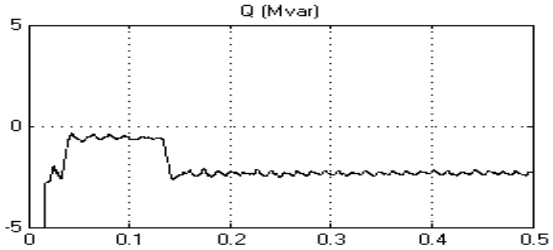

Figure 8. Reactive power of wind turbine

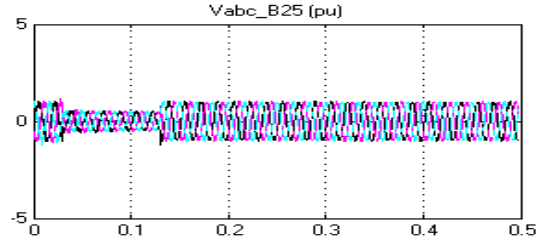

Figure 9. Voltage waveform of wind turbine

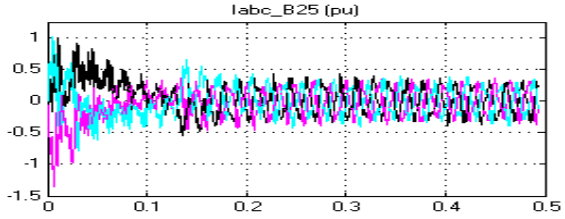

Figure 10. Current waveform of wind turbine

DIFFERENT WIND SPEED

Table 1

Wind Speed (M/Sec)	Line to Line Voltage (volts)	Frequeny (Hz)	Rotor Speed (rad/sec)	Active Power (kW)	Reactive Power (kVAR)
7	245	38.5	105	5.4	140
9	312	43.2	130	6.95	180
12	390	50	152	8.5	270
14	438	55.8	174	10.8	420
16	487	62.2	205	14.28	580

V. CONCLUSION

This paper presented a wind generation system employing in the model of MC and DFIGURE When the speed increases, both frequency and amplitude of the output voltage from the DFIG also increases. In order to obtain the constant output voltage with constant frequency, the synchronous generator is coupled with the matrix converter. A controlled rectifier rectifies the output voltage of DFIG and rectified output is given to the inverter. As there is no DC link element between the converter and the inverter, the converter produces the constant DC voltage irrespective of wind velocities. The constant DC voltage from the converter is given to the input of inverter to obtain an AC output voltage of constant amplitude with constant frequency. There by constant output voltage with constant frequency is obtained from the proposed Wind Energy Conversion Scheme. The MC, controlled by SVM, enables excellent transient response while sinusoidal current waveforms are dominant with grid currents in-phase with the grid voltage for unity power factor.

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In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Rectangular Microstrip Patch Antenna Design

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ABSTRACT

This article presents the design of Rectangular Microstrip Patch antenna for communication. The simple patch antenna can be designed by varying the substrate and the thickness of the substrate. In Microstrip patch antenna (MPA) design, choosing the substrate is difficult task because, the designer should select the proper substrate material, to get the proper Gain value, Radiation pattern, Return loss and Impedance bandwidth. This paper presents how the rectangular Microstrip patch antenna can be designed and the performance of patch antenna varies when we are changing the substrate thickness and substrate materials. The proposed antenna operates at a band of WiMAX, Wi-Fi and ISM.

Key words: Rectangular MPA, Wi-Fi and ISM.,

I. INTRODUCTION

The Microstrip patch antenna contains very compact in size, it requires less power, fast data transmission and better return loss. The challenging task in the antenna design is Electromagnetic Interference and Compatibility (EMI/EMC). So we need to analyse the performance of the proposed antenna by varying the substrate materials. The proposed antenna is used for most of the ISM and ultra-wide band applications. In this article we study about the different substrate materials used in Microstrip patch antenna design and the thickness of the substrate. The simple patch antenna is shown in the figure (1)

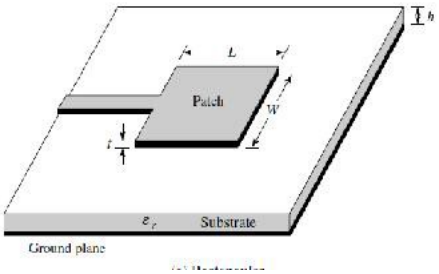

Figure 1

The Patch antenna consists of Ground plane, substrate, Patch and Feed line. It gives the different Antenna parameters, Metamaterial as a composite material structure that exhibits a special property like negative refractive index or left-handed materials. It gives a polarization in negative direction because of negative μ and negative ε. The Metamaterial can enhance the directivity, gain of the patch antenna and reduce the return loss. The variation in gap size of Split ring resonator (SRR) improves the Bandwidth of patch antenna. These Metamaterial structures miniaturize the antenna, inducing the resonator.

Antenna design

The Microstrip patch antenna can be designed using the theoretical calculation using the steps.

Step1: The width of the patch can be calculated using,

$$W = \frac{c}{2f_0}\sqrt{\frac{2}{\epsilon_r + 1}}$$

Step 2: The effective dielectric constant,

$$\varepsilon_{reff} = = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{w}\right]^{\frac{-1}{2}}$$

Step 3: The length of the patch,

$$\Delta L = 0.412h \left[\frac{(\varepsilon_{reff}+0.3)(\frac{w}{h}+0.264)}{(\varepsilon_{reff}-0.258)(\frac{w}{h}+0.8)}\right]$$

Step4: Effective length of the patch,

$$L_{eff} = \frac{c}{2f_o\sqrt{\varepsilon_{reff}}}$$

Step5: Final length of the patch and ground plane

$$L = L_{eff} - 2\Delta L$$

$$W_g = 6h + W$$
$$L_g = 6h + W$$

The patch design is shown in the figure (2),

The calculated width and length of the patch can be used to simulate the two rectangular patch connected one with other.

II. RESULT AND ANALYSIS

The rectangular patch can be created for the width W=25.2mm, Length L=18.2mm, thickness 1.6mm, FR4 substrate and the gain -0.25dB is obtained.

The antenna gain value changes to -1.2dB for the substrate material RT Duroid 5880 of thickness 1.6mm. The result of rectangular patch can be analyzed using the patch simulation. From the above analysis the FR4 substrate gives the gain value minimum at the frequency 5.1GHZ, when the thickness increases the return loss increases and the frequency decreases also the antenna performance can be increased. The gain, S-parameter and Magnitude analysis can be shown in the graph given below.

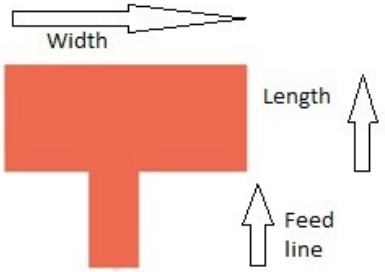

Figure 2

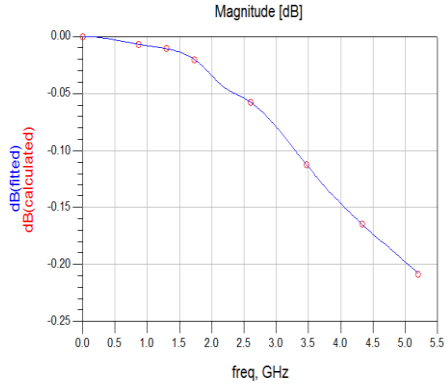

Figure 3

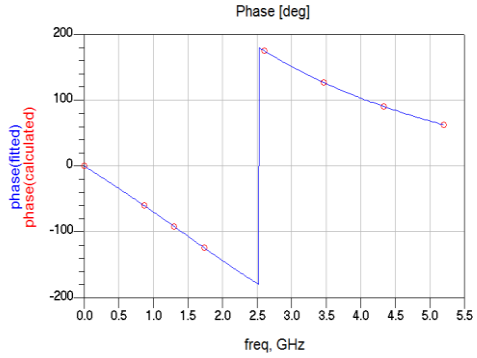

Figure 4

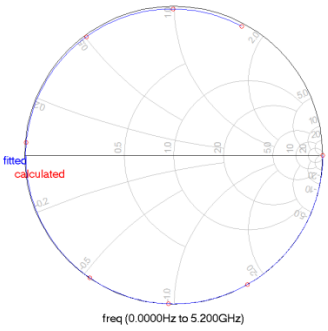

Figure 5

III. CONCLUSION

The proposed design was simulated using the advanced design system (ADS), the substrate materials

used for the design are FR4 and RT duroid5880. The rectangular patch gives the better radiation for different frequency band. The thickness of the substrate can be 1.6mm,2.2mm,4.4mm etc., are used for the patch design, Most of the patch antennas are designed using the FR4 substrate but in this design RT duroid5880 is also used for patch design, it is observed that the gain varies when we are varying the substrate material, it gives a better radiation pattern and Return loss. The antenna is used in WiMAX, Wi-Fi and ISM band applications.

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Organized By : CIrcuit Branches of SCSVMV, (EEE, ECE, EIE & Mechatronics) , Kanchipuram, Tamil Nadu, India
In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Simulation Study of 1O Fc-Tcr using ANN Method

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ABSTRACT

In simple power system, source and load are connected by the wires or line conductors. Overhead transmission lines are introduced to transmit huge amount of power with high voltage (HV) /extra high voltage level (EHV) of power frequency. The load end voltage is less than the source end voltage magnitude mostly, except no load and lightly loaded conditions. Consequence of that a device needed at the load end/receiving end to retain the voltage constant. Synchronous condensers are used followed by static VAr compensators. Mechanical switches are replaced by power electronics switches. FACTS devices are developed to improve the efficiency of power transmission either series or shunt or series and shunt combination successfully. However fixed capacitor thyristor controlled reactor is a more popular for VAr compensation either Transmission or distribution system or individual load. A single phase FC-TCR type VAr compensator suggested, designed and implemented in a simple distribution system. Characteristics behaviour of FC-TCR are studied using the derived model. MATLab/Simulink Model constructed and tested with the derived analytical model. Artificial neural network based controller implemented to generate the gating signal of the FC-TCR.

Keywords: FC-TCR, ANN, MATLab simulation

I. INTRODUCTION

Over the last two decades, voltage instability problem in power system has become one of the most important concerns in the power industry. The ability to transfer reactive power from generating station to the load centre during steady-state operating conditions is a major problem of voltage stability. A system mainly enters a state of voltage instability when a disturbance, increase in load demand, or change in system condition causes a progressive and uncontrollable decline in voltage. Voltage instability and the problem of voltage collapse can cause the major blackout in the power system.

Higher reactive load causes for high transmission and distribution losses. The presence of highly inductive loads is detrimental to the power system and an increase of such loads leads to increase in reactive power demand thus decreasing power factor of the system resulting in higher losses.The presence of capacitive loads causes supply of reactive power, resulting in increase in voltage and losses.

Placing FACTS devices like SVC, in a suitable location will help to maintain bus voltages at a desired level and also to improve the voltage stability margins [5]. The SVC devices such as Thyristor Switched Capacitor (TSC) and Thyristor Controlled Reactor (TCR) can deliver and absorb the reactive power respectively is shown in Figure 1.

ANN based control can be adopted on SVC to improve dynamic stability, reactive power control and voltage control.

An initial requirement for the use of ANN in this application is to train the ANN with a number of data generated in real situations. Then ANN is tested to get desired output states from a number of input states.

In this paper, the steady state operating characteristics of the power system is obtained for a five bus system from load flow analysis using Newton-Raphson method in ETAP software for varying load conditions and power factors .The results from load flow analysis are used for training the Artificial Neural Network (ANN). In this application, ANN is trained to predict the combination of capacitors and inductor for various loads and power factors. The reactive power demand and load bus voltages are given as inputs. Thus voltage regulation in the 5 bus system is obtained by placing the SVC device in optimal position and controlling their ON/OFF condition by ANN for varying load conditions. The entire ANN is implemented in dsPIC30F4011. The switching of SVC devices are shown by LED blinking for the 3 phase 5 bus system. For the hardware, the voltage regulation in the single phase induction motor connected through the transmission line is considered. The real power, reactive power, load voltage are given as inputs to the DSPIC , which decides the combination of the fixed capacitor(as the load is inductive) and TCR with firing angle to meet the reactive power demand. High frequency pulse triggering method is used for triggering purpose.

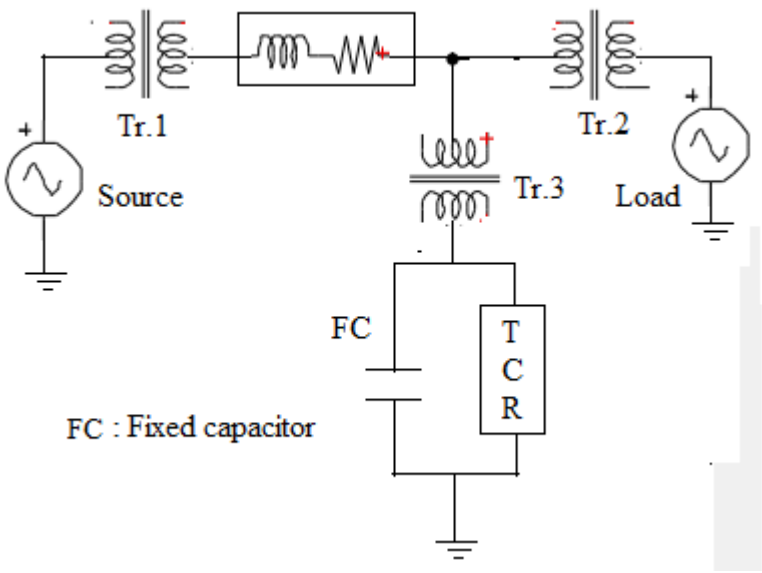

Figure 1. Single line diagram of single phase in distribution system with FC-TCR scheme

II. PROPOSED SCHEME

The term static VAR system has been adopted to apply to a number of static VAR compensation devices for use in shunt reactive control. These devices consist of shunt connected, static reactive elements (linear or nonlinear reactor and capacitor) configured into a VAR compensating system, and their distinction is that the shunt reactive power flowing in these devices is controllable over some rated range of VARs. The basic system consists of parallel combination of fixed capacitors and thyristor switch by an angle α, in each half cycle (α increased from 90° to 180°) the technique of controlling the conduction intervals of the thyristor switch, generate harmonic current components [6]. Fast response and the capability of balance load make the fixed capacitor, thyristor controlled inductor particularly advantageous for compensating those loads which present rapidly at various unbalanced conditions. In this study capability of ANN is used to recognize unbalance conditions and to provide proper firing angle as quickly as possible for thyristors which provide reactive power to balance the system. FC-TCR is shown in Figure 1.

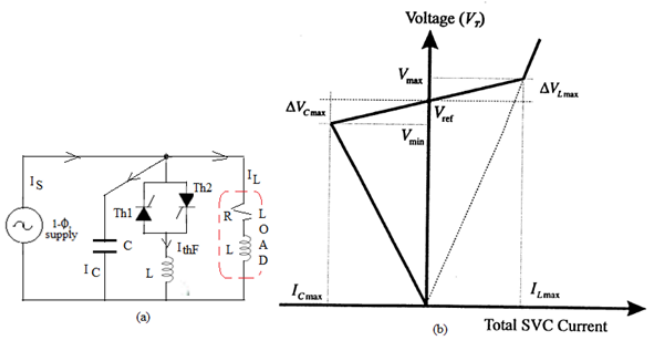

Figure 2. illustrates (a) single phase FC-TCR with load (b) VI characteristic

Figure 2 illustrates the basic configuration of single phase static compensator FC-TCR. In this case capacitor represents a switched capacitor bank either as mechanically switched or thyristor switched in binary sequential steps as explained earlier and L represents reactor with phase angle control [0].

The controllable range of TCR firing angleα extends from90^o to 180^o. In case of ideal reactor of L Henry firing angle of 90 results in full conduction with continuous sinusoidal current flow. Practically all six air cored reactors are designed with an average resistance of 10 Ω and inductance of 230 mH. The following "(5)" [5] illustrates the relation between firing angle α and the current through inductor I_L for ideal inductor having resistance tending towards zero while "(6)" represents the practical case considering resistance R Ω.

$$I_L = \left(\frac{V}{\omega L}\right)\left[1 - \left(\frac{2}{\pi}\right)\alpha - \left(\frac{1}{\pi}\right)\sin 2\alpha\right] \quad (1)$$

$$I_L(\alpha) = \frac{V_m}{\sqrt{R^2 + {X_L}^2}}\left[\frac{1}{2\pi}\left\{(\beta - \alpha) + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right\}\right]^{1/2} \quad (2)$$

Above equations concludes two cases such as,

Case: 1 If α = θ, then the firing angle is equal to phase angle, therefore $\sin(\beta - \theta) = \sin(\beta - \theta) = 0$ and conduction angle = β - α = π

Case: 2 since, conduction angle should not exceed π, therefore the control range of TCR lies between θ and π i.e. $\theta \le \alpha \le \pi$

The equation (2) re rewritten as

$$I_F(\alpha) = \frac{V_L}{Z} = V_m Y_{TCR(\alpha-\theta)} \quad (3)$$

$$Y_{TCR(\alpha-\theta)} = \left[\frac{1}{2\pi}\left\{(\beta - \alpha) + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right\}\right]^{1/2} \quad (4)$$

Thus the TCR acts like a variable admittance. By varying the firing angle α admittance changes and consequently fundamental current component which in turn gives rise to variation of reactive power absorbed by reactor. Hence if $\alpha = \theta = 85.5^o$ continuous conduction of current take place. However, if firing angle is increased beyond this, non-sinusoidal currents are generated and hence harmonics get introduced. The rms value of nth order harmonic is expressed as

$$I_1(\alpha) = \frac{V}{Z} \times \frac{2}{\pi}\left[\frac{-2\cos(\alpha - \theta)}{n}\sin\, n(\alpha - \theta) + \frac{\sin(n-1)(\alpha - \theta)}{n-1} + \frac{\sin(n-1)(\alpha - \theta)}{n-1}\right] \quad (5)$$

Where, n = 2k+1 and k = 1, 2,3…

III. CONTROL STRATEGY

Figure 3(a) illustrates unique control scheme of SVC possible to implement either in small or large disturbances occurred in power system. . It comprises with different blocks based on TCR suceptance calculation, error calculation and tuning circuit.

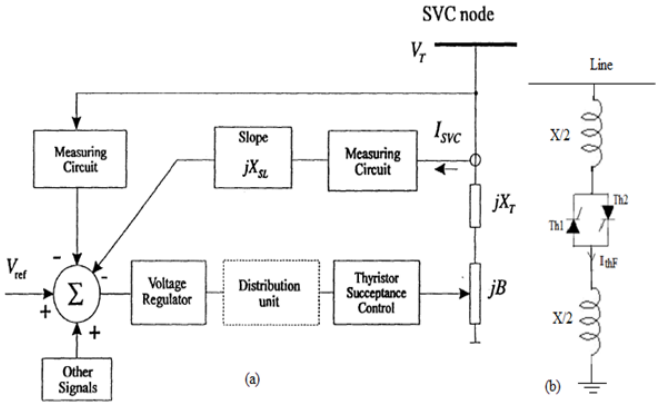

Figure 2. SVC control block diagram

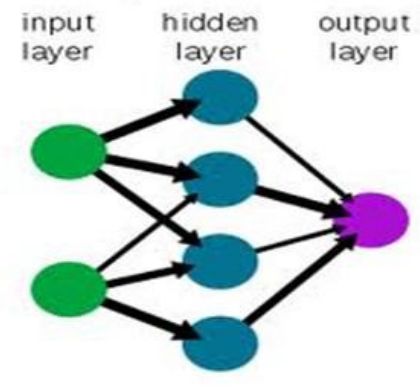

Figure 3. structure of ANN

In order to implement ANN as a decision making block of this control, ANN should trained in such way that firing angle of TCR with respect to suceptance variations. Therefore the total suceptance of the TCR divided into different intervals and calibrated with delay angleα, whereαlies between zero and maximum of 90^oi.e. $0 < \alpha < \frac{\pi}{2}$. If we want to the control over 180^o degree the TCR split into two halves as shown in Figure 3(b). The control range could vary between zero degrees to 180 degree by making the reactance value of reactor into two half and connect the thyristors as shown in Figure 3(b)

3.1 IMPLEMENTATION OF ANN

Consequence of above cited calculation could be carried out by artificial neural network (ANN) is a network of simple processing elements called neurons, which can exhibit complex global behaviour determined by the connection between the processing elements. This is an artificial representation of our human brain. The back propagation algorithm is used in layered feed-forward ANN. This means that the artificial neurons are organized in layers, and send their signals "forward", and then the errors are propagated backwards. These models have the three subgroups of processing elements such as Input layer, Hidden layer and Output layer. Different activation functions can be used in these layers to get the output of ANN. Figure 4 shows the structure of ANN.

In this paper, hyperbolic tangent sigmoid transfer function is used for input layer. Log-sigmoid transfer function is used for hidden layers and output layers. Gradient descent with momentum back propagation strategy is used for ANN.

IV. MATLAB BASED SIMULATION OF SINGLE PHASE FC-TCR

The proposed scheme of single phase FC-TCR as shown in Figure 2 (a) is constructed using the power system tool box of MATLab/Simulink version 16 is shown in Figure 5 and Figure 6. Designed value of TCR, fixed capacitor and load is shown in Table-1

Table 1. Designed Values Of Fcr

TCR inductance	:	65mH
Fixed capacitor	:	65 Micro Farads
Load resistance	:	4.5 ohm
Load Inductance	:	60 mH
Line inductance	:	10mH
voltage	:	230V
frequency	:	50 Hz

2.1. Without FC-TCR

A load resistance of 4.5 ohm and inductance of 60mH connected across a source voltage of 230 volts along

with a series inductance of 10 mH. This series inductance represents the line inductance of the transmission line is shown in Figure 5. The source and load considering as a sending end and receiving end respectively of a transmission line for this study.

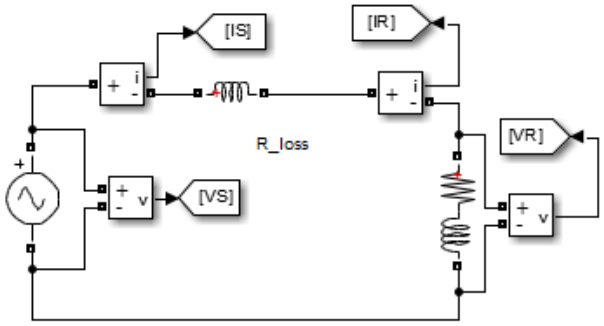

Figure 4. Simulink connection of simple power system model

Figure 6 illustrates the measuring blocks of the proposed study single phase power system as shown in Figure 5. RMS values of both measured current and voltage is calculated by using a RMS block is shown in Figure 6.

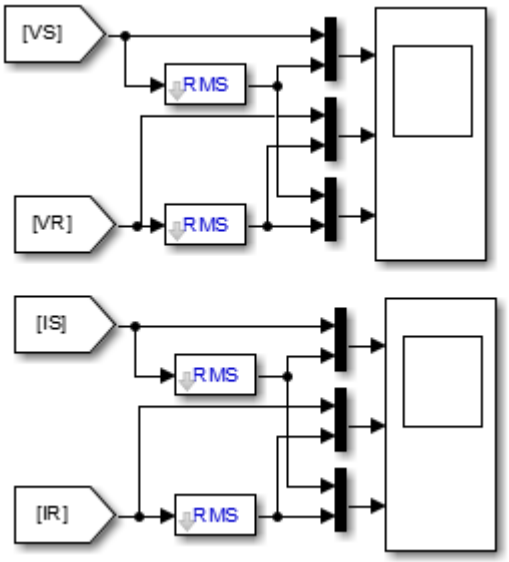

Figure 5. measurement blocks of single phase power system as shown in Figure 5

2.2. With FC TCR

A load resistance of 4.5 ohm and inductance of 60mH connected across a source voltage of 230 volts along with a series inductance of 10 mH. This series inductance represents the line inductance of the transmission line is shown in Figure 7. The source and load considering as a sending end and receiving end respectively of a transmission line for this study. In order to compensate the reactive power drawn by the load is compensated by shunt connected FC-TCR. A 65 micro farad capacitor directly connected to the source after the series inductance, another 65 milli henry inductance is connected across the fixed capacitor so called fixed capacitor thyristor controlled reactor is shown in Figure 7, Capacitor current is controlled by controlling the fundamental current flowing through the reactor. Thus capacitive currents are controlled so that burden of the source is reduced.

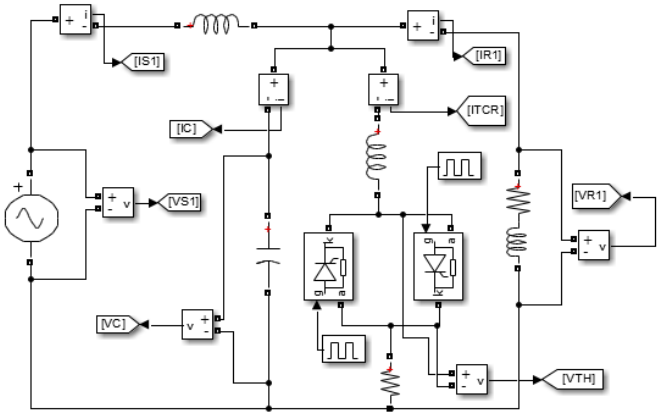

Figure 6. Simulink connection of FC-TCR

Figure 8 illustrates the measuring blocks of the proposed study single phase power system as shown in Figure 7. RMS values of both measured current and voltage is calculated by using a RMS block is shown in Figure 8.

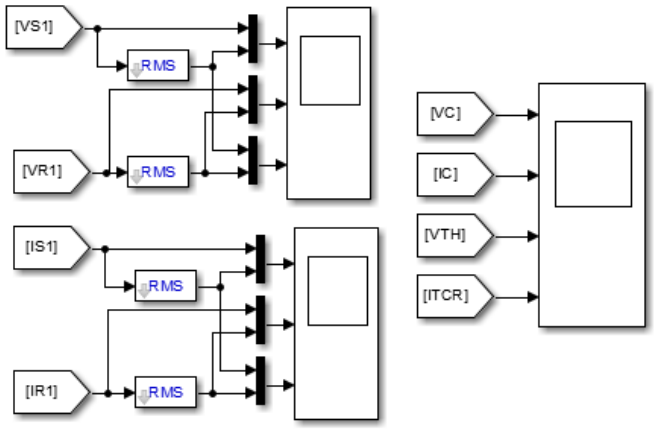

Figure 7. measuring block of FC-TCR connection as shown in Figure 7.

The above cited circuits are connected in MATLab/Simulink software version 16 and completed the simulation for 3 seconds of simulation time. The results are presented in forth coming sections.

V. RESULTS

Simulation experiment is completed by using the designed parameters as shown in Table-1. Figure 9 illustrates the voltage waveforms of both sending (source side) end and receiving end (load side) of the proposed study system and its RMS values also. It shows source voltage magnitude is slightly more than the load side voltage.

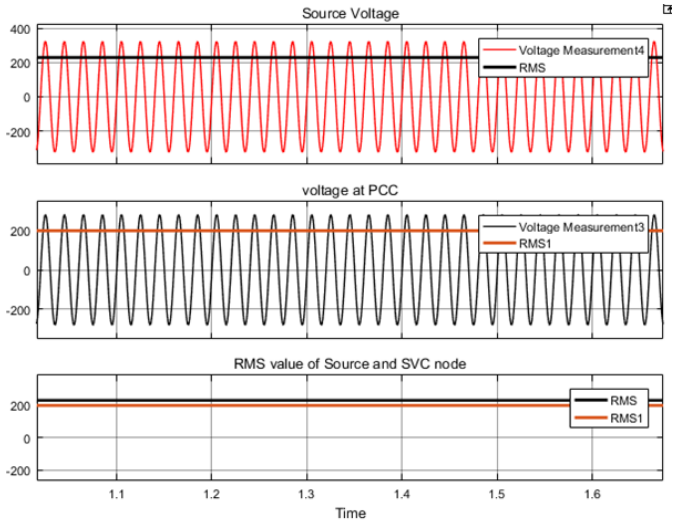

Figure 8. simulated voltage waveforms at source and load side (receiving end) without FC-TCR

Figure 10 illustrates the current waveforms having same magnitude. Obviously it is true because no other devices are connected between source and load.

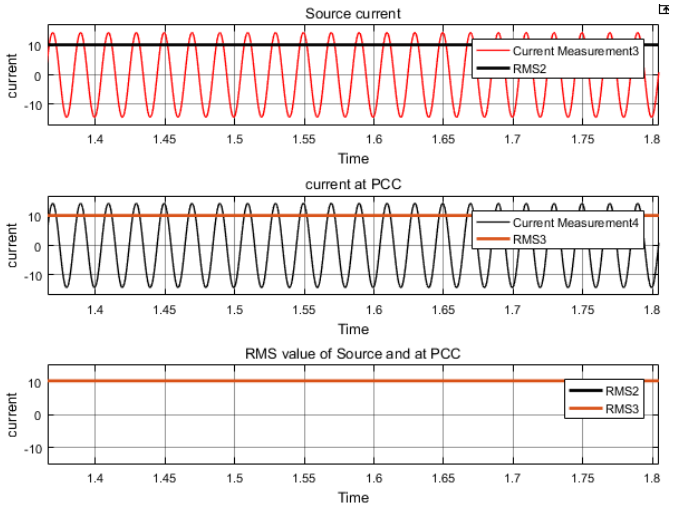

Figure 9. simulated current waveforms at source and load side (receiving end) without FC-TCR

Figure 11 illustrates the voltage waveforms of both sending (source side) end and receiving end (load side) of the proposed study system with FC-TCR and its RMS values also. It shows source voltage magnitude is slightly more but less than earlier load side voltage. Obviously it is correct because shunt connected devices not able to increase the voltage magnitude until external active source is not connected or if source is connected externally voltage profile will increase at point of common coupling (PCC).

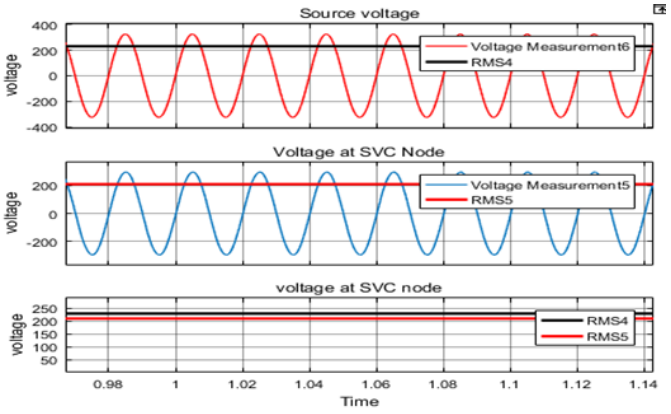

Figure 10. simulated voltage waveforms at source and load side (receiving end) with FC-TCR

Figure 12 illustrates the current waveforms having less magnitude in source and load current is same value shows that FC – TCR supplying reactive current required by the load. Obviously it is true because shunt connected SVC delivering the controllable current component either leading or lagging at PCC.

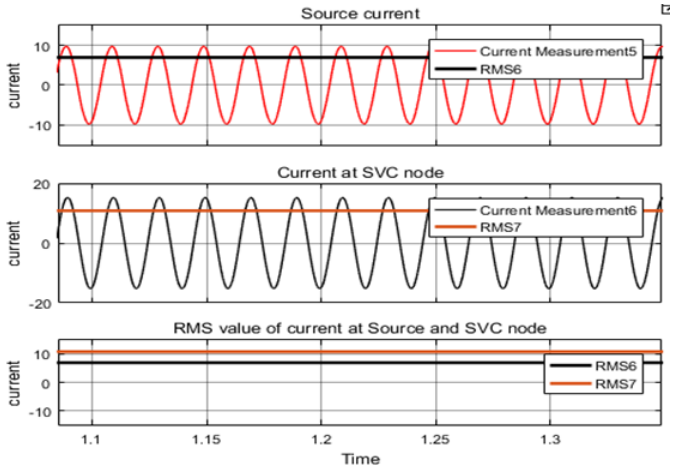

Figure 11. simulated current waveforms at source and load side (receiving end) with FC-TCR

Figure 13 illustrates the voltage and current waveforms of fixed capacitor, voltage across the thyristor and current flowing through the TCR for the delay angle of 30^{o}.

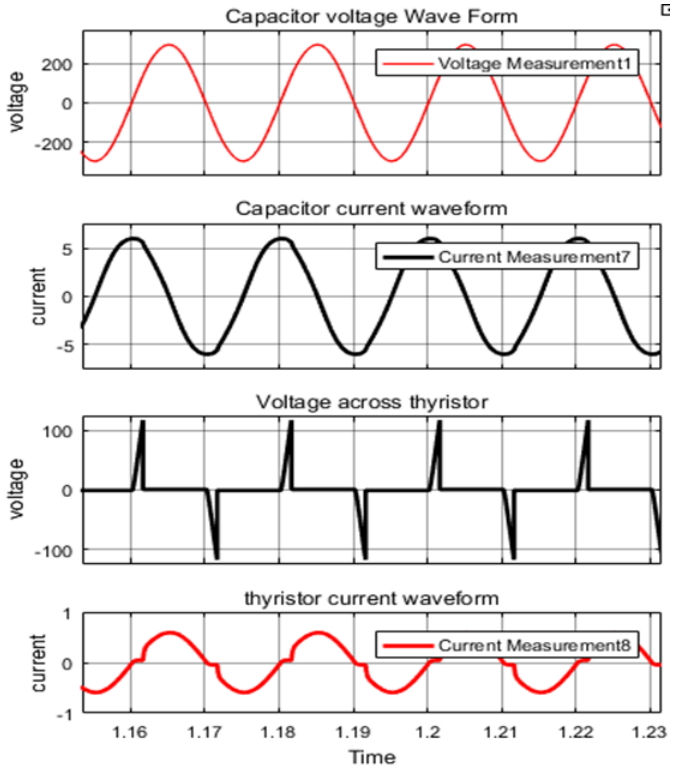

Figure 12. simulated waveforms across fixed capacitor, TCR

VI. CONCLUSIONS

Thus from the above result it is conclude that the Static VAr compensator(SVC) will control the voltage stability of the system and also maintains the dynamic performance of the system by controlling the suceptance of the reactor in such a way that the current drawn by the capacitor is controlled. The control range can be decided by the thyristor controlled reactor and fixed capacitor. From the simulation results it is observed that reactive power variation is smoother by using FC-TCR.

VII. ACKNOWLEDGEMENTS

The authors acknowledge the Management of SCSVMV University, Tamil Nadu, India, 631561, and Head of the department of Electrical and Electronics Engineering, for the support and keen interest in promoting the research and development in the division by providing the facilities and time

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National Conference on 'Innovative Research on Robotics, Circuits and Technology' (IRCT 2018)
Organized By : CIrcuit Branches of SCSVMV, (EEE, ECE, EIE & Mechatronics) , Kanchipuram, Tamil Nadu, India
In Assotiation with International Journal of Scientific Research in Science, Engineering and Technology
© 2018 IJSRSET | Volume 5 | Issue 1 | | Print ISSN: 2395-1990 | Online ISSN : 2394-4099

Power Quality Improvement in Grid from Wind Turbine by Using Shunt Hybrid Active Filter

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ABSTRACT

This paper presents a shunt hybrid active power filter for power quality improvement. The SHAPF improves the source power factor to unity, provides reactive power compensation and reduces the source harmonics. Therefore the power quality can be enhanced efficiently by using this hybrid active power filter. Finally, representative simulation results of a three phase shunt hybrid active power filter are presented to verify the effectiveness of SHAPF in power quality enhancement.

Keywords: Active power filters (APFs), hybrid active power filters (HAPFs), passive power filters (PPFs), power quality enhancement.

I. INTRODUCTION

In today‘s environment, electronic loads are very sensitive to harmonics, sags, swells and other disturbances. Among these parameters, current harmonics have become a growing power quality concern. One more power quality issue is reactive power compensation. Reactive power is required to maintain the voltage to deliver active power. When there is not enough reactive power, the voltage sags down and it is not possible to push the power demanded by loads through the lines. Though reactive power is needed to run many electrical devices, it can cause harmful effects on electrical appliances. So the reactive power compensation is very important in electrical power system. So, power quality become important in the power system.

In the mid-1940s, passive power filters (PPFs) have been widely used to suppress current harmonics and compensate reactive power in distribution power systems [1] due to their low cost, simplicity, and high-efficiency characteristics. But, PPFs have many disadvantages such as low dynamic performance, resonance problems, and filtering characteristics that are easily affected by small variations of the system parameters [2]–[7]. Since the concept of an ―active ac power filter‖ was first developed in 1976 [1], [5], research studies on active power filters (APFs) for current quality compensation are getting more and more attention. APFs can overcome the disadvantages in PPFs, but their initial and operational costs are relatively high [2]–[6] because the dc- link operating voltage should be higher than the system voltage. This slows down their large scale application in distribution networks.

In addition, different hybrid active power filter (HAPF) topologies composed of active and passive components in series and/or parallel have been proposed, aiming to improve the compensation characteristics of PPFs and reduce the voltage and/or current ratings (costs) of the APFs, thus leading to improvements in cost and performance [2]–[13]. The

HAPF topologies in [2]–[8] consist of many passive components, such as transformers, capacitors, reactors, and resistors, thus increasing the size and cost of the whole system.

A transformer less shunt hybrid active power filter(SHAPF) has been recently proposed and applied for current quality compensation and damping of harmonic propagation in distribution power systems [12]–[13], in which it has only a few passive components. In this paper, an instantaneous power control scheme for the three-phase SHAPF is proposed and studied. In the following, a transformer less three-phase and its single-phase fundamental equivalent circuit model are illustrated in Section II. Then, the instantaneous power theory for hybrid active filter control is deduced in Section III. The simulation verification of the proposed HAPF is presented in Section IV.

II. TRANSFORMERLESS THREE PHASE HYBRID ACTIVE FILTER

The schematic diagram of the shunt hybrid Active power filter (SHAPF) is presented in Fig 1. This configuration of hybrid filter ensures the compensation of the source current harmonics by enhancing the compensation characteristics of the passive filter besides eliminating the risk of resonance. It provides effective compensation of current harmonics and limited supply voltage distortion. The hybrid filter is controlled such that the harmonic

currents of the nonlinear loads flow through the passive filter and that only the fundamental frequency component of the load current is to be supplied by the ac mains.

The HAPF topologies in [2]–[9] consists many passive components which increases the size and cost of the whole system which makes the topology non preferable. As a result, a shunt hybrid power filter topology named transformer less hybrid filter was proposed. The series connection between the passive filter and the voltage source converter is completed without using any matching transformer.

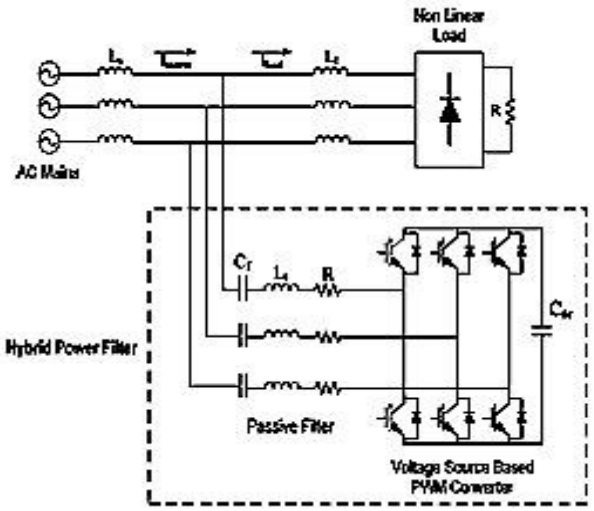


Figure 1. Transformerless Shunt Hybrid Power Filter

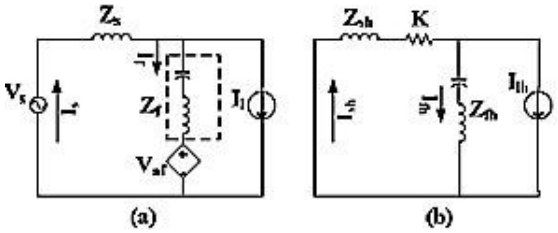


Figure 2. (a) Single Phase Equivalent Circuit (b) Harmonic Equivalent Circuit

In order to clarify the compensation characteristic of the shunt Hybrid Power Filter, the system can be simplified by obtaining its single phase equivalent circuit as indicated in (Fig 2) where Z_s represents the source impedance and Z_f represents the passive filter impedance. The non linear load is shown as an ideal current source (I_l), and the APF is considered as a voltage source.

If the active power filter terminal voltage is assumed to have no fundamental component, voltage across the PWM inverter can be represented as K x I_{sh} at harmonic frequencies where _h' stands for the harmonic components and K represents the feedback gain.

Hence, assuming the source voltage to be pure 50Hz and considering the current directions as in Fig 2, the following equations can be obtained by applying Kirchhoff's voltage law.

$$V_{sh} - I_{sh}Z_{sh} - I_{sh}Z_{fh} - V_{af} = 0 \quad (1)$$

Where,

$$V_{sh} = 0 \text{ and } V_{af} = K.I_{sh}$$

$$I_{sh} = I_{lh} + I_{fh} \quad (2)$$

Combine (1) and (2),

$$I_{sh} = Z_{sh} / (Z_{fh} + Z_{sh} + K) \quad (3)$$

Equation (3) indicates that as the active power filter is connected to the system, feedback gain K acts as a damping resistor which suppresses the resonance between the supply and the passive filter. Theoretically, as K approaches to infinity, the harmonic content of the source current goes towards zero. However due to stability problems in the control loop, the gain K should be limited to certain values.

III. INSTANTANEOUS POWER CONTROL TECHNIQUE

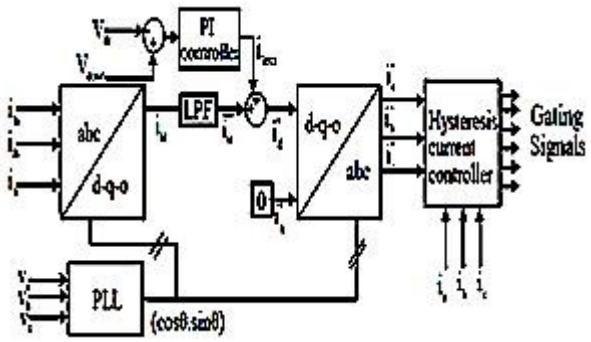


Figure 3. Instantaneous power control technique

Figure 3 shows the instantaneous power control block diagram for the three phase shunt hybrid active power filter, which consists of three parts: instantaneous power theory, calculation of current reference and regulation of DC voltage.

A. Instantaneous power theory

The control strategy of the active filter is based on the generation of reference source currents. These reference source currents are generated using synchronous frame reference theory (SRF). The load currents (i_{la}, i_{lb}, i_{lc}), PCC voltages (V_a, V_b, V_c) and dc link voltage (V_{dc}) are sensed and used as feedback signals. The load currents in a-b-c coordinates are transformed in to d-q coordinates using Park's transformation. The d-q components of the load currents are calculated as,

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos(\theta - a) & \cos(\theta + a) \\ \sin\theta & \sin(\theta - a) & \sin(\theta + a) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

Where cosθ and sinθ are obtained from three phase PLL. These d-axis and q-axis currents can be separated into two parts namely average and oscillatory parts as,

$$I_d = \bar{I}_d + \tilde{I}_d$$

$$I_q = \bar{I}_q + \tilde{I}_q$$

The reference source currents in d-q coordinates are transformed into a-b-c coordinates using inverse Parks transformation and it is expressed as,

$$\begin{bmatrix} I_a^* \\ I_b^* \\ I_c^* \end{bmatrix} = \left(\frac{2}{3}\right) \begin{bmatrix} \cos\theta & \sin\theta \\ \cos(\theta - a) & \sin(\theta - a) \\ \cos(\theta + a) & \sin(\theta + a) \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix}$$

where,

$$a = \frac{2}{3}\pi$$

B. Calculation of current reference.

The reference source currents (i_a^*, i_b^* and i_c^*) are compared with the sensed source currents (i_a, i_b and i_c). The switching sequence of the IGBTs is generated from the PWM current controller. The current errors are calculated as,

$$I_{a\_err} = i_a^* - i_a$$

$$I_{b\_err} = i_b^* - i_b$$

$$I_{c\_err} = i_c^* - i_c$$

This error signals are fed to the current controller for switching of the IGBTs of the active filter. ***C. Regulation of dc voltage***

DC link voltage control is maintained by a proportional plus integral (PI) regulator. DC link capacitor voltage is build up and regulated without any external power supply. In order to meet the loss inside the active power filter, an amount of active power is required and generated by producing a fundamental ac voltage controlled by the active filter. Since fundamental leading current flows through the passive filter, the active filter should generate a fundamental voltage that is in phase with this leading current. As a result, the current reference obtained in this control loop is added to the reactive current component.

IV. SIMULATION RESULTS

A. No Load Change Condition

1) Before Compensation

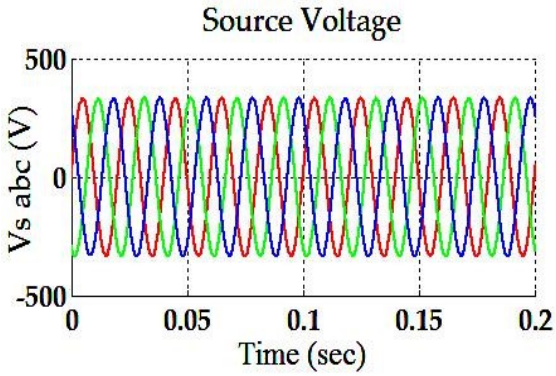


Figure 4. (a)

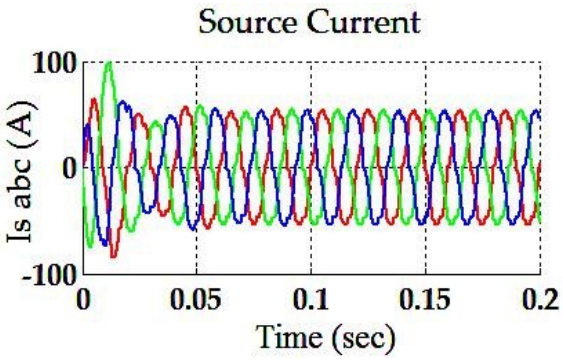


Figure 4. (b)

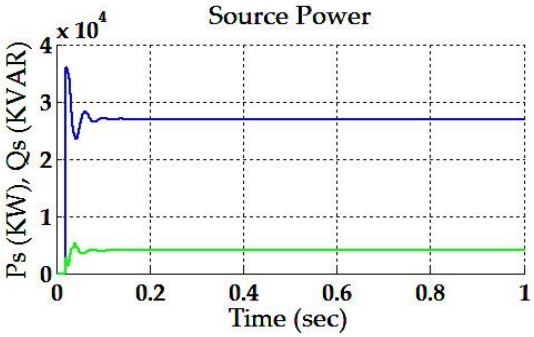


Figure 4. (c)

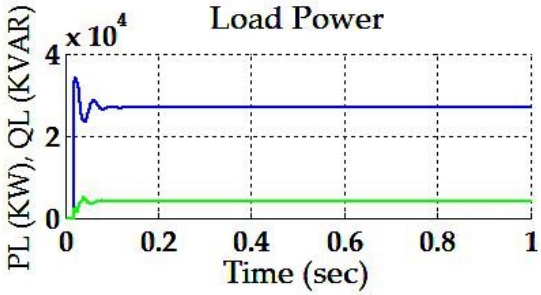


Figure 4. (d)

Figure 4. (a),(b),(c) and (d) shows the system response without HAPF

2) After Compensation

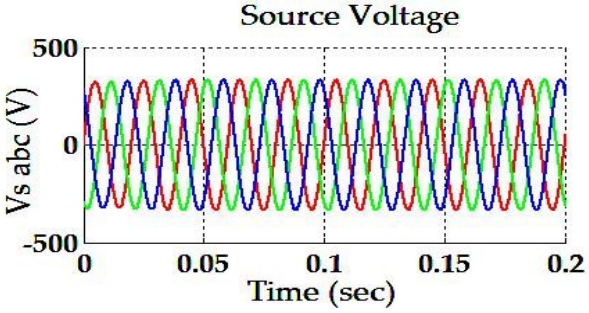


Figure 5. (a)

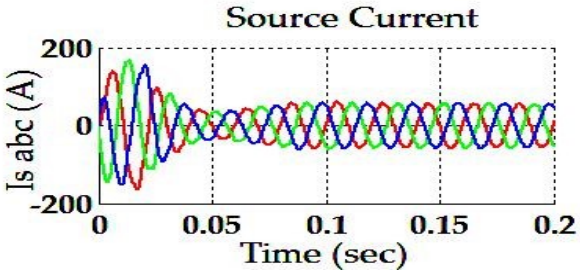


Figure 5. (b)

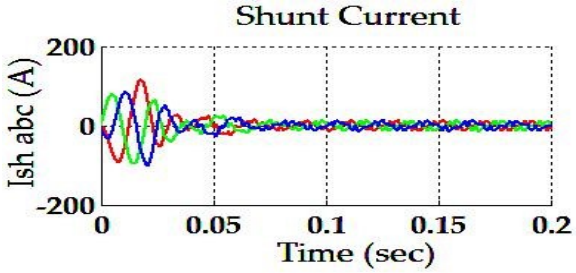


Figure 5. (c)

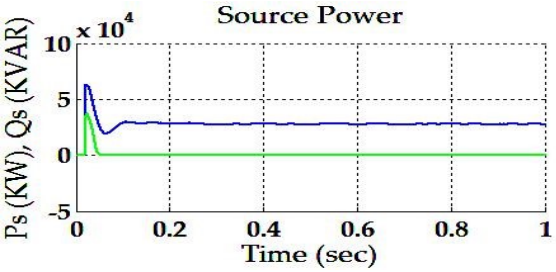


Figure 5. (d)

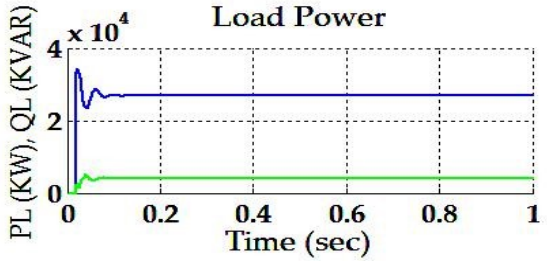


Figure 5. (e)

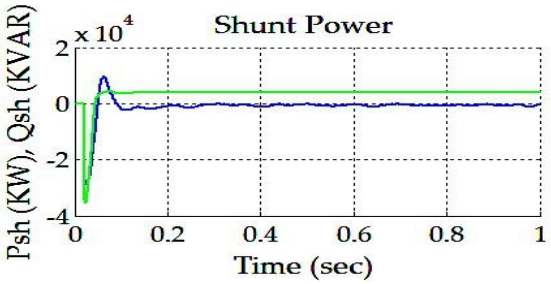


Figure 5. (f)

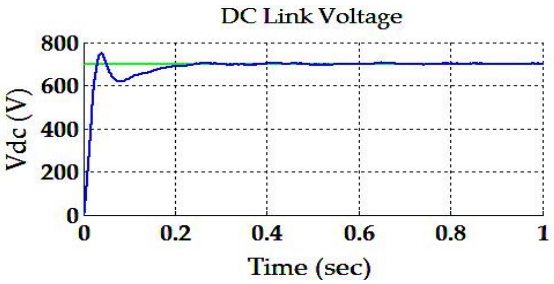


Figure 5. (g)

Figure 5. (a) to (g) shows the performance of HAPF.

B. Load Change Condition

1) Before Compensationg

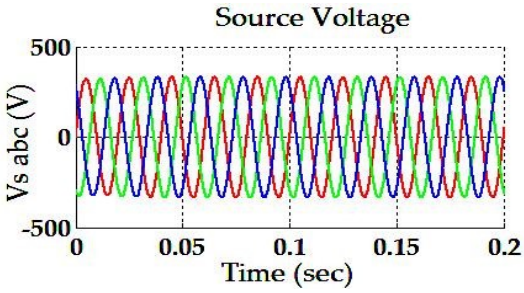


Figure 6. (a)

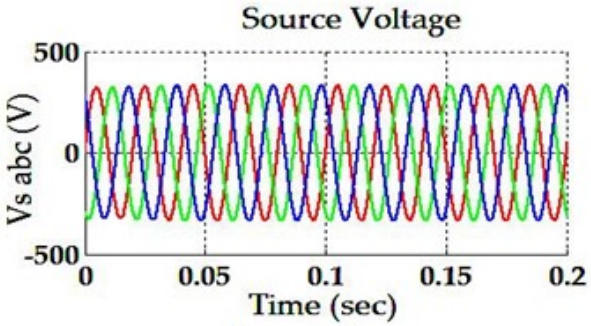


Figure 6. (a)

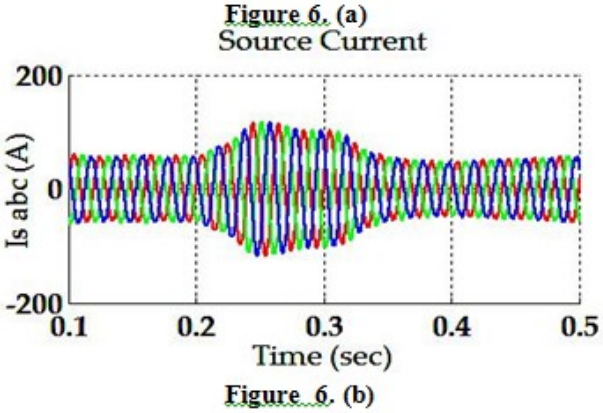


Figure 6. (b)

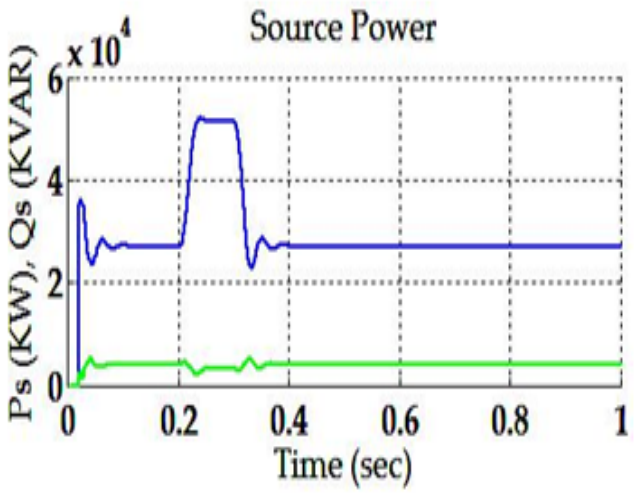


Figure 6. (c)

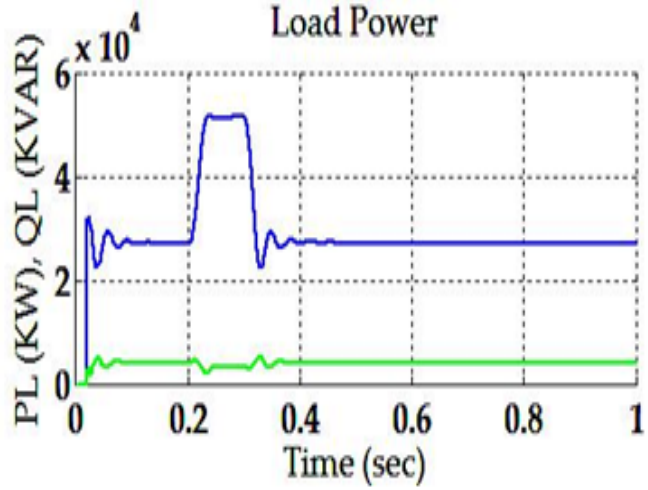


Figure 6. (d)

Figure 6.(a) to (d) shows the system response without HAPF. At 0.2 sec. second load is connected with the first load.

At 0.3 sec, second load is disconnected. The above figure shows the simulation response during the load variation.

2) After Compensation

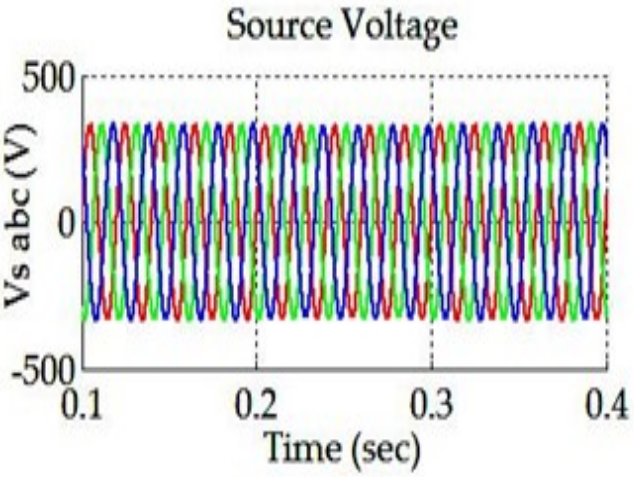


Figure 7. (a)

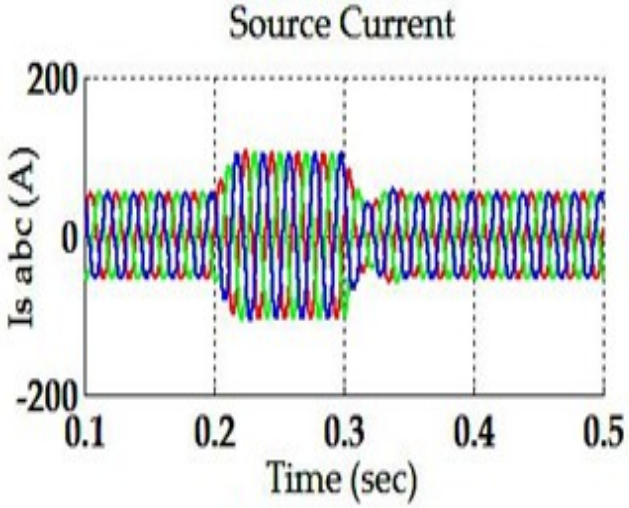


Figure 7. (b)

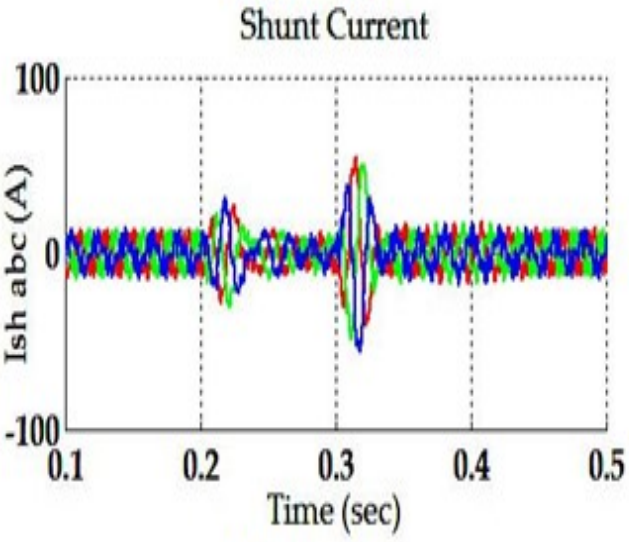


Figure 7. (c)

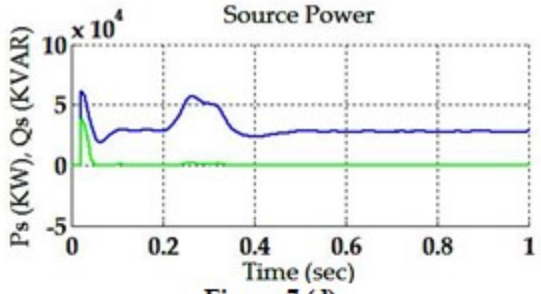
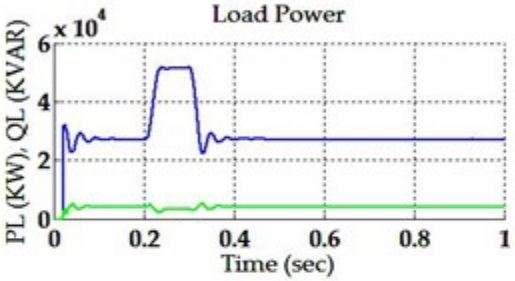


Figure 7.(d)



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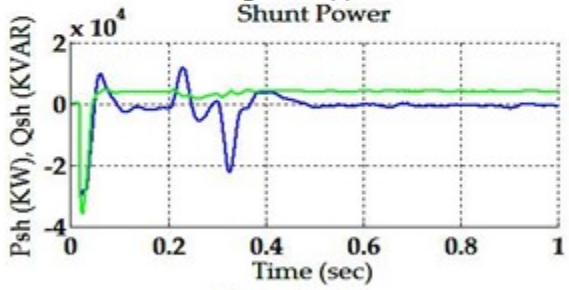

Figure 7. (f)

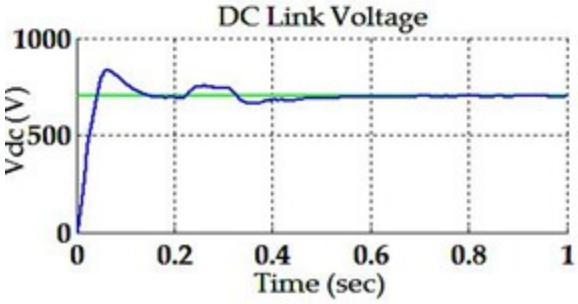

Figure 7. (g)

Figure 7. (a) to (g) shows the performance of HAPF.

Table 1. Load Specification

Nominal Line-to-Line rms Voltage	415 V
Line Frequency	50 Hz
Diode Rectifier Rating	30 KW
Rs	0.1 Ω
Ls	0.1 mH
DC Link Capacitor	3000 μF
Filter Capacitor	3000 μF
Filter Inductor	15 mH
DC Link Voltage	700 V
AC Line inductor	10 mH

Table 2. Dc Link Voltage Regulation

	Before Compensation		After Compensation			
	P_S (KW)	P_L (KW)	P_S (KW)	P_L (KW)	P_{sh} (KW)	V_{dc} (KW)
NoLoad variation	27.1	27.1	27.6	27.1	-0.5	701
Load variation	27.09	27.09	27.91	27.1	-0.81	699

Table 3. Reactive Power Compensation

	Before Compensation		After Compensation		
	Q_S (KVAR)	Q_L (KVAR)	Q_S (KVAR)	Q_L (KVAR)	Q_{sh} (KVAR)
No Load variation	3.99	3.99	0.039	4.03	3.99
Load variation	3.99	9.99	0.055	4.03	3.97

Table 4. Power Quality Improvement

	Before Compensation				After Compensation			
	Q_s (KVAR)	I_s (A)	DPF_s	$^I sTHD$ (%)	Q_s (KVAR)	I_s (A)	DPF_s	$^I sTHD$ (%)
No Load Variation	3.99	54.2	0.8	9.02	0.039	56	1	3.08
Load variation	3.99	54.2	0.8	9.02	-0.81	55	1	3.78

The simulation responses for Rectifier RL load for both operating conditions are obtained. In no load and load change condition, the THD is compensated from 9.02% to 3.08% and 3.38% respectively by using instantaneous power technique which is represented in Table 3. Hence after compensation, in both the case the supply current THD is reduced to less than 5%, the harmonic limit imposed by the IEEE-519 & IEC-6000-3 standard. The main objective of the shunt hybrid active power filter is unity source power factor. It is achieved in both operating conditions which are shown in Table 3. And also Reactive power is compensated for both operating conditions with hybrid active power filter.

SIMULATION OUTPUT

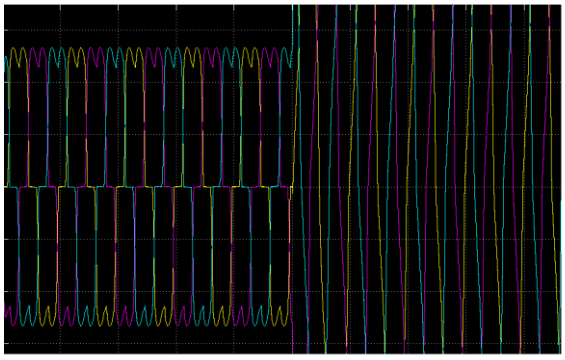

Figure 8

HARDWARE

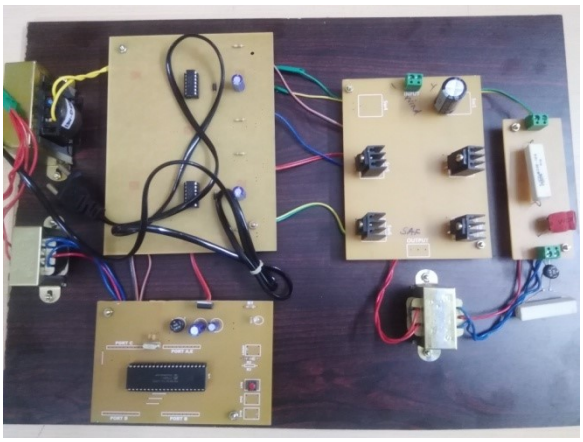

Figure 9

V. CONCLUSION

This paper work presents design of transformer less hybrid active power filter (HAPF) for a distribution system. The above results show the comparative simulation results for both operating conditions. The hybrid filter reduces the harmonics as compare to open loop response. This hybrid filter is tested and verified using MATLAB simulation. A PI controller is implemented for three phase shunt hybrid power filter. The PI controller extracts the reference current from the distorted line current and hence improves the power quality parameters such as harmonic current and reactive power due to nonlinear load. Here the two operating conditions i.e. before and after compensation and the load change condition is analyzed. The harmonic current control and DC capacitor voltage can be regulated under these two conditions.

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Microcontroller Based Over/Under Frequency Relay

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ABSTRACT

This paper investigates the frequency fluctuation in power system and protects the power system from its harmful effects. Therefore we design a Microcontroller Based Under/Over Frequency Relay. In this paper we use microcontroller dsPIC30F4011 for protecting the power system from the problem of frequency fluctuation. When frequency goes below or above from desired value then electromagnetic relay trip and isolate our power system from its harmful effect. Electromechanical protective relays operate by either magnetic attraction, or magnetic induction. Frequency Variation also decreases the life of the equipment and directly affects the overall production of the plant.

Keywords: Frequency Relay, Microcontroller, Trip, CMOS Technology ULN2003

I. INTRODUCTION

During severe emergencies which result in insufficient generation to meet load, an automatic load shedding program throughout the affected area can prevent total area collapse. It also helps to achieve fast restoration of all affected loads. This paper describes the factors involved in applying under frequency and over frequency relays to achieve a desired "deficient generation" protection level and a calculating method to achieve optimum relay settings.

When generator operates with under frequency and over frequency mostly its speed matches with resonance frequency which causes high vibration in generator and turbine. So generator do not operates with under frequency. Under overloading condition the generator will slow down to try to accommodate the extra load, this will result in overheating of stator windings, while also under this condition (under frequency) some equipment can be damaged. A load shedding scheme using dedicated frequency sensing relays will trip (disconnect) a set of load from the grid to recover from under freq and stabilize the system avoiding damage to generator and connected equipments.

II.NEED OF MAINTAINING FREQUENCY CONSTANT

Constant frequency is to be maintained for following functions:

1. All ac motors require constant frequency supply to maintain constant speed.
2. For synchronous operation of various units in the power system network, it is necessary to maintain constant frequency.
3. Frequency affects amount of power transmitted through interconnected lines. So it necessary to maintain constant frequency.
4. Electrical clocks will lose or gain time if they are driven by synchronous motor and accuracy of clocks depends on frequency.

III. DESCRIPTION OF BLOCK DIAGRAM

We can give an overview of complete operation with the help of microcontroller dsPIC30F4011, Electromechanical relay, driver ULN2003 etc.

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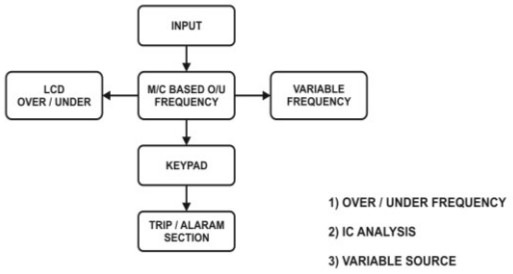
In this block diagram microcontroller(dsPIC30F4011) for control card gets two supply one is the main power supply for their operation and other is the input main ac for variation in frequency. LCD display the operating frequency. Driver is used for driving the relay, LED and buzzer. When frequencies goes less or above from our desired value then relay trips in respond to which LED



start glowing and buzzer start producing noise to aware operators.

Fig: 1. Block Diagram of Over/Under Frequency Relay

IV. POWER SUPPLY

The power supply circuit consists of a bridge rectifier with shunt capacitance filter. A 5 volts regulated source is used for the entire circuit. Three terminal voltage regulators IC 7805 is used to provide 5 volts supply.

A.NEED OF POWER SUPPLY

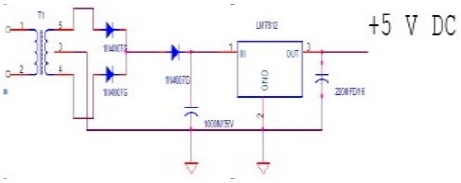
Perhaps all of you are aware that a 'power supply' is a primary requirement for the 'Test Bench' of a home experimenter's mini lab. A battery eliminator can eliminate or replace the batteries of solid-state electronic equipment and the equipment thus can be operated by 230v A.C. mains instead of the batteries or dry cells. Nowadays, the use of commercial battery eliminator or power supply unit has become increasingly popular as power source for household appliances like transreceivers, record player, cassette players, digital clock etc.

A.USE OF DIODES IN RECTIFIERS

Electric energy is available in homes and industries in India, in the form of alternating voltage. The supply has a voltage of 220V (rms) at a frequency of 50 Hz. In the USA, it is 110V at 60 Hz. For the operation of most of the devices in electronic equipment, a dc voltage is needed. For instance, a transistor radio requires a dc supply for its operation. Usually, this supply is provided by dry cells. But sometime we use a battery eliminator in place of dry cells. The battery eliminator converts the ac voltage into dc voltage and thus eliminates the need for dry cells. Nowadays, almost all-electronic equipment includes a circuit that converts ac voltage of mains supply into dc voltage. This part of the equipment is called Power Supply. In general, at the input of the power supply, there is a power transformer. It is followed by a diode circuit called Rectifier. The output of the rectifier goes to a smoothing filter, and then to a voltage regulator circuit. The rectifier circuit is the heart of a power supply.

C. FILTRATION

The rectifier circuits we have discussed above deliver an output voltage that always has the same polarity: but however, this output is not suitable as DC power supply for solid-state circuits. This is due to the pulsation or ripples of the output voltage. This should be removed out before the output voltage can be supplied to any circuit. This smoothing is done by incorporating filter networks. The filter network consists of inductors and capacitors. The inductors or choke coils are generally connected in series with the rectifier output and the load. The inductors oppose any change in the magnitude of a current flowing through them by storing up energy in a magnetic field. An inductor offers very low resistance for DC whereas; it offers very high resistance to AC. Thus, a series connected choke coil in a rectifier circuit helps to reduce the pulsations or ripples to a great extent in the output voltage. The fitter capacitors are usually connected in parallel with the rectifier output and the load. As AC can pass through a capacitor but DC cannot, the ripples are thus limited and the output becomes smoothed. When the voltage across its plates tends to rise, it stores up energy back into voltage and current. Thus, the fluctuations in the output voltage are reduced considerable. Filter network circuits may be of two types in general: Choke Input Filter, Capacitor Input Filter.



V. CIRCUIT DIAGRAM

We can see the complete operation of this paper with the help of this circuit diagram.

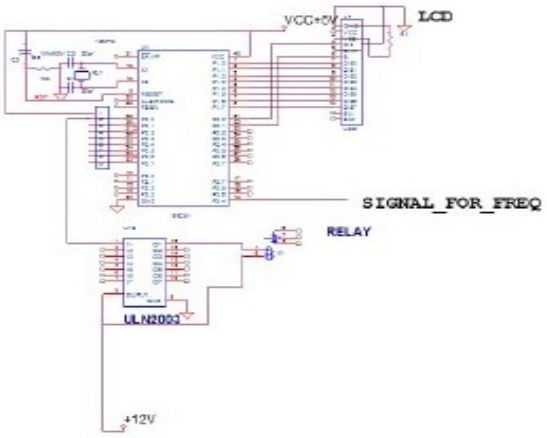


Fig: 2. Circuit Diagram of Over/Under Frequency Relay

Fig: 3. Picture of Over/Under Frequency Relay

VI. DECRIPTION OF MICROCONTROLLER dsPIC30F4011

Microcontroller dsPIC30F4011 which are used for controlling the frequency deviation. The dsPIC30F4011 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the indus-try-standard 80C51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel dsPIC30F4011 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications. The dsPIC30F4011 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the dsPIC30F4011 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM con-tents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

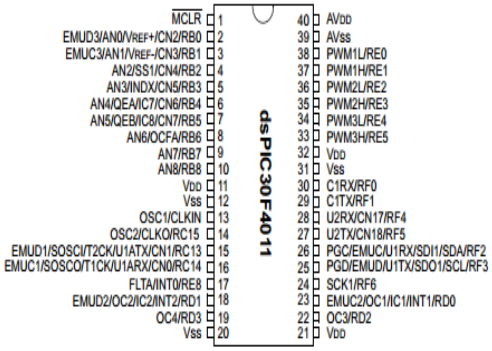


Fig: 4. Pin details of Microcontroller dsPIC30F4011

VII. RELAY

A relay is an electrical switch that opens and closes under the control of another electrical circuit In the original form, the switch is operated by an electromagnet to open or close one or many sets of contacts. Because a relay is able to control an output circuit of higher power than the input circuit, it can be considered, in a broad sense, to be a form of an electrical amplifier. When a current flows through the coil, the resulting magnetic field attracts an armature that is mechanically linked to a

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moving contact. The movement either makes or breaks a connection with a fixed contact. . When the current to the coil is switched off, the armature is returned by a force approximately half as strong as the magnetic force to its relaxed position. Most relays are manufactured to operate quickly. In a low voltage application, this is to reduce noise. In a high voltage or high current application, this is to reduce arcing.

VIII. POLE AND THROW

SPST – Single Pole Single Throw These have two terminals which can be switched on/off. In total, four terminals when the coil is also included SPDT - Single Pole Double Throw. These have one row of three terminals. One terminal (common) switches between the other two poles. It is the same as a single change-over switch. In total, five terminals when the coil is also included DPST - Double Pole Single Throw These have two pairs of terminals. Equivalent to two SPST switches or relays actuated by a single coil In total, six terminals when the coil is also included. This configuration may also be referred to as DPNO

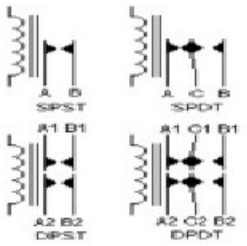

Fig: 5. Circuits symbols of relays

The contacts can be either Normally Open (NO), Normally Closed (NC), or change-over (CO) contacts.

IX. APPLICATION

Frequency relays are used whenever deviations from nominal system frequency need to be detected. Frequency deviations can be harmful to connected objects, such as generators and motors, or when abnormal frequency creates inconvenience for power consumers and may cause failures of electrical apparatuses. Frequency relays are also used where detection of high or low frequency indicates system abnormalities, such as faults in speed regulation units or system overload. Under frequency relays should be considered for applications where the detection of under speed conditions for synchronous motors and condensers is required. On lines where reclosing of the source breaker is utilized, damage to large synchronous motors can be avoided by disconnecting the motors from the system. Likewise, disconnection of synchronous condensers can be initiated upon loss of power supply. The over frequency relay is generally utilized for the protection of ac machines from possible damage due to over speed conditions. These conditions can occur, for example, on machines with no mechanical governor or on those with the machine shaft linked to a prime mover or to another machine, either one of which could accelerate the combination to a hazardous over speed condition (e.g. a hydro generator).

X. RESULTS

The relay is tested under different test conditions. These tests conditions are given below. Case 1 is over-frequency case, while Case 2 is under-frequency case.

Case 1: Over-Frequency

In the first case, the load is shed in two stages. Initially from 190MW to 150MW at 70sec, later on further load shed of 70MW is made at 120sec and the relay behaviour is observed. Fig. 6 represents the relay status under different load conditions.

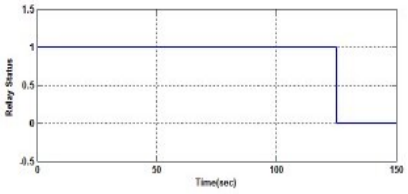

Fig 6. Relay Status

In first stage the relay does not trip. However a huge decrement in load of 70MW results in relay tripping. Fig.

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7 represents the behaviour of electrical frequency.

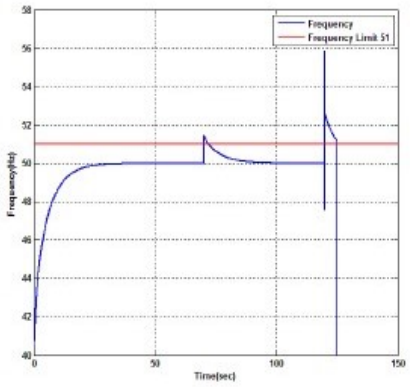

Fig. 7. Output Frequency

Case 2: Under-Frequency

In this case, 40MW is added at 70 sec in addition to base load of 150MW. Later on further load shed of 50MW is done at 120sec. Fig. 8 represents relay status under different load conditions.

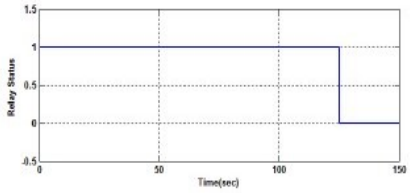

Fig 8. Relay Status

XI. CONCLUSION

At last we would like to conclude this paper under the guidance of highly capable mentor along with group members. Basically it is not just a paper it is the need of our initiative should be taken up to implement this practically in the college environment and the research is continued further by the students with maintenance. Future aspects of this paper is to be mainly used in chemical industries, protection of transformers and generators in power system which might badly affected by frequency variation .Also the life and performance of equipment suffers due to frequency variation.

ACKNOWLEDGEMENT

The authors acknowledge the Management of SCSVMV University, Tamilnadu, India and Head of the Department of Electrical and Electronics Engineer, for the support and keen interest in promoting the research and development in the division by providing the facilities and time.

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Advanced Distribution Automation for a Smart Grid Environment

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ABSTRACT

Everyone is looking to "the Smart Grid" to provide electric utilities with information age technologies that will significantly improve distribution system protection, reliability, operating efficiencies, power quality, safety, and customer satisfaction. These technologies are now readily available in mature and sophisticated products that make it easier than ever for an electric utility to implement elegant protection coordination schemes at the distribution level complete with advanced Distribution Automation (DA). This white paper discusses some of the most useful of these technologies, including pulse reclosing, and describes how they can be used effectively to install an advanced Distribution Automation System based on practical experiences and successful implementations. The benefits of such a system are enormous and will directly improve an electric utility's reliability figures (SAIDI, SAIFI and CAIDI) and reduce momentary operations (MAIFI).

EXECUTIVE SUMMARY

Many proven and effective Distribution Automation (DA) technologies are now available to help an electric utility significantly improve reliability, operating efficiency, power quality, and public and worker safety. These technologies are already built into products that are readily available from established and trusted manufacturers. Many of the products "plug and play" together very nicely under the right infrastructure which is ideal from any utility's viewpoint. The key to unlocking the full benefits in these technologies and products is for a utility to develop a comprehensive DA design plan up-front that meets its specific requirements and its short and long-term objectives.

Since many utilities have already successfully implemented some form of Distribution Automation with excellent results, there is no longer any question of DA's potential overall benefits. However, when evaluating cost-benefits of the various types of DA functionality now available, each utility may find a different set of functions that provide the best overall cost-to-benefit ratio. This is the functionality they should focus on for their DA implementation.
The concept of implementing a Distribution Automation System closely aligns with the U.S. Department of Energy's (DOE) vision to implement Smart Grid across the United States in each of its 3,100+ electric utilities[1] by the year 2030.

Grid 2030 Vision calls for the construction of a 21st century electric system that connects everyone to abundant, affordable, clean, efficient, and reliable electric power anytime, anywhere. We can achieve this through a smart grid, which would integrate advanced functions into the nation's electric grid to enhance reliability, efficiency, and security. It would also contribute to the climate change strategic goal of reducing carbon emissions. These advancements will be achieved by modernizing the electric grid with information-age technologies, such as microprocessors, communications, advanced computing, and information technologies.[2]

The Smart Grid that DOE envisions will actually be built as a series of inter-related projects of which Distribution Automation will only be a part. However, DA will be a critical component in terms of the Smart Grid's ability to provide safe, reliable and secure electric power of high quality to the nation's 131 million[3] electric customers. In fact, the main objective of a Distribution Automation System is to improve electric service reliability by 1) avoiding potential outages, 2) localizing outages quickly when they do occur, 3) shortening restoration time to customers that have outages, and 4) minimizing momentary interruptions and voltage fluctuations.

Once a utility develops a design plan for its overall Distribution Automation System, it can be implemented incrementally rather than all at once. This allows each utility to develop its DA System at a rate that fits its resource capabilities and its financial constraints.

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[1] Estimate from the DOE's "Grid 2030"- A National Vision for Electricity's Second 100 Years, page 3.

[2] See http://www.oe.energy.gov/smartgrid.htm

[3] Same as Footnote 1.

DISTRIBUTION AUTOMATION

Defining Distribution Automation is somewhat like defining Smart Grid because if you ask ten different utilities you will likely get at least ten definitions. For this paper, it's important to start by defining what the distribution system includes and what is being automated when describing Distribution Automation.

The distribution system is the collection of primary radial circuits that a utility uses to deliver power from a substation to the end customers. The substation breaker is the source device for a distribution circuit and it forms the boundary between substation and distribution. The substation itself is not considered part of the distribution system. The circuit feeder is the backbone of a distribution circuit that can carry the circuit many miles from the substation. The feeder often reaches a fork where it

splits and goes in two or more directions. A feeder can have multiple forks as it spreads out from the substation. The feeder "feeds" many smaller lateral branches all along its length that carry power out from the feeder to the customers.

With this basic configuration, a fault anywhere on a circuit would lockout the station breaker and all of its customers would experience an outage until the fault was located and repaired. Sixty years ago when circuits were small and had few customers, a couple of well place fuses on the distribution circuit would have improved reliability enough to be acceptable. However, this would not be acceptable today, and distribution circuits now have very complex protection schemes utilizing sophisticated protection devices that attempt to minimize the number of customers affected by a circuit fault.

The most common protection devices used on distribution circuits today are fuses, sectionalizers and reclosers [4]. All three of these devices will automatically operate for a fault according to programmed settings or fuse size and type. Reclosers and sectionalizers are used on the main feeder of a circuit and fuses are generally only used on lateral branches. Reclosers are designed to operate like a station breaker. They interrupt fault current and reclose a preset number of times before going to lockout. Sectionalizers count breaker and recloser operations during a fault sequence and lockout [5] when they reach their preset shots-to-lockout count while the breaker or
recloser is still open. Sectionalizers can interrupt normal load current but not fault current. Fuses blow when they see fault current above their rating according to a specific time-current curve (TCC). It is fairly easy to set these devices up on each circuit so they coordinate correctly with each other and provide the desired protection over a wide range of fault conditions. This is very important and is the reason these devices are widely used.

Sectionalizers and reclosers can be remotely monitored and controlled, but they still always operate for a fault using their own local programming and control logic. Fault protection requires much faster analysis and decision making than existing remote monitoring and control technologies can provide from a remote location.

[4] Because sectionalizers and reclosers operate automatically for a fault according to their programmed settings, they are sometimes referred to as "Automatic Sectionalizers" and "Automatic Reclosers".
[5] Sectionalizers cannot interrupt fault current and they do not reclose. They open and lockout once when their programmed shots-to-lockout count is reached while the circuit is deenergized, i.e., the breaker or an upstream recloser is open.

A typical distribution circuit of the type being described would have the configuration shown in Figure 1. This circuit has a station breaker, 7 normally closed sectionalizers, and 2 normally closed reclosers for its protection. No fuses are shown because they are not used on the feeder. The circuit also has 5 normally open tie sectionalizers to other distribution circuits that are used as alternate feeds when needed.

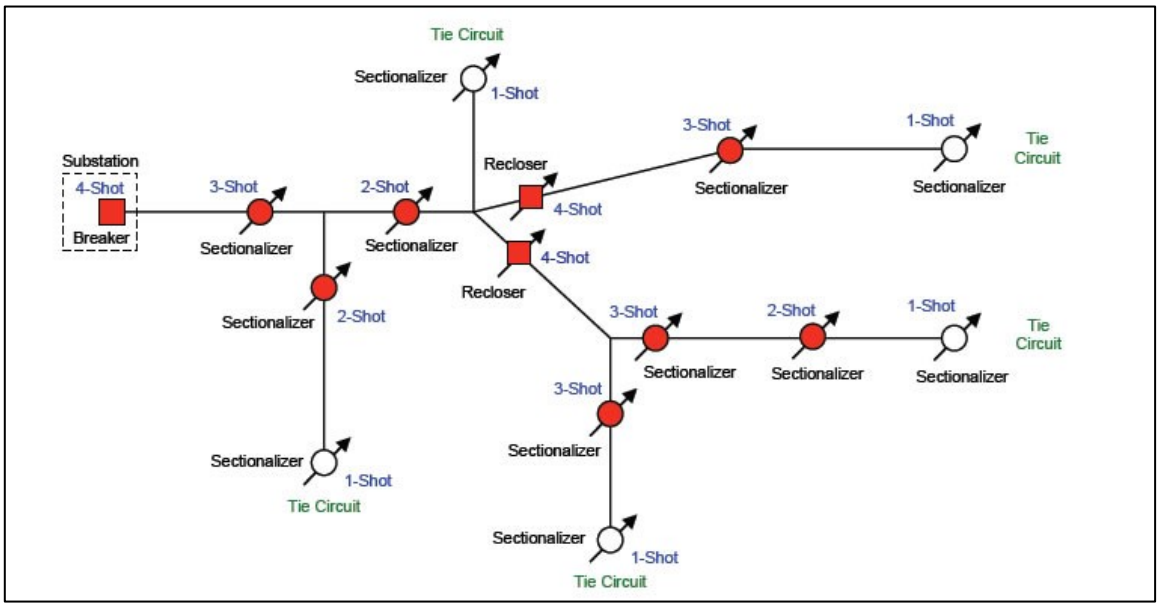

Figure 1. Protection Configuration for a Typical Large Radial Distribution Circuit

The protection devices on this circuit are set so that, for a fault in any load block, the closest upstream device locks out. See the example in Figure 2 below.

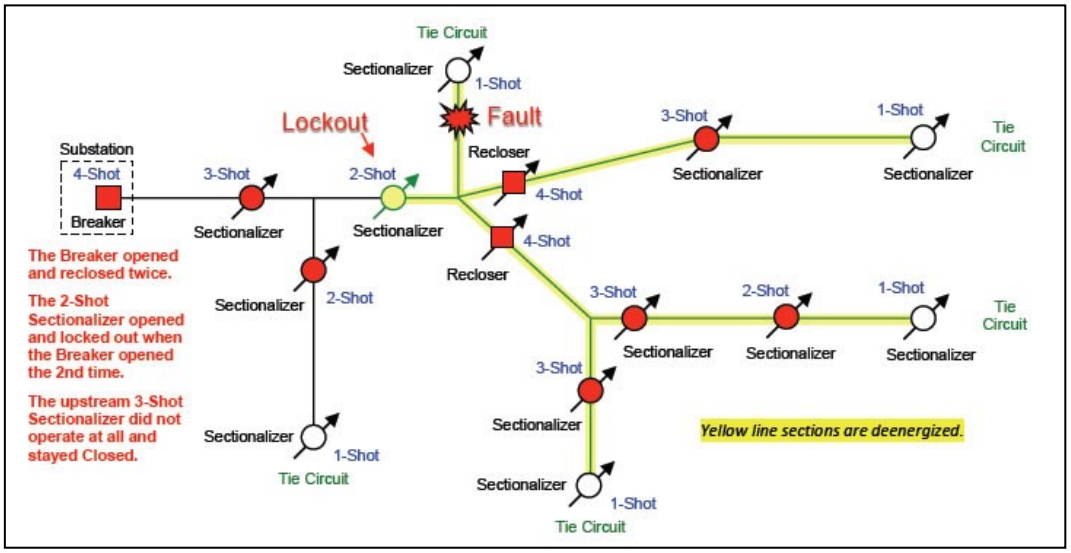

Figure 2. Circuit with 2-Shot Sectionalizer Locked Out for Downstream Fault

The 2-Shot sectionalizer in Figure 2 has correctly locked out for a fault in the adjacent downstream load block[6]. With the fault removed from the circuit, the upstream station breaker and 3-Shot sectionalizer stay closed and all customers in the 3 upstream load blocks retain power. However, all load blocks downstream of the 2-Shot sectionalizer have now lost power since this is a radial circuit with only one upstream source, the substation breaker. Approximately 70% of the customers are experiencing an outage for a fault in a load block that only has 10% of the customers.

This outcome could be significantly improved if the substation breaker and all sectionalizers and reclosers on the distribution system were remotely monitored and controllable through a Distribution SCADA System and either 1) distribution operators were given special tools needed to quickly analyze outage and fault conditions and safely reroute power around problems using remote control, or 2) have an application that performs automatic restoration for the distribution operator. Figure 3 shows the results of such a system.

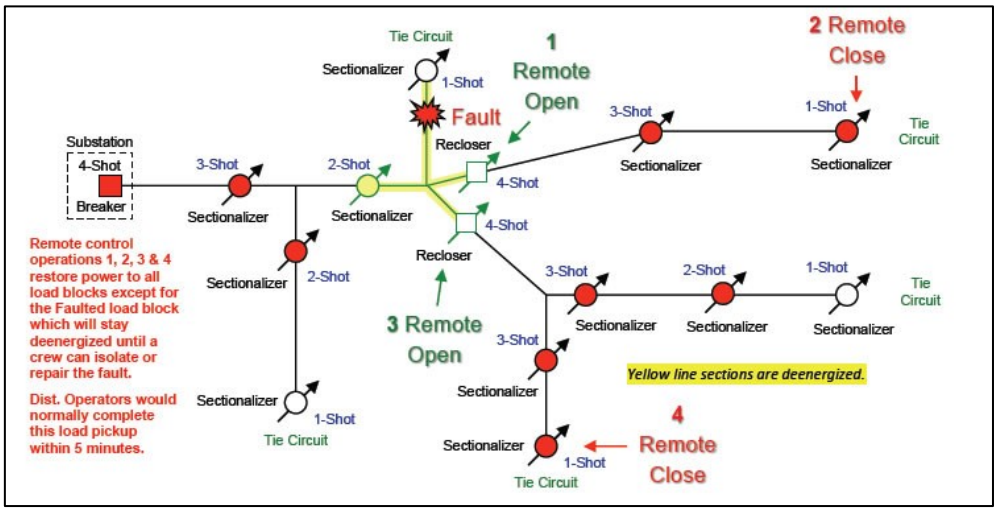

Figure 3. Circuit Restoration through two N.O. Tie Sectionalizers after Fault Isolation

Figure 3 now shows 90% of the circuit restored with only the load block containing the actual fault still out of power. A repair crew would be quickly dispatched to this load block to locate and repair the actual fault.

Collectively, Figures 1, 2 & 3 show the essence of what Distribution Automation is, and it doesn't matter whether distribution operators do the remote switching using SCADA remote controls or an Auto-Restoration Application[7] does it automatically.

[6] Each line section between protection devices is called a load block. Utilities usually have a design standard they follow for the number of customers or KVA assigned to each load block.

[7] Experience has shown that distribution operators can do a better job than Auto-Restoration Applications because of the complexity of most distribution systems. However, new approaches to automation that are limited to small groups or teams of devices are proving to be very effective. With small group automation, a distribution operator still oversees the big picture.

The sectionalizer/recloser circuit configuration described above has proven itself to be both effective and reliable since the late 1960's, but it does have shortcomings. In order for a sectionalizer to open and lockout to isolate a fault beyond, an upstream device[8] has to trip and reclose multiple times. This causes unwanted momentary outages for customers upstream of the fault. It also requires multiple reclosings of an upstream device under fault conditions to enable a downstream sectionalizer to reach full count. This stresses the distribution system and can cause additional circuit damage. Attempts to use all-recloser configurations in the past to avoid these problems have resulted in a lot of mis-coordination because reclosers have not had the time-current curve accuracy needed to reliably open and lockout the correct device[9]. Therefore, the sectionalizer has had a dominant role in distribution automation systems since the 1970's because there hasn't been anything better.

THE PULSE RECLOSER

Today, a totally new type of device is available that significantly improves the whole distribution protection/automation landscape. This new device is the Pulse-Recloser and it is designed to eliminate the weaknesses that sectionalizers and reclosers have had. It also brings a whole new set of advanced features to the distribution system that truly embodies the Smart Grid vision.

The Pulse-Recloser represents a totally new class of distribution device. It is more like a 3-Phase recloser than a sectionalizer because it can interrupt fault current It provideseasily selectable TCC curves of every type a utility could want which enables it to coordinate extremely well with all the standard protection devices on a distribution circuit from the substation breaker down to single-phase fuses without coordination problems. In addition, Pulse-Reclosers can be installed on a circuit as close together as needed to meet load block (*connected-KVA*) design guidelines and the correct one will lockout for a fault. To enable all this amazing functionality, a Pulse-Recloser provides a number of sophisticated features.

1. Its TCC curves are extremely accurate, i.e., much more accurate than anything previously available for use on a distribution feeder. This makes device coordination much easier and a lot more flexible.

2. It has a Pulse-Close / Pulse-Reclose feature that pulses and tests the line one phase at a time so it does not hard-close directly into a solid fault. *(This is why it is called a Pulse-Recloser.)*
3. It takes both its preferred and its alternate AC Power directly from the primary lines so no secondary power sources are needed.
4. It synchronizes time[10] and location through a built-in GPS Radio.
5. It is a totally self-contained unit/package that mounts near the top of a pole *(i.e., it has no control box, no control cables and no power cables to deal with.)*
6. It can be configured to operate in single phase mode where applicable to only open faulted phases keeping unfaulted phases energized.
7. It has a fuse-saving feature that enables one fast trip and reclose to save a downstream fuse from blowing for a momentary fault such as a lightning arrestor flashover or a tree branch brushing past a conductor in a wind storm. *(This could save hours of outage time to customers in a storm when no one may be available to replace a blown fuse for hours because of other more critical problems.)*
8. It provides a feature called Pulse-Finding[11] for improved coordination at the ends of a circuit where minimum trip settings are constrained by load and fuse sizes or on circuits that have a standard recloser downstream with less accurate timecurrent curves.
9. It maintains a very accurate and detailed sequence of events log that can be easily downloaded remotely to analyze circuit operations. *(The detail and accuracy of these logs easily rivals anything available from a substation.)*
10. It also provides very accurate waveform captures that can be easily downloaded remotely to analyze circuit operations. *(Again, the detail and accuracy of the waveform captures easily rival anything available from a substation.)*

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[8] Since a sectionalizer cannot interrupt fault current, an upstream breaker or recloser has to operate.

[9] Protection devices on a distribution circuit are generally spaced too close together for all-recloser deployments to accurately open the correct device for a fault. A 2 to 1 mix of sectionalizers to reclosers generally works best as shown in figures 1 through 3.

[10] It's wonderful to analyze a fault across multiple distribution devices and have the time be exactly the same in all of them.

[11] Pulse-Finding allows Pulse-Reclosers near the end of the circuit to use the same TCC Curves. They will all trip simultaneously for a fault beyond and the most upstream device will reclose first because it has AC source voltage. If it recloses successfully, it momentarily raises its minimum trip setting. Now the next downstream device has source voltage and it recloses. If it closes successfully without seeing the fault return, it momentarily raises its minimum trip setting. If the fault returns at any point in the sequence, then that Pulse-Recloser opens and locks out and the upstream devices stay closed.

Pulse-Reclosers are deployed on a circuit the same way sectionalizers and reclosers are used. Figure 4 below shows all Pulse-Reclosers installed on the same circuit we examined in Figures 1, 2 and 3 above.

Note that most of the devices are now set for 2 Shots-to-Lockout which provides 1 Pulse-Reclose after an initial trip on fault.

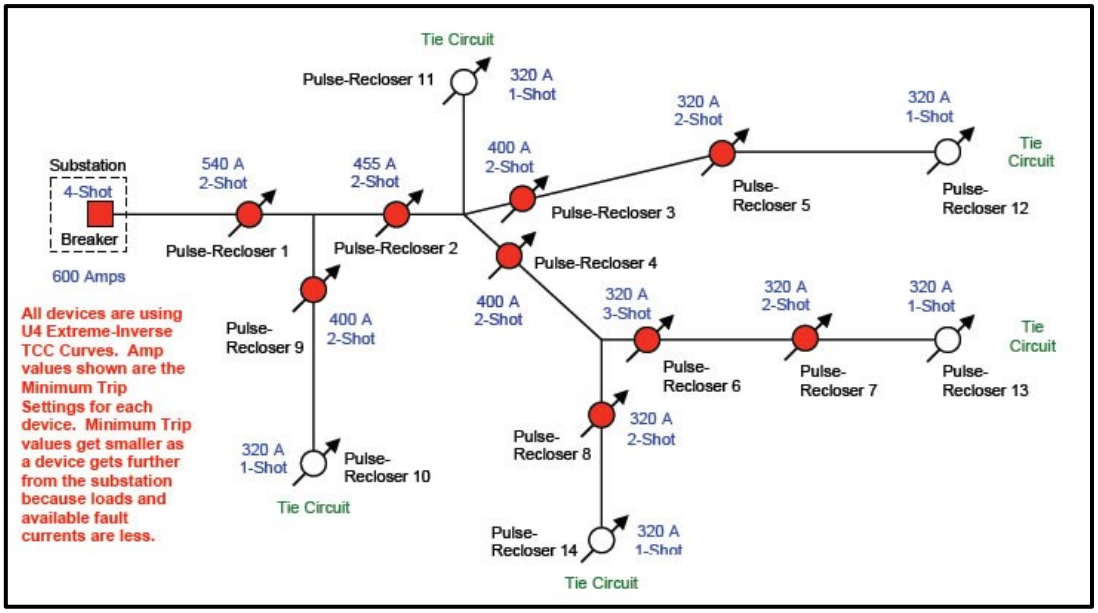

Figure 4. Protection on a Radial Distribution Circuit using all Pulse-Reclosers

Pulse-Recloser coordination relies mainly on TCC Curves and minimum trip settings and not on Shots-to-Lockout settings to clear a downstream fault. Figure 5 below shows how the Pulse-Reclosers operate for the same fault analyzed in Figure 2 above.

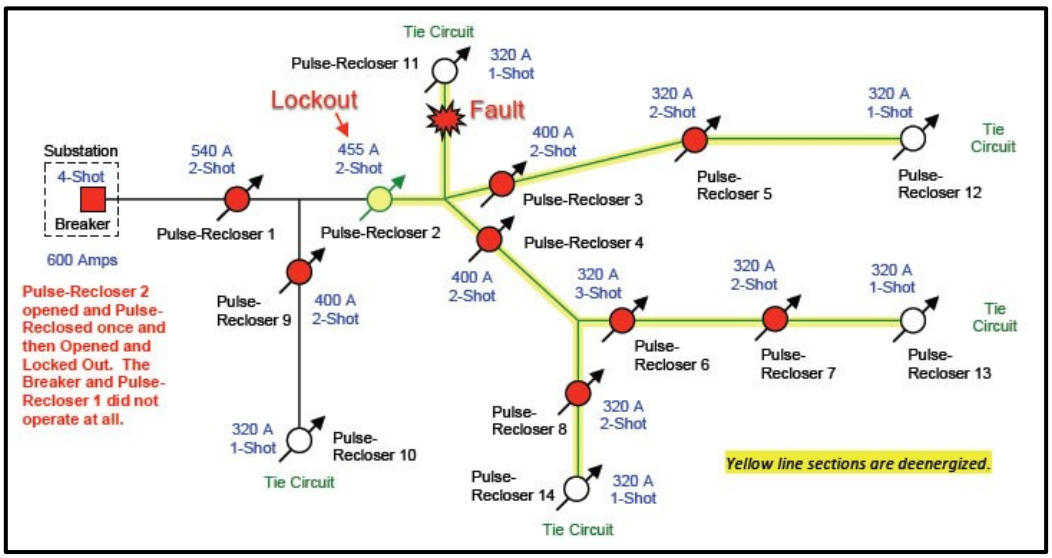

Figure 5. Circuit with Pulse-Recloser 2 Locked Out for a Fault just Downstream

With all Pulse-Reclosers installed on our sample distribution circuit, the fault sequence for a fault just downstream of Pulse-Recloser 2 is quite different than what we saw for the Sectionalizer/Recloser

configuration shown in Figure 2. Only Pulse-Recloser 2 operates for the fault now and the breaker does not operate at all. What are the benefits?

1. Upstream customers between the substation and Pulse-Recloser 2 (PR 2) do not see any momentary outages because the breaker does not operate.
2. PR2 trips faster for a fault than the breaker since it uses a faster TCC curve, so less energy is delivered to the fault putting less stress and potential damage on the circuit. (See See Figure 7 which shows the TCC Curves for each of the devices.)
3. Only one reclose is needed to verify that the fault is not temporary because shotsto- lockout is not used for coordination as with sectionalizers.
4. The reclose performed by PR 2 is a Pulse-Reclose which tests each phase for fault before actually closing. If the fault is still present during the Pulse-Test, then the device locks out without actually reclosing into the fault. Pulse-Reclose Testing is quite effective in detecting both phase and ground faults with only a small current pulse injected into the downstream line. In this example, PR 2 was only configured to perform 1 Pulse-Reclose, but up to 4 recloses can be configured. Each reclose can be individually configured for either a Pulse or a Hard[12] reclose.

[12] Downstream sectionalizers cannot reliably see and count a Pulse-Reclose so sometimes one Hard-Reclose is needed to allow a 2-Shot downstream sectionalizer to coordinate with a Pulse-Recloser.

Figure 6 below shows 90% of the circuit restored with only the load block containing the actual fault still out of power. This load pickup would normally be completed via remote controls issued by Distribution Operators in less than 5 minutes[13] from the start of the fault. The Operators would first verify the location of the fault by checking to see that PR 1 and PR 2 both had fault indicators active. They would then check to verify that downstream devices PR 3 and PR 4 did not have active fault indicators. This would confirm that the fault was in the load block just downstream of PR 2. They would then isolate the fault by opening downstream devices PR 3 and PR 4 via remote control. Next the Operators would determine if adjacent circuits could pick up the deenergized load blocks by checking those circuits to see what their available capacity was. Generally, circuits are designed to allow load pickup through N.O. Tie devices when they are originally built. In this example, there was adequate capacity and the Operators closed PR 12 and PR 14.

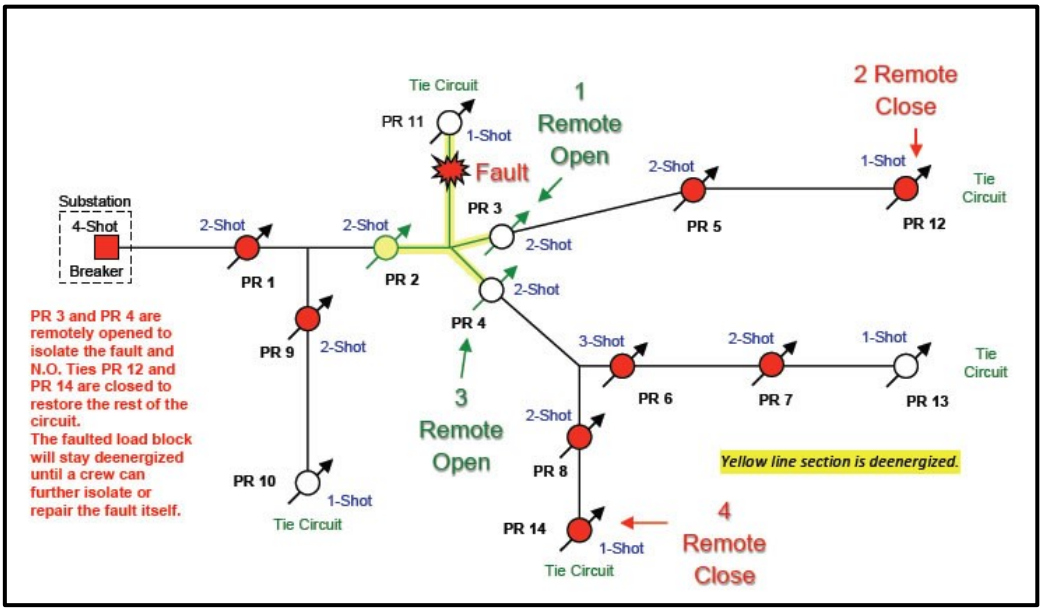

Figure 6. Circuit Restoration through N.O. Ties, PR 12 and PR 14, after Fault Isolation.

Later when a distribution operator is ready to remotely close Pulse-Recloser 2, believing the fault has been cleared, a Pulse-Close will be issued which again tests each phase first to verify that no other faults are still present before actually closing. If a fault is still present, the Pulse-Recloser will report which phase(s) appear faulted, what the estimated fault magnitude is and it will lockout without closing. Operators always have the option to send a hard close to the device which might help crews spot the fault
location.

Figure 7 shows the TCC curves used by the Pulse-Reclosers in the example circuit.

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[13] The target for First Pickup of customers downstream of the actual fault through Normally Open Tie devices is generally 5 Minutes because any outages 5 minutes or less are considered momentary operations and not outages. However, with modern SCADA tools, Distribution Operators routinely analyze and isolate a fault and then pickup downstream customers within two minutes.

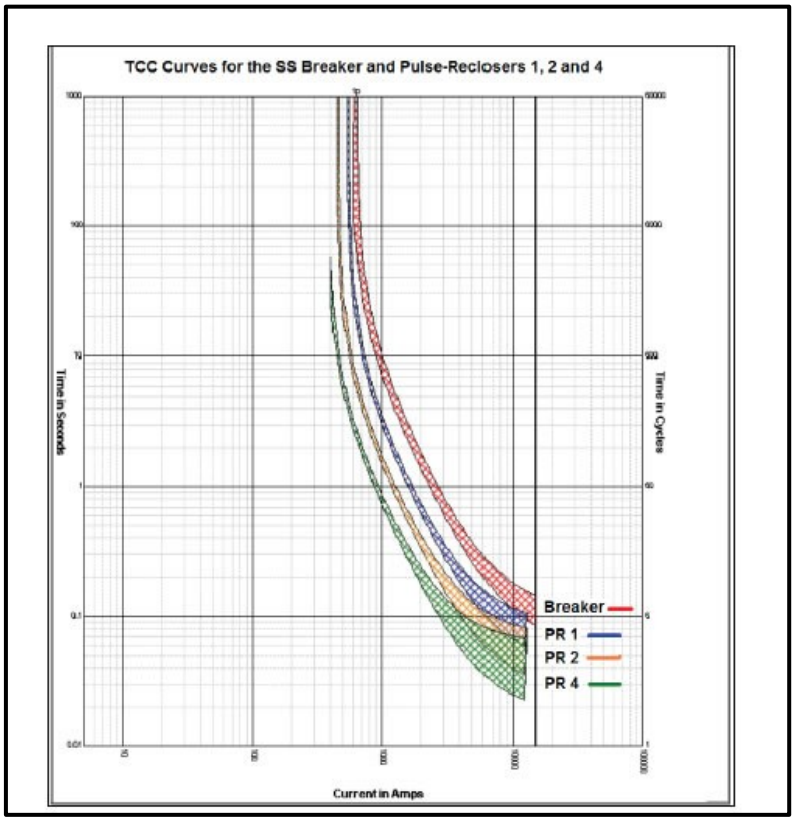

Figure 7a. U4 Extreme Inverse Curves for the Breaker, PR 1, PR 2 & PR 4.

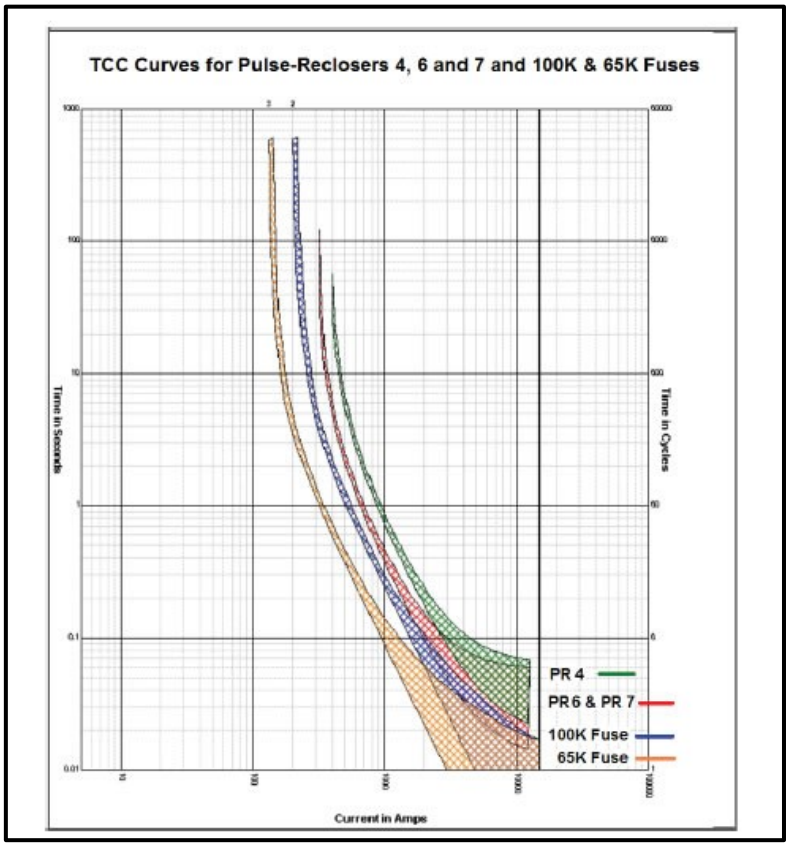

Figure 7b. U4 Extreme Inverse Curves for PR 4, PR 6 & PR 7, a 100K Fuse & a 65K Fuse.

In Figure 7, there are portions of the curves that overlap. This is not a problem because the overlaps occur at higher current levels that are above available fault currents at the point on the circuit where they would apply.

In the preceding Pulse-Recloser example, PR 6 and PR 7 both use the same TCC Curve. This means that if a fault occurs just beyond PR 7, both PR 6 and PR 7 will trip at the same time. This was done to insure that 100K fuses downstream of PR 7 will operate (blow) for a fault beyond before PR 7 trips. Pulse-Reclosers have a lower curve limit that is defined by the type fuses used beyond. This is only a concern near the end of a feeder. Since PR 6 and PR 7 do use the same TCC Curve, PR 6 is configured for 3
Shots-to-Lockout and PR 7 is configured for 2 Shots-to-Lockout. When PR 7 locks out for a fault beyond on 2-Shots, PR 6 will have one additional reclose remaining. It will close and stay closed because PR 7 is open and locked out.

This is somewhat similar to the sectionalizer coordination scheme described earlier. The difference is that the Pulse-Reclosers are still tripping on fault overcurrent and not waiting for an upstream device

to operate. Also, since Pulse-Recloses are used rather than Hard-Recloses, the circuit is not being stressed with full fault current on each Pulse- Reclose.

The Pulse-Recloser also provides a Pulse-Finding Mode which allows devices to use the same initial TCC Curve and the same Shot-to-Lockout setting and still coordinate correctly.

Additional Pulse-Recloser Notes:

- When Pulse-Reclosers are used on a circuit, station breaker ground trip settings may need to be tuned. Because a Pulse-Recloser closes one phase at a time after each successful phase pulse test, there is a very short period of time when just one phase is closed and then two phases closed. If ground fault settings are set too low at the breaker, it could start timing on ground fault overcurrent. This would not cause the station breaker to trip because Pulse-Closing is so fast, but if a delayed fault returns just after the Pulse-Recloser fully closes, the station breaker might already be timing on ground overcurrent and trip before the Pulse-Recloser. Tree faults sometimes come back slow enough to cause this problem. If this occurs, setting breaker ground trip levels slightly higher will correct the problem.
- When pulse-reclosing after tripping on a fault, a Pulse-Recloser always tests the phase that had the highest fault current first, then the phase that had the second highest fault current, etc.
- Pulse-Recloser settings can be easily installed, changed, verified, copied, saved or reapplied remotely. A snapshot downloaded from an installed device can be used to build a setting sheet or run in a simulator program to test and verify settings.
- On circuits that use both Pulse-Reclosers and Sectionalizers, the Pulse-Reclosers might need to have at least one Hard-Reclose configured in order for downstream sectionalizers to count correctly. Sectionalizers generally can't see or count an upstream Pulse-Reclose.

COMMUNICATIONS FOR DISTRIBUTION AUTOMATION

The biggest obstacle to implementing Distribution Automation over the last 30 years has been the lack of good communication options. A utility's distribution assets are spread-out across its service territory, they move[14] frequently and a lot are in locations that until recently were cost-prohibitive to reach with reliable two-way communications. This lack of good communication alternatives in the past is the major reason why DA is not more widely utilized today.

However, this has now changed significantly and a wide range of cost-effective communication technologies and good products are readily available to use for Distribution Automation. Even older technologies now work much better because of greatly improved equipment. Examples:

Technology	Qualities / Features	Configurations	Owner
UHF Radio *Wide Range of Technologies Available*	Line of Sight Basic Coverage, Repeaters Extend its Reach, Some Support Routable Hopping Networks & Some are Self-Configuring, Speed Varies – Slow to Very Fast	Point-to-Point, Spread Spectrum, Fixed NW-Packet Hopping, Peer-to-Peer Meshed Networks 800 & 900Mhz	Utility or 3rd Party
VHF Radio *30-300Mhz*	Licensed, Spread Spectrum Long Dist., Penetrates Hills and Valleys	Wireless Conduit, Some Limited Address Routing	Utility or 3rd Party
Cellular	Excellent coverage in urban areas and along major highways, Low Implementation Costs	Public Cell Phone Network, Dial-up and Limited Direct Access over Control Channels	Cell Phone Company
CDMA/GSM *(Keeps Improving)*	Good coverage in urban areas, Low Implementation Costs, Low Monthly Operating Costs	Public Wireless Data Network, Supports Routable IP Protocols, *Technology is Changing Fast*	Cell Phone Company
Fiber	High Speed, High Bandwidth, Non-Metallic, Resistant to Fault Surges	Supports Routable IP Protocols	Utility or 3rd Party
Wire-Pair *(Twisted-Pair)*	Standard from the Past, Limited Bandwidth & Speed, Still Works Well with the Right Modems	Point-to-Point, Party-Line Leased Line	Utility or 3rd Party

Most utilities will need to use a mix of the communication technologies listed above to achieve the best performance and cost-benefit ratio from their Distribution Automation System. It is extremely critical for a utility to plan their communication strategy up-front, pick the technologies that will work with each of their DA end-points and establish standards[15] that the entire company adheres to. Then, for example, when a new distribution device is needed on a circuit, the design engineer will automatically include
the required DA communications equipment needed to automate the device according to the standard.

[14] As distribution load grows, circuits are changed and distribution protection devices get moved to new locations. DA communication needs to follow the device.

[15] Make the communication standards practical. For example, poletop devices (sectionalizers and reclosers) that could move due to future circuit load growth should use wireless technology. Then if they are moved, they will continue to communicate in their new location as soon as they are reinstalled without having to redesign the communications network. For a distribution substation where high speed and large throughput are important, it might be best to have the standard require a communications engineer to determine the best technology that can be supported at this location.

DA Functional Components

There are seven major functional components in a Distribution Automation System as envisioned by Smart Grid. Five of these are associated with automating major components of the distribution feeder and include: **1) the Distribution SCADA System, 2) Distribution Breakers, 3) Sectionalizers, Reclosers & Pulse-Reclosers,**

4) Fault Locators, and 5) Capacitor Banks. The remaining two components are associated with the end points on the distribution feeder, 6) Distribution Transformers and 7) the Customer- DA and Outage Management.

1. DISTRIBUTION SCADA

The heart of a Distribution Automation System is its real-time, computer-based Supervisory Control and Data Acquisition (SCADA) System that continuously monitors distribution field equipment and enables remote control. For most companies, this will be a separate system from the one that is used for Transmission, however the Transmission SCADA System may already be collecting a lot of the data that the DA System needs, such as substation breaker information. Likewise, there may be additional data that the Distribution SCADA will be collecting that the Transmission Operators would like to have access to. Rather than bringing duplicate data back from the field, the DA SCADA System should have a real-time, two-way data link[16] with the Transmission SCADA System so the two systems can continuously share information. However, for security and safety reasons, distribution operators should not be able to control transmission points and transmission operators should not be able to control distribution points.

There is a wide range of good SCADA Systems available for use in Distribution Automation today and most of these have their roots in Transmission SCADA, so they are mature and reliable products. One Northeastern utility, that has a fully deployed DA System, now uses a single combined Transmission/Distribution SCADA System[17], which has helped them to reduce maintenance and support costs, improve information access across the traditional Distribution/Transmission boundaries and improve SAIFI and SAIDI reliability. However, recent CIP security standards by NERC now discourage this.

a. Dynamic (Real-Time) Circuit / Feeder One-line Displays

These are full-graphic circuit maps that are viewed on a computer screen[18] and show actual real-time feeder device "open/close" statuses and feeder section flows as continuously reported from the field. Devices and analog values that are in an alarm condition generally flash or have a special predefined color to make them easy to spot. Operators can perform remote controls to field devices directly from these displays. Some SCADA Systems support an underlying distribution network model that shows the live/dead condition of every line section on the circuit.

Circuit one-line displays are the most important and most critical screens in a DA System and should be designed very carefully with a lot of operator input. Don't rely on the SCADA Vendor to design[19] these displays even though they have the technical skill. They just don't have the right operating experience.

b. Real-Time Digital Alarm Point & Detail Displays

These are live, real-time displays that show lower priority detail information for circuits and field equipment. This is data that's not really suitable or needed on the one-line displays and can include both digital and analog information as required. They can have a standardized tabular layout or be made to mimic a device or relay's front panel or its diagnostic screen. Some points on these displays will allow operator input or control, such as group alarm resets.

Displays of this type can be categorized into the following groups:

- General Circuit Alarm Point Displays
- General Device Alarm Point Displays
- Device or Relay Setting Displays
- Communication Performance & Statistic Displays

c. Real-Time Analog and Rating Displays

These are live, spreadsheet-like displays that are viewed on a computer screen and show actual real-time analog values (e.g., Amps, MW, MVAR, Volts, Temp) reported from the field. Usually, analog Amp values are shown along with their corresponding seasonal limit ratings (2 Hour, 24 Hour, etc) and Tie Amps[20] Available. Analog values that are in an alarm state flash and/or have a special predefined color and an accompanying tag to indicate which limit value they have exceeded. Monitored values can be easily compared against all the displayed seasonal limit values. These displays are critical during peak load periods because they help operators to manage circuit overload conditions, prevent lockouts and avoid over stressing distribution equipment.

d. Alarm Displays & Historical Event Logs

Alarm displays are live, sorted, filtered, scrollable lists that show the active alarms in the DA System (similar in appearance to an email in-box) with one alarm per line[21]. The alarm lines are often color-coded by a priority/category scheme to make it easy to distinguish them from one another and to find the high priority alarms quickly. New alarms can generally be configured to come in on the top (newest to oldest) or the bottom (oldest to newest) as desired and new alarm lines usually flash until an operator views and acknowledges them. Some alarm systems can be configured to only allow a point to be shown in the active alarm list once, so a new occurrence automatically deletes or overwrites a previous occurrence. This guarantees that every point in the alarm list always shows its current state in the field. Operators usually try to

keep the number of alarms in the active alarm list to a minimum by deleting alarms that have been corrected or otherwise addressed. This makes it easier to manage the next group of alarms that come in.

It's important that the filter and sort, acknowledge and delete, alarm print function, and the priority/category settings for the Alarm Displays all work the way operators need. The vendor's standard setup may not be best here. Address this early in a project because some of this configuration needs to be done when the database is being set up. Also, make sure that operators can get to their most used alarm display filter settings with predefined one-click points so they don't have to go through a multi-step selectable menu each time.

Historical Event Logs are scrollable, filtered lists that show a chorological sequence of the events captured by the DA System (similar in appearance to the alarm display). The event lines can be color-coded by a priority/category scheme to help distinguish them from one another. Some events are not considered to be alarms, so they may never have been in the alarm list. Events in the Historical Event log cannot be deleted by an operator, so a typical Event Log will contain many thousands of events. Good filtering capabilities in the Historical Event Log are important to make it easy to deal with all these events.

As with the Alarm Display, it's important that the filter & sort, event print function and the priority/category settings for the Event Displays work the way operators need. Again, the vendor's standard setup may not be best.

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[19] This is not suggesting that each utility will need special customized screen functions that the vendor has to build. This is more about logical screen layout, design consistency, making sure the right information is shown in the right place and in the right size, and eliminating data that's not needed.

[20] Tie Amps Available are values calculated by the DA System indicating the reserve capacity in amps that a circuit or tie device can support without exceeding its current seasonal limits. They are used when determining if a tie device can be safely closed to pickup load on an adjacent circuit without causing an overload.

[21] Some systems allot more than one line per alarm to provide extra information to the operator.

[22] Distribution devices that are monitored and controlled through the DA/SCADA System will be referred to as "Automated" throughout the rest of the document.

[23] Or the Auto-restoration Program if it's turned on.

---

2. DISTRIBUTION BREAKER AUTOMATION

Ideally, every distribution breaker should be monitored and controlled[22] by the DA System because the distribution operator[23] has to know what the breaker did during a fault sequence to

accurately determine 1) where the fault is and 2) if the rest of the protection on the circuit worked correctly. During restoration, it's also important to know what the breaker load was just prior to the fault in order to determine how much load needs to be picked up. Because the breaker is the source device for a circuit, it's actually one of the most important devices on a circuit to monitor and control remotely, and it can have a huge effect on customer outage time and overall circuit reliability. The DA System should continuously monitor every distribution breaker for overloads, fault operations and lockouts.

When a breaker operation or lockout occurs, the responsible distribution operator is immediately notified via a SCADA alarm. The distribution operator will then:

- analyze and locate the faulted line section[24 & 25]
- isolate the faulted line section from the rest of the circuit by remotely opening the closest normally closed (N.C.) downstream device
- restore power to downstream line sections by remotely closing a normally open (N.O.) tie device to an adjacent circuit[26]
- dispatch field resources to fix the problem

In most cases, the distribution operator will have the un-faulted line sections of the circuit back in power in less than 5 minutes from the time of the first operation[27] and often before customer outage complaints start coming in. The restored customers only see a momentary interruption in power rather than a sustained outage[28] which improves SAIFI and SAIDI reliability figures for the circuit.
Of course, if there are no downstream automated devices or ties on the circuit, then the distribution operator will have to rely on dispatched field resources to do the fault isolation and restoration switching. However, there is still some benefit because the operator is able to mobilize the field resources more quickly thanks to the initial SCADA alarm for the breaker.

a. Remote Monitoring & Control of Distribution Feeder Breakers

Many utilities already have remote monitoring and supervisory control of distribution breakers through their Transmission SCADA. The T&D Data Link between the Transmission and Distribution SCADA Systems would then provide the DA System with the desired breaker automation.

There are 3 options for automating breakers not already supervised by the Transmission SCADA:

- Add the breaker to an existing Transmission RTU if there is one already installed at the substation and get this data through the T&D Data Link.
- Install a Transmission SCADA RTU in the SS and get the data through the T&D Data Link.
- Install a small DA SCADA RTU at the SS and get the data directly. This option is only available for distribution substations that do not have Transmission (BES) Assets because of new CIP requirements.

---

[24] Finding the faulted line section is generally fairly simple as will be described in section 3c below.

[25] This and the following two steps can be performed automatically by an auto-restoration application, however such software has not yet been very effective, it's difficult to maintain the underlying databases, and operators have demonstrated that they can do the restoration better and faster.

[26] Before actually closing the tie device, the operator would estimate the load in amps that needs to be picked up and then check it against the Tie Amps Available for the tie device as described in 3d.

[27] It can take up to 90 seconds from the initial fault operation for a station breaker to reach lockout.

[28] Many Regulatory Agencies only consider outages over 5 minutes to be sustained outages that are reported in SAIFI and SAIDI reliability figures. This allows a complicated fault sequence followed by DA restoration activities to run to completion before customer outage counting starts.

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b. Automatic Limit Alarming for Overloads

The DA System will continuously monitor breaker load amps and generate an overload alarm for any circuit that goes above its current seasonal limit setting.

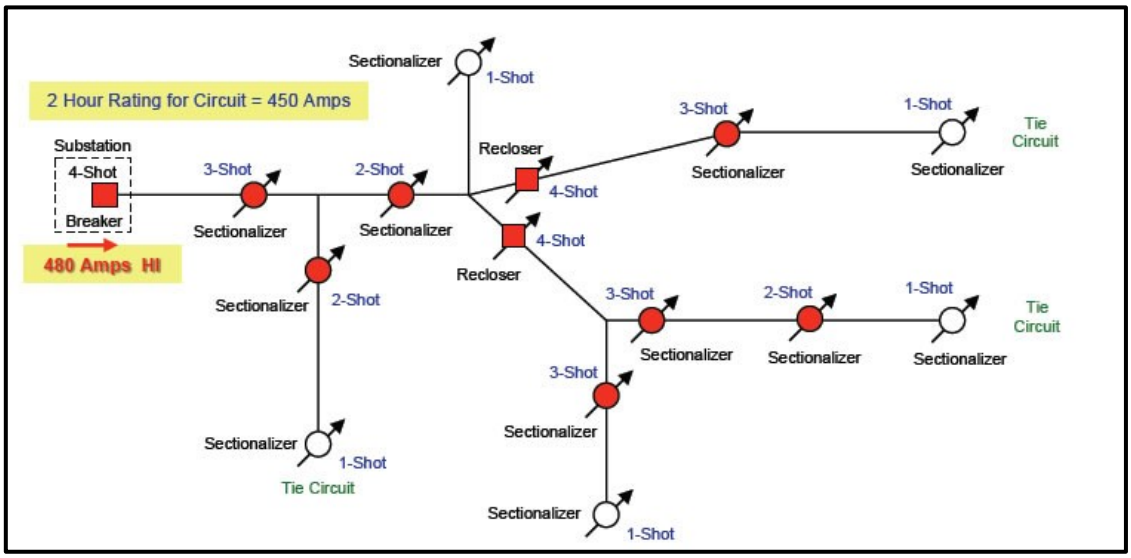

Figure 8. Circuit has Exceeded its 2 Hour Load Rating by 30 Amps

A distribution operator would then take corrective action to relieve the overload condition by transferring parts of the overloaded circuit to more lightly loaded circuits. If N.C. feeder devices and N.O. tie devices are automated by the DA System, then the distribution operator can quickly and easily perform a circuit load transfer using remote controls.

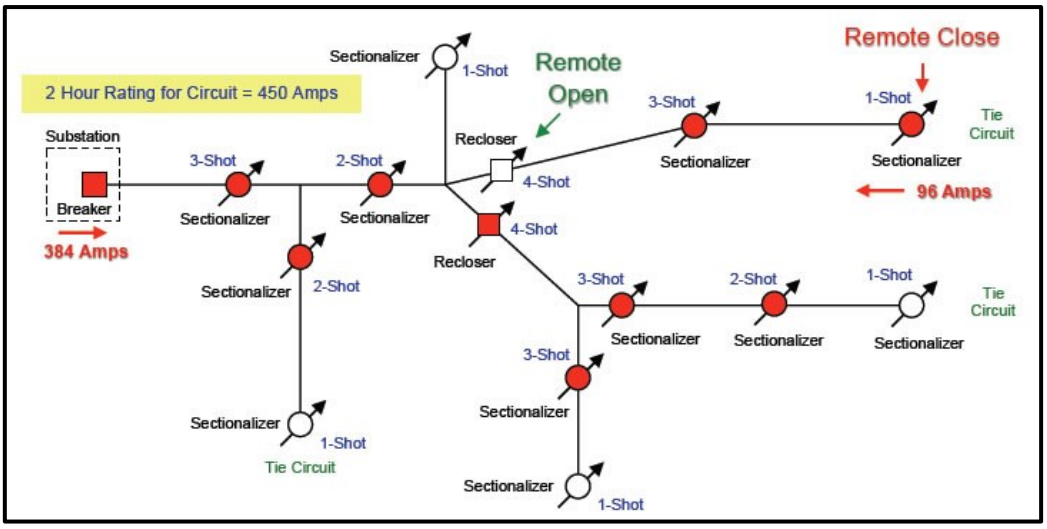

Figure 9. Circuit Loading Returned-to-Normal due to Partial Load Transfer

The operator would close the N.O. tie before opening the N.C. device so that customers do not experience a momentary outage. When the overload is removed, a Return-to-Normal alarm is generated and a Return-to-Normal event is placed into the historical log.

---

[29] Protection Engineers can access information stored in the devices remotely through the DA System.

[30] Lower voltage hydraulic reclosers and sectionalizers generally do not support SCADA functionality. For DA operation, motor operated sectionalizers & reclosers are required.

[31] The opening and reclosing of the station breaker or a downstream recloser during a fault sequence is the mechanism that allows Sectionalizers to coordinate correctly for a fault. However, each time a breaker or recloser closes back into a fault, it stresses and can damage components of the distribution circuit. The new Pulse-Recloser technology is able to determine where a fault is located without requiring a breaker or recloser to reclose repeatedly into the full fault. Pulse-Reclosers pulse the line for very short and precise reclose periods to determine where the fault is located without needing to fully reclose into the fault.

[32] All the information required by the operator to make this decision should be right on the circuit one-line display if it has been designed properly, so it normally take less than 30 seconds. If a crew is working on the circuit, the one-line display will show a tag near the work location and the operator will not take any action until the crew is contacted.

---

c. Automatic Feeder Load Monitoring and Storage

The DA System should provide functionality to selectively monitor distribution analogs (Amps, MW, MVAR, Volts, etc.) for any circuit or other point and produce 15-minute average integrated values that are automatically stored for use by distribution planners and engineers.

d. Improved Verification of Feeder Protection Coordination after each Fault

Distribution circuit fault protection requires feeder devices to coordinate correctly during a fault sequence or the wrong device will lockout affecting more customers than necessary. The DA System allows distribution operators to verify that device coordination worked correctly after every fault sequence. When a problem is found, protection engineers analyze information stored in the System and in the devices[29] to find the cause of the coordination problem.

3. SECTIONALIZERS, RECLOSERS & PULSE-RECLOSERS

Sectionalizers and (Pulse-) Reclosers are distribution circuit protection devices that provide more accurate and more flexible coordination for faults than can be obtained from fuses. Generally, these devices[30] are motor or solenoid operated smart devices that support SCADA remote control and data acquisition. Reclosers are designed to operate like a station breaker and can interrupt fault current and reclose a preset number of times before going to lockout. Sectionalizers count breaker and recloser operations during a fault sequence and open when they reach their preset count while the breaker or recloser is still open. Sectionalizers cannot interrupt fault current.

a. Enhanced Protection on Radial Circuits using Normally Closed

Sectionalizers & (Pulse-) Reclosers Improves Reliability As a means of improving circuit reliability, most electric utilities utilize sectionalizers and reclosers in the design of their distribution circuits to divide the main feeder into a series of load blocks. The sectionalizers and (Pulse-) reclosers are
programmed to coordinate with each other and with the substation breaker so that when a fault occurs, only the closest upstream device to the fault locks out, not the entire circuit. This limits the resulting outage to the faulted load block and all downstream load blocks. Customers upstream of the device that locked out do not have an outage. This protection scheme improves the average reliability of each circuit but this improvement is not equal for all customers on the circuit. Upstream load blocks will generally have much better reliability than downstream load blocks and the last load block will have little improvement.

b. Remote Monitoring & Control of the Feeder Devices

The protection function provided by sectionalizers and reclosers are selfcontained and do not require any communication between the devices for the protection[31] to work properly. The fault current itself followed by loss of voltage when an upstream breaker or recloser opens provides all the information that each device needs to perform its role correctly during a fault sequence. The device just upstream of the actual fault will be the one that locks out. If the substation breaker is monitored by the DA/SCADA System, distribution operators will know that the circuit has operated but will not know which downstream device actually locked out. By adding SCADA monitoring and control to sectionalizers and reclosers, distribution operators will immediately know which device locked
out for the fault plus the status of all the other devices on the circuit.

c. Faster Fault Location & Fault Isolation between Feeder Devices

The fault sequence has completed and the distribution operator is notified by the DA/SCADA System of the problem. The operator then quickly analyzes all the circuit device operations to verify if the protection worked correctly by answering the following:

- How many breaker operations occurred?
- Did any reclosers operate?
- How many "Shots-to-Lockout" is the device that locked out?
- Did the total number of breaker + recloser operations equal this?
- Did any other devices also lock out on the circuit?
- Did the circuit load drop consistently with the lockout?
- Are any line crews working on this circuit?

If the protection worked correctly[32] and no line crews are working on the circuit, the operator will then open the downstream sectionalizer(s), recloser(s) or Pulse- Recloser(s) for the faulted load block using remote control. This will isolate the fault form the rest of the circuit.

d. Faster Restoration of Non-Faulted Line-Sections using N.O. Tie Devices

Once the fault has been isolated from the rest of the circuit, the operator looks for a normally open tie device to an adjacent circuit for use as a temporary feed to restore power to the non-faulted line sections. A quick check of the Tie Amps Available for each tie device will indicate

which ties can be used to pickup the load. Usually the operator calls the chosen tie circuit one-line up on the second

SCADA screen so both circuits can be seen and then closes the tie device remotely. This restores the customers downstream of the faulted line section. Operators can generally restore these customers in less than five minutes from the time the first fault operation occurred on the circuit. If no single tie device can supply the total load that needs to be restored, operators will sectionalize the non-faulted load blocks into two or more sections and attempt to pick up each section through a different tie device. Figure 6 shows a circuit that has been restored through 3 tie devices.

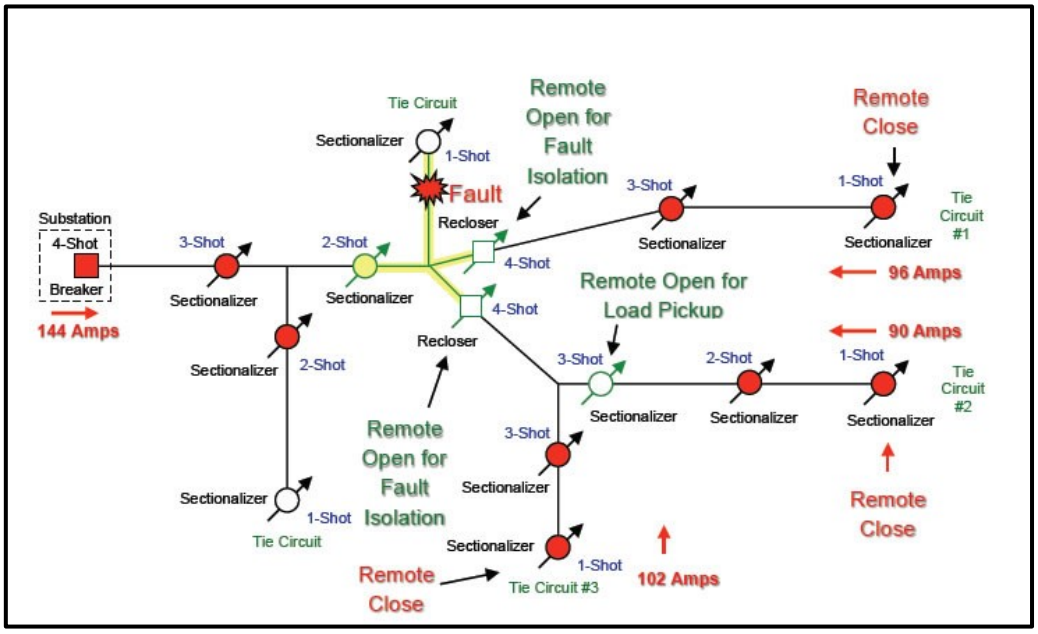

Figure 10. Restoration through three N.O. Tie Sectionalizers after Fault Isolation.

e. Automatic Restoration via Centralized or Field Localized Intelligence

It is possible to have the DA System include software that will automatically perform all the functions that an operator does to isolate a faulted line section and restore power to non-faulted downstream load blocks. One advantage of this is that when more than one circuit has a fault at the same time, the DA System can manage both circuits simultaneously where an operator would have to manage them one at a time.

However, during storms, this auto-restoration functionality should be completely turned off because of the high number of momentary operations and temporary faults that can occur. In

storm conditions, it's generally best to let the storm pass though and then determine where the permanent faults are.

Also, for safety reasons, when line crews are working[33] on a circuit, autorestoration functionality should be turned off for the circuits they are working on. Other circuits can still have auto-restoration functionality enabled. This can be done automatically using the DA/SCADA tagging interface.

Some sectionalizer and recloser manufacturers now offer special in-device software that provides automatic restoration functionality locally within the devices. These devices communicate automatically with other devices in a predefined family and can decide how to restore power within their small group. The DA System could still communicate with and have remote control of these
devices but the auto-restoration would be managed by the devices themselves. The DA System would need to have the ability to turn this auto-restoration function on and off remotely.

Note: Some operations people feel that auto-restoration functionality is not yet as good, as safe or as reliable as having a distribution operator perform the same DA functions. There is evidence to back this up, but it depends greatly on how complex a utility's protection scheme is, how many devices they use on a circuit, and how experienced the operators are. When watching an experienced operator
in action, it's obvious that automated restoration can't be any faster and can't deal with the rare unexpected event the way an operator can. Still, sub-transmission circuits which are not usually as complex as a typical distribution circuit have been using auto-restoration schemes for many years with very good success.

f. Reduced Customer Outage Time & Improved Customer Satisfaction

Section 3a demonstrated how the use of non-automated sectionalizers and reclosers on a distribution circuit can improve average circuit reliability[34], but it also revealed that this improvement is not equal for all customers on the circuit. Upstream customers in load blocks near the substation will see a lot fewer
outages than customers in load blocks near the end of the circuit. Customers in the last load block will continue to experience an outage[35] for every upstream fault. This is not the ideal reliability scenario.

With remote monitoring and control of feeder devices through the DA System, this reliability picture changes significantly. Distribution operators can generally perform fault location, fault isolation and downstream restoration within two to five minutes. Therefore, only customers in the faulted load block will experience a sustained outage.[36] This improves the average reliability for all customers on a circuit equally which certainly advances customer satisfaction.

This analysis demonstrates that the only real way to fully utilize all the potential value that sectionalizers and reclosers offer in terms of improved reliability and customer satisfaction is to automate them with a Distribution Automation System. Otherwise, a lot of their inherent value is lost.

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[33] Line crews generally work lines hot and if they have a problem it's safest not to perform any restoration or switching until it has been verified that all crew members are in the clear and safe.

[34] Assuming that every load block on a circuit is equally likely to experience a fault, the average number of outages that a customer midpoint on the circuit sees will be reduced by about 50%.

[35] Even though customers in the last load block will not see a reduction in the number of outages, these outages will be shorter in duration because field resources can be dispatched to perform fault isolation and downstream restoration using the sectionalizers and reclosers.

[36] The Pennsylvania PUC only considers outages over 5 minutes to be sustained outages. Outages of 5 minute duration or less are considered to be momentary operations that are part of a modern protection and automated restoration scheme.

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g. More Precise Monitoring of Line Section Loads, Phase Balancing & Overloads

One of the important objectives of Smart Grid is for utilities to use information age technologies to avoid potential outages and improve power quality. The DA System accomplishes this by monitoring not only feeder loads at the substation but also downstream line section 3 phase loads, 3 phase voltages and power
factor at each sectionalizer recloser and Pulse-Recloser. The DA System can integrate 15-minute averages for this data and store it for distribution planners to utilize in monitoring:

- 3-Phase Load Balancing
- Load Growth
- Potential Overloads - requiring load relief
- Downstream Voltage Levels

h. Smart Devices Provide New Improved Functionality

An important benefit of utilizing smart devices (sectionalizers, reclosers and Pulse-Reclosers) on distribution feeders is that they not only provide traditional real-time SCADA information, but they also allow 1) historical event data to be downloaded to enable better analysis of fault operations, 2) device diagnostic information to be accessed and 3) configuration data to be viewed. Additionally, they allow configuration changes to be made remotely without having to travel to the device in the field. This is useful for:

- Abnormal Circuit Configuration Setups
- Improving Safety during Line Maintenance Work
- Permanent Circuit Configuration Changes

4. FAULT LOCATORS

The DA System and its automated distribution devices enable faulted load blocks to be quickly identified, isolated and power rerouted to downstream load blocks. However the actual fault still has to be found and repaired by field crews before all customers can be restored. It can sometimes be very difficult to find the actual fault, especially in certain areas[37]. Utilities sometimes install permanent fault locators between automated devices in these problem areas to help narrow the location where crews need to look. Some fault locators support remote monitoring by the DA SCADA System enabling distribution operators to narrow the search area for field crews. These fault locators provide the following benefits:

- More Effective Dispatching of Repair Crews to the Fault Location
- Faster Restoration because the Fault is Found more Quickly
- Reduced Customer Outage Time

5. CAPACITOR BANKS

The Distribution Automation System can be used to monitor and control distribution capacitors that are installed out on the distribution feeders where they can be more effective in controlling voltage and power factor than in the substation.

a. Remote Control & Monitoring of Capacitors

Some capacitor banks that are installed on distribution feeders operate from their own local controllers and they turn on and off automatically without any centralized control. These

capacitors can be monitored by the DA System to verify that they are working correctly and to track voltage levels and power factor.
They can also have their local control settings adjusted remotely for things like change of season. It's also possible to perform a mass request to turn all the capacitors on for special conditions like a peak load day in the summer. However, an individual capacitor's local controller may block this remote close request if voltage is already too high at the capacitor.

b. Automatic Voltage & VAR Control at the Circuit Level

Most SCADA manufacturers offer a Capacitor Control Application that can be used to control distribution capacitors on a circuit-by-circuit basis. The application will automatically turn capacitors on and off based on Voltage and VAR levels monitored over the entire circuit. This can provide more optimized results than local cap controllers and it prevents capacitors from cycling on and off due to
interaction between the local controllers. Also, with a centralized application running, the individual capacitors can utilize a simpler controller.

[37] Certain areas can have a history of being difficult for first responders and crews to find a fault. In these areas it can be very beneficial to install permanent fault locators.

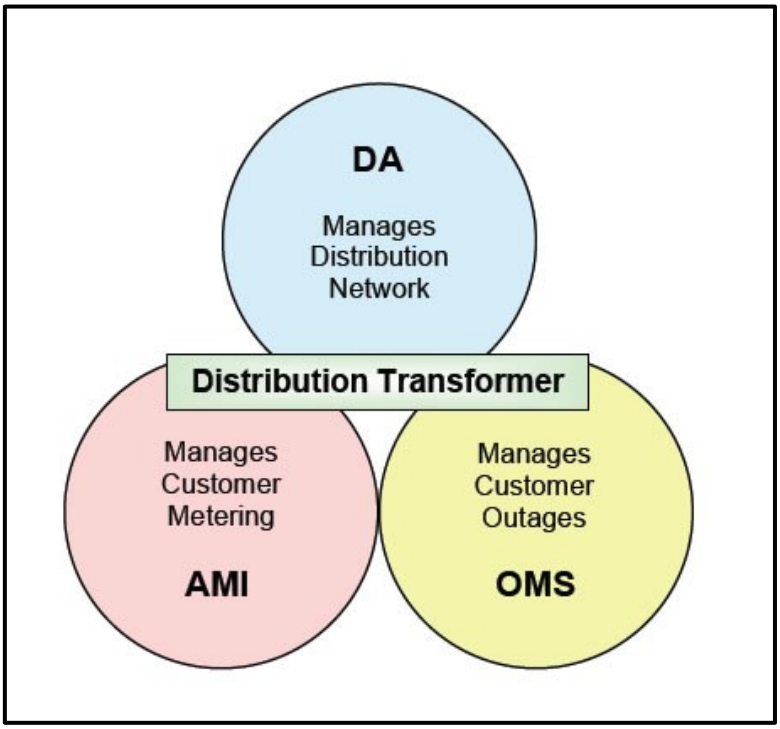
c. Centralized Automatic Voltage & VAR Control (Network-Based)

The Capacitor Control application can also be used to control distribution capacitors on a system-wide basis. The application will automatically turn capacitors on and off based on Voltage and VAR level requirements for the system. This can be especially useful for utilities that don't have their own generation and they need VAR control.

6. DISTRIBUTION TRANSFORMER MONITORING

Direct distribution transformer monitoring is not a traditional function that has been supported by Distribution SCADA Systems. Electric utilities generally have tens of thousands of distribution transformers and SCADA monitoring has not tried to deal with this many individual end points directly in real-time yet. However, the Smart Grid 2030 Vision sees distribution transformers as an important link between the distribution feeder and the customer that needs to be monitored. Therefore, it is inevitable that the technology and functionality needed to accomplish this will soon emerge.

The realm of the distribution transformer actually falls in between three different technologies that are part of the Smart Grid, i.e., Distribution Automation (DA), Advanced Metering Infrastructure (AMI) and Outage Management System (OMS). All three systems have an interest in the distribution transformer but to different degrees.



To the DA System, the distribution transformer is an end point on the distribution feeder. To the AMI System, the distribution transformer is the source of the customer/meter's power. And, to the OMS System, the distribution transformer is an essential and critical component in the customer's network model.

Of the three systems, OMS is the System that really needs distribution transformer information, but it has no mechanism to retrieve it from the field. The DA System has a mechanism to retrieve data from a distribution transformer but no link to it. The AMI System has a direct link to the distribution transformer and a mechanism to retrieve its data through the meter.

Therefore, the AMI System is probably where Smart Grid will focus for retrieving distribution transformer information. The technology is pointing it in this direction because it's a natural fit and 10,000 transformers is not that significant to a system that is already monitoring 500,000+ meters. The AMI System can then pass the transformer information on to the OMS System.

Of course, to make this work efficiently, the distribution transformer manufacturers will need to start building smart-transformers that can communicate with the meter over the secondary service wires. The smart-transformers should provide the following data:

- Secondary Voltage (Analog)
- Secondary Current (Analog)
- Secondary Power (Analog)
- Transformer Temperature (Analog)
- High Temperature Alarm (Status)
- Critical Temperature Alarm (Status)
- Secondary Breaker Open/Close (Status)

It is generally very difficult to identify distribution transformers that are being overloaded due to normal load growth until they either fail or their secondary breaker operates causing an outage. This is especially problem some during summer heat waves when hundreds of distribution transformers can start failing, causing storm like problems for a utility. Distribution transformer load monitoring would help to prevent
this by identifying overload conditions more gradually as they first occur, rather than during the next hot spell.

One additional benefits that distribution transformer load monitoring could provide is "Theft of Power" detection. Transformer real time loads should closely match the sum of the meter loads connected to that transformer[38]. When this is not the case, it could indicate that a meter bypass has been installed at a business or residence, an illegal secondary tap has been connected or there is a problem with the network
model/customer-to-network links for this transformer.

[38] Un-metered services like street lighting would need to be factored into the calculation.

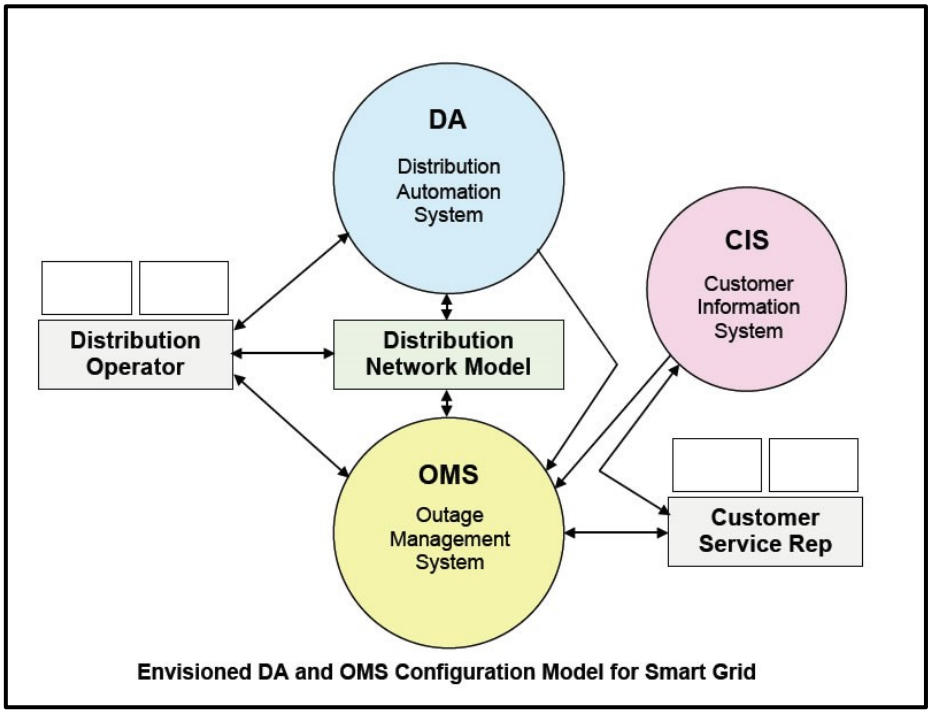
7. THE CUSTOMER - DA & OUTAGE MANAGEMENT

The distribution operator in the forthcoming "Smart Grid Age" will be able to focus more on the end customer because of two highly effective tools that will be very closely integrated with each other, namely, Distribution Automation and Outage Management (OMS). With the DA tool, the operator

will efficiently operate the distribution system and with the OMS tool he will manage customer outages and
customer restoration work.

These two systems will utilize a common distribution network model with an accurate customer-to-network link for every customer. Any action on the DA System will immediately translate to the customers affected on the OMS side. For example, if a sectionalizer is opened on the DA-side causing a forced outage, the operator can immediately look at the OMS-side to see which customers just lost power. The integration will work the other way too. If the OMS indicates that a distribution transformer has lost power, the operator can look at the DA System to examine the distribution feeder powering the failed transformer. The transformer may have lost power because of a blown primary fuse on the distribution circuit.

Existing OMS Systems already utilize some form of a distribution network model that includes a customer-to-network link. However, not all DA Systems have a distribution network model. The challenge will be to have both the DA and OMS Systems use the same network model so that only one model needs to be maintained. The block diagram below shows this configuration.



Envisioned DA and OMS Configuration Model for Smart Grid

The real benefit gained from the envisioned DA and OMS configuration model for Smart Grid is that the Customer Service Department will automatically have near real-time access to outage and

restoration information from the operations side to provide to customers. When a customer calls to report an outage, the correct[39] outage trouble ticket will automatically pop-up on the Customer Service Rep's screen so they can provide the customer with accurate and up-to-date information about their outage, e.g., cause of outage, location of problem, what's currently being done, estimated time of restoration and number of customers affected. For example, if a sectionalizer locks out, the very first customer that calls to report the outage could be told…

[39] Customer is identified automatically by their phone number as the Service Rep answers the call.

"We just had a feeder device lockout on 42nd St & Main due to a circuit fault. We are currently rerouting power around the problem area. Estimated time of restoration is 9:00 PM (2 Hours from now). There are currently 750 customers affected."

Remember, the distribution operator hasn't had time to enter any of this outage information. The DA System provided it automatically to the OMS System. The estimated time of restoration (ETR) for this situation would be a standard default for a sectionalizer lockout which would be used until more is found out about the problem.

This same information can also be made available on the Utility's web site where customers will be able get restoration updates as they occur.

Surveys indicate that customers who have outages are less dissatisfied and rate their electric company higher if they can receive timely and accurate outage/ restoration information when they call[40].

SUMMARY OF THE BENEFITS PROVIDED BY DISTRIBUTION AUTOMATION

The main benefits provided by Distribution Automation have already been covered in the previous sections as various aspects of DA were described. However a more consolidated list of these and some of the additional ancillary benefits that a utility can receive are worth summarizing.

- **Improved SAIFI Reliability Figures (20% to 30% Improvement[41])**
- **Improved SAIDI Reliability Figures (10% to 20% Improvement[42])**
- **Improved Customer Satisfaction**
- **More Efficient and Flexible Distribution System Operation**
  - ✓ Improved monitoring of circuit loads, voltages & power factor.
  - ✓ During peak load periods, circuits can be remotely reconfigured to avoid overloads and potential outages.

- ✓ This can extend equipment life and reduce maintenance costs.

- **Improved Voltage and VAR Control on the Distribution System**
  - ✓ Centralized distribution capacitor control can be optimized by analyzing and coordinating with tap-changer controls.
  - ✓ Distribution voltages are better able to stay within targeted levels over the length of the circuit.
  - ✓ Capacitor maintenance can be reduced by preventing capacitors from cycling on and off due to interaction between local controllers.

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[40] Customers indicate that they are better able to plan their activities during an outage if they receive timely and accurate information about the outage from their electric company.

[41] SAIFI improvements from DA result mainly from the ability to rapidly reroute power to load blocks downstream of a fault so that these customers never see an outage, only a momentary interruption.

[42] SAIDI improvements from DA result mainly from the ability to shorten outages by deploying field crews to outage repairs more quickly & efficiently due to 1) knowing where the problem is, 2) not needing these resources to restore power to downstream load blocks first via manual switching, and 3) faster restoration of the faulted load block after repairs are completed using remote switching.

- **More Flexible and Cost-Efficient Circuit Designs Possible**
  - ✓ Distribution circuits can be longer and have more connected customers without degrading reliability below targeted levels.
  - ✓ Longer circuit design can avoid the need to build new substations or add additional circuits.
- **Improved Distribution System Planning**
  - ✓ Better planning information is available concerning load growth.
  - ✓ Planners are more effective in meeting load growth requirements without over-building.
- **More Effective Distribution System Maintenance**
  - ✓ Circuit protection coordination can be analyzed after every fault and problems can be identified and corrected before they impact reliability.
  - ✓ Device setting changes can be made remotely. This is especially efficient for implementing temporary changes

CONCLUSION

This white paper has taken a close look at Distribution Automation implementation in terms of the new technologies that are part of the "Smart Grid Vision". Many of these information age technologies are already developed, tested & proven and built into products that are readily available from established and trusted manufacturers. Of special importance are the wide range of cost-effective communication options that are now available for DA and the "plug-and-play" compatibility of much of the DA equipment.

The benefits of effective Distribution Automation were also explored with detailed discussions on how DA can help an electric utility significantly improve reliability, operating efficiency, power quality, customer satisfaction and safety. All of these discussions have been based on practical DA experiences and successful implementations.

The final topics of this paper looks to the future when Distribution Automation will be closely integrated with Outage Management and utilize a shared distribution network model and customer-to-network link that will tie the end customer to every action, planned or unplanned, that occurs in the DA System.

Techno Science Academy
The International Open Access Publisher

National Conference on "Innovative Research on Robotics, Circuits and Technology" (IRCT 2018)

Organised by

CIrcuit Branches of
Sri Chandrasekharendra Saraswathi Viswa Mahavidyalaya,
(EEE,ECE,EIE & Mechatronics)
Kanchipuram, Tamil Nadu, India

Publisher

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